Renesas Electronics America Inc - UPD78F0755MC-CAB-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	3-Wire SIO, DALI, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	22
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	30-LSSOP (0.240", 6.10mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0755mc-cab-ax

Documents Related to Development Tools (Software)

Document Name		Document No.
RA78K0 Ver.3.80 Assembler Package User's Manual[Note 1]	Operation	U17199E
	Language	U17198E
	Structured Assembly Language	U17197E
78K0 Assembler Package RA78K0 Ver.4.01 Operating Precautions (Notification Document)[Note 1]		ZUD-CD-07-0181-E
CC78K0 Ver.3.70 C Compiler User's Manual[Note 2]	Operation	U17201E
	Language	U17200E
78K0 C Compiler CC78K0 Ver. 4.00 Operating Precautions (Notification Document)[Note 2]		ZUD-CD-07-0103-E
SM+ System Simulator User's Manual	Operation	U18601E
	User Open Interface	U18212E
ID78K0-QB Ver.2.94 Integrated Debugger User's Manual	Operation	U18330E
ID78K0-QB Ver.3.00 Integrated Debugger User's Manual	Operation	U18492E
PM plus Ver.5.20[Note 3] User's Manual		U16934E
PM+ Ver.6.30[Note 4] User's Manual		U18416E

Notes 1. This document is installed into the PC together with the tool when installing RA78K0 Ver. 4.01. For descriptions not included in "78K0 Assembler Package RA78K0 Ver. 4.01 Operating Precautions", refer to the user's manual of RA78K0 Ver. 3.80.

2. This document is installed into the PC together with the tool when installing CC78K0 Ver. 4.00. For descriptions not included in "78K0 C Compiler CC78K0 Ver. 4.00 Operating Precautions", refer to the user's manual of CC78K0 Ver. 3.70.

3. PM plus Ver. 5.20 is the integrated development environment included with RA78K0 Ver. 3.80.

4. PM+ Ver. 6.30 is the integrated development environment included with RA78K0 Ver. 4.01. Software tool (assembler, C compiler, debugger, and simulator) products of different versions can be managed.

Other Documents

Document Name	Document No.
RENESAS MICROCOMPUTER GENERAL CATALOG	R01CS00001E
Semiconductor Package Mount Manual	**Note**
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

Note See the "Semiconductor Package Mount Manual" website
<R> (http://www.renesas.com/products/package/manual/index.jsp).

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document when designing.

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Table 4-3. Port Functions (78K0/IA2)

Function Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0. 1-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TI000/INTP0/<TOH1>/<TI51>
P20	I/O	Port 2. 6-bit I/O port. Input/output can be specified in 1-bit units.	Analog input	ANI0/AMP-Note
P21				ANI1/AMPOUTNote/PGAINNote
P22				ANI2/AMP+Note
P23				ANI3/CMP2+
P24				ANI4/CMP0+
P25				ANI5/CMP1+
P31	I/O	Port 3. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TOX00/INTP2/TOOLC1
P32				TOX01/INTP3/TOOLD1
P33				TOX10
P34				TOX11/INTP4/<TOH1>/<TI51>
P60	I/O	Port 6. 2-bit I/O port. Input/output can be specified in 1-bit units. Input can be set to SMBus input buffer in 1-bit units. Output can be set to N-ch open-drain output (V_{DD} tolerance). Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SCLA0/TxD6
P61				SDAA0/RxD6
P121	Input	Port 12. 3-bit input-only port. For only P125, use of an on-chip pull-up resistor can be specified by a software setting.	Input port	X1/TOOLC0/<TI000>/<INTP0>
P122				X2/EXCLK/TOOLD0
P125				$\overline{\text{RESET}}$

Note μPD78F0753, 78F0754 (products with operational amplifier) only

Remark Functions in angle brackets < > can be assigned by setting the input switch control register (MUXSEL).

4.5 Settings of Port Mode Register and Output Latch When Using Alternate Function

To use the alternate function of a port pin, set the port mode register and output latch as shown in **Tables 4-13** to **4-16**.

Table 4-13. Settings of Port Mode Register and Output Latch When Using Alternate Function (78K0/IY2) (1/2)

Pin Name	Alternate Function		PM××	P××
	Function Name	I/O		
P20	ANI0[Note 1]	Input	1	×
P21	ANI1[Note 2]	Input	1	×
	PGAIN[Notes 2, 3]	Input	1	×
P23	ANI3[Note 4]	Input	1	×
	CMP2+[Note 4]	Input	1	×
P24	ANI4[Note 4]	Input	1	×
	CMP0+[Note 4]	Input	1	×
P25	ANI5[Note 4]	Input	1	×
	CMP1+[Note 4]	Input	1	×
P31	TOX00	Output	0	0
	INTP2	Input	1	×
	TOOLC1	Input	×	×
P32	TOX01	Output	0	0
	INTP3	Input	1	×
	TOOLD1	I/O	×	×
P33	TOX10	Output	0	0
P34	TOX11	Output	0	0
	INTP4	Input	1	×
	<TOH1>	Output	0	0
	<TI51>	Input	1	×

Notes 1. The pin function can be selected by using ADPC0 register, PM2 register, and ADS register. Refer to **Table 4-7** in **4.2.2 Port 2**.

2. The pin function can be selected by using ADPC0 register, PM2 register, ADS register, and PGAEN bit. Refer to **Table 4-8** in **4.2.2 Port 2**.

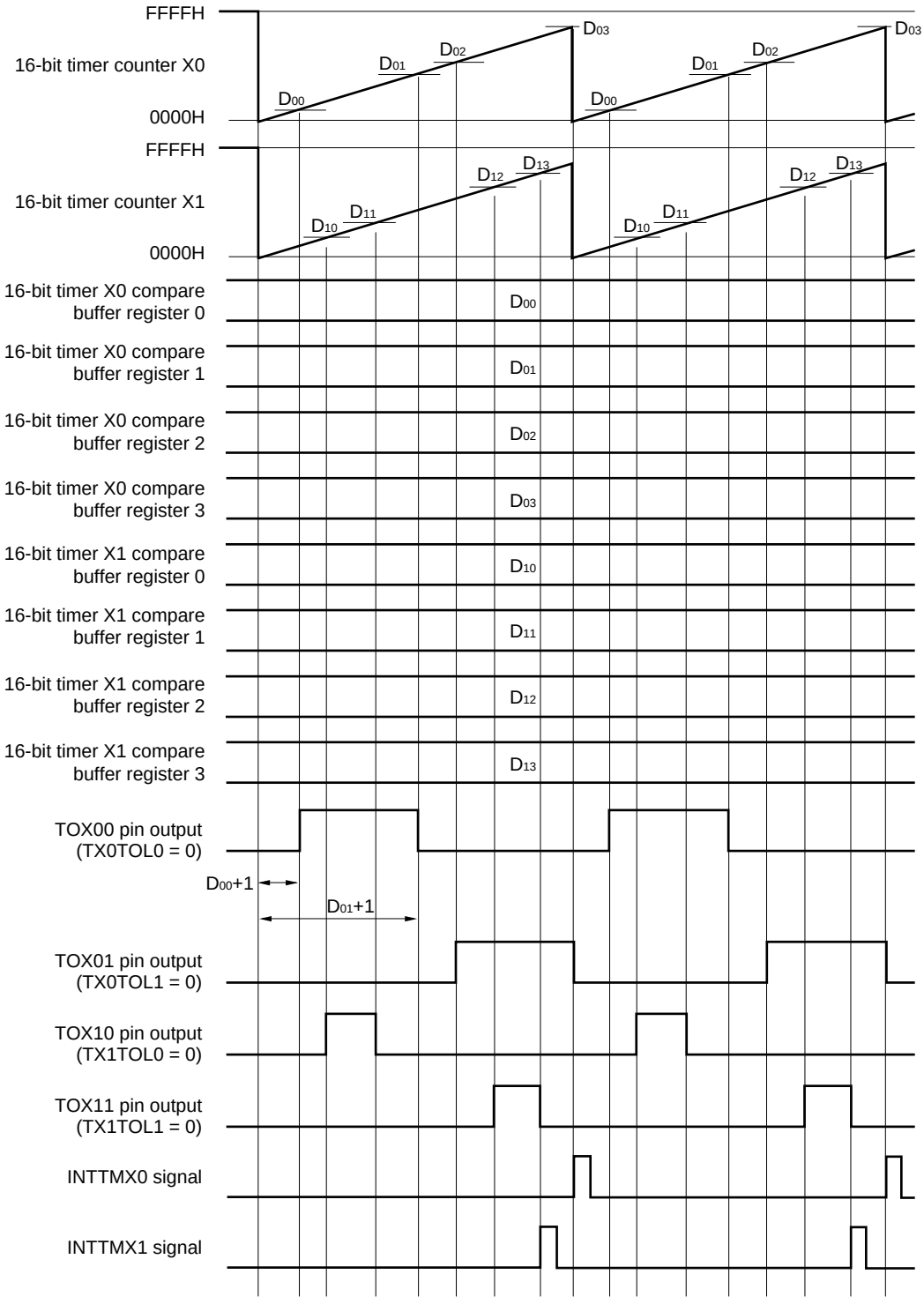
3. μPD78F0750, 78F0751, 78F0752 (products with operational amplifier) only

4. The pin function can be selected by using ADPC0 register, PM2 register, ADS register, and CMPmEN (m = 0-2) bit. Refer to **Table 4-9** in **4.2.2 Port 2**.

Remarks 1. ×: Don't care
PM××: Port mode register
P××: Port output latch

2. Functions in angle brackets < > can be assigned by setting MUXSEL register.

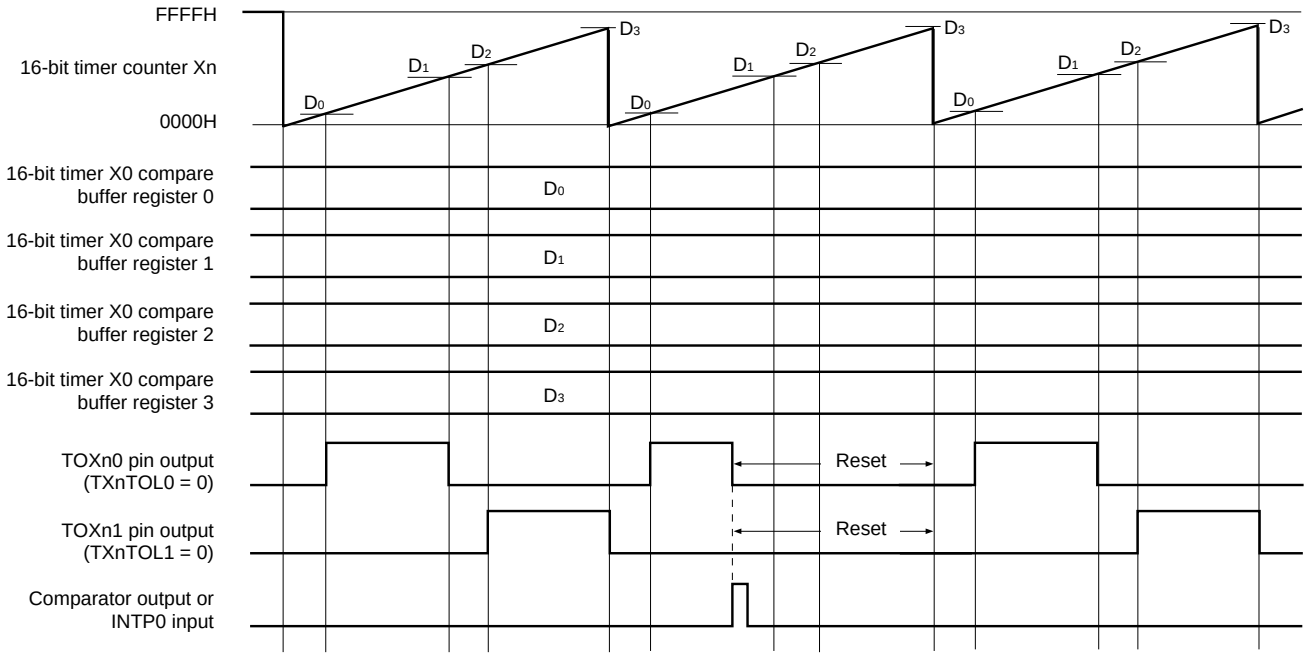
Figure 6-34. PWM Output Timing (Synchronous start/clear mode, TMX0 dual output, TMX1 dual output)



<R>

Remark n = 0, 1

Figure 6-51. Timing of Interlocking mode 3 (timer output reset mode)



Remark n = 0, 1

(2) 16-bit timer capture/compare register 000 (CR000), 16-bit timer capture/compare register 010 (CR010)

CR000 and CR010 are 16-bit registers that are used with a capture function or comparison function selected by using CRC00.

Change the value of CR000 while the timer is stopped (TMC003 and TMC002 = 00).

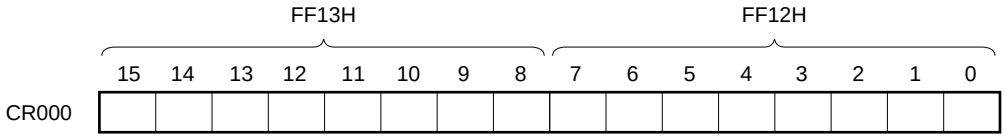
The value of CR010 can be changed during operation if the value has been set in a specific way. For details, refer to **7.5.1 Rewriting CR010 during TM00 operation**.

These registers can be read or written in 16-bit units.

Reset signal generation clears these registers to 0000H.

Figure 7-3. Format of 16-Bit Timer Capture/Compare Register 000 (CR000)

Address: FF12H, FF13H After reset: 0000H R/W



(i) When CR000 is used as a compare register

The value set in CR000 is constantly compared with the TM00 count value, and an interrupt request signal (INTTM000) is generated if they match. The value is held until CR000 is rewritten.

Caution CR000 does not perform the capture operation when it is set in the comparison mode, even if a capture trigger is input to it.

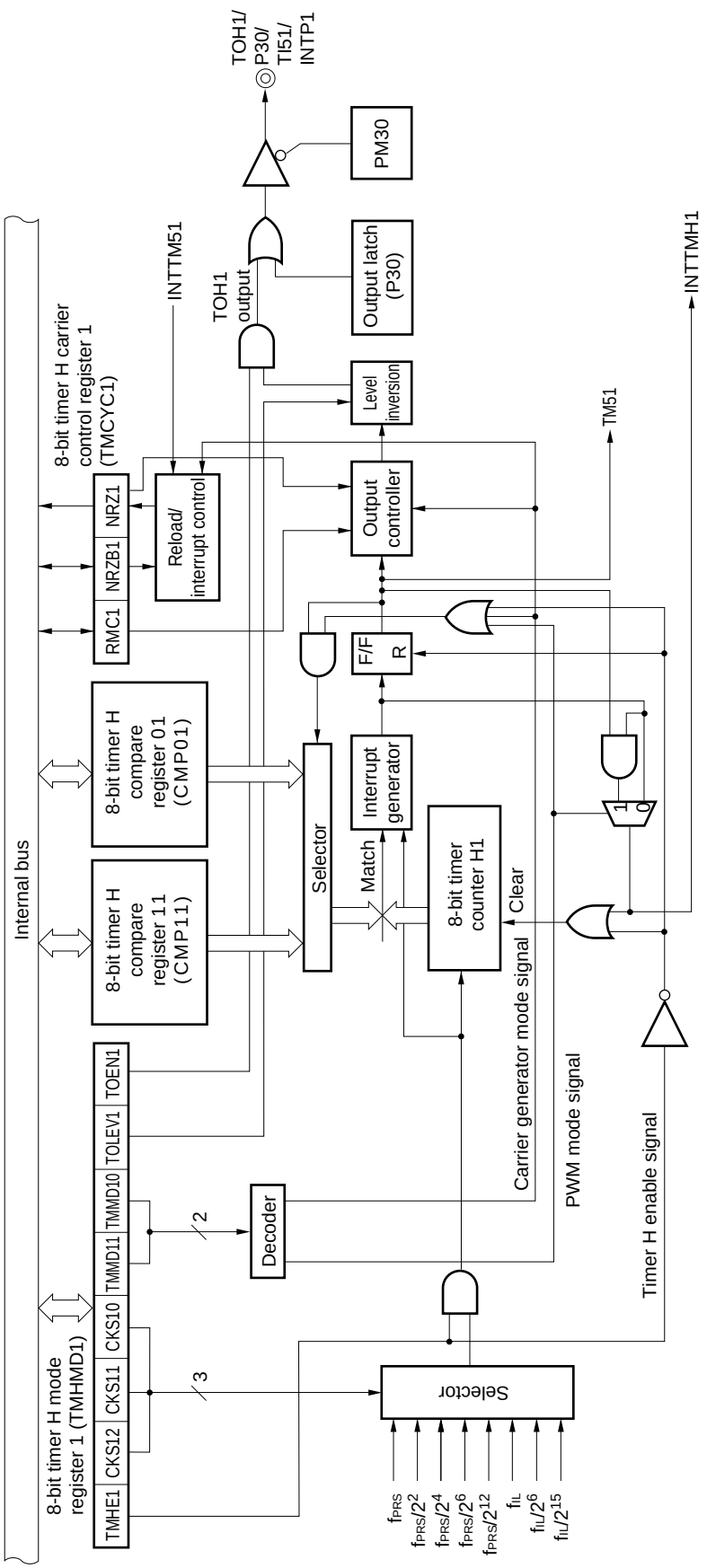
(ii) When CR000 is used as a capture register

The count value of TM00 is captured to CR000 when a capture trigger is input.

As the capture trigger, an edge of a phase reverse to that of the TI000 pin or the valid edge of the TI010 pin[Note] can be selected by using CRC00 or PRM00.

Note The 78K0/IY2, 78K0/IA2, and 78K0/IB2 (32 pins) can be used as capture triggers only at the edge of the inverted phase of the TI000 pin.

Figure 9-1. Block Diagram of 8-Bit Timer H1



Remark 78K0/IY2: <TOH1>/P34/TOX11/<TI51>/INTP4
78K0/IA2, 78K0/IB2 (32 pins): <TOH1>/P00/TI000/<TI51>/INTP0, <TOH1>/P34/TOX11/<TI51>/INTP4
78K0/IB2 (30 pins): TOH1/P30/TI51/INTP1

Figure 13-3. Format of Comparator 1 Control Register (C1CTL)

Address: FF64H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	2	<1>	<0>
C1CTL	CMP1EN	C1DFS1	C1DFS0	C1MODSEL1	C1MODSEL0	0	C1OE	C1INV

CMP1EN	Comparator 1 operation control
0	Stops operation
1	Enables operation Enables input to the external pins (CMP1+) on the positive and negative sides of comparator 1

C1DFS1	C1DFS0	Noise elimination width setting
0	0	Noise filter unused
0	1	$2/f_{PRS}$
1	0	$2^2/f_{PRS}$
1	1	$2^4/f_{PRS}$

C1MODSEL1	C1MODSEL0	Reference voltage selection
0	0	Internal reference voltage: DA0
0	1	Internal reference voltage: DA1
1	0	Internal reference voltage: DA2
1	1	Internal reference voltage: CMPCOM[Note]

C1OE	Enabling or disabling of comparator output
0	Disables output (output signal = fixed to low level)
1	Enables output

C1INV	Output reversal setting
0	Forward
1	Reverse

Note Setting prohibited in the 78K0/IY1 and 78K0/IA2.

Cautions
1. **Rewrite C1DFS1, C1DFS0, C1MODSEL1, C1MODSEL0, C1INV after setting the comparator 1 operation to the disabled state (CMP1EN = 0).**
2. **With the noise elimination width, an extra peripheral hardware clock frequency (f_{PRS}) may be eliminated from the setting value.**
3. **If the comparator output noise interval is within "set noise elimination width + 1 clock", an illegal waveform may be output.**
4. **To use the internal reference voltage, enable (CVRE = 1) operation of the internal reference voltage before enabling (CMP1EN = 1) the comparator operation.**

Remark f_{PRS}: peripheral hardware clock frequency

Figure 14-9. Format of Clock Selection Register 6 (CKSR6)

Address: FF56H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
CKSR6	0	0	0	0	TPS63	TPS62	TPS61	TPS60

TPS63	TPS62	TPS61	TPS60	Base clock (f_{XCLK6}) selection				
					f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 10 MHz	f_{PRS} = 20 MHz (when using PLL)
0	0	0	0	f_{PRS}	2 MHz	5 MHz	10 MHz	20 MHz
0	0	0	1	$f_{PRS}/2$	1 MHz	2.5 MHz	5 MHz	10 MHz
0	0	1	0	$f_{PRS}/2^2$	500 kHz	1.25 MHz	2.5 MHz	5 MHz
0	0	1	1	$f_{PRS}/2^3$	250 kHz	625 kHz	1.25 MHz	2.5 MHz
0	1	0	0	$f_{PRS}/2^4$	125 kHz	312.5 kHz	625 kHz	1.25 MHz
0	1	0	1	$f_{PRS}/2^5$	62.5 kHz	156.25 kHz	312.5 kHz	625 kHz
0	1	1	0	$f_{PRS}/2^6$	31.25 kHz	78.13 kHz	156.25 kHz	312.5 kHz
0	1	1	1	$f_{PRS}/2^7$	15.625 kHz	39.06 kHz	78.13 kHz	156.25 kHz
1	0	0	0	$f_{PRS}/2^8$	7.813 kHz	19.53 kHz	39.06 kHz	78.13 kHz
1	0	0	1	$f_{PRS}/2^9$	3.906 kHz	9.77 kHz	19.53 kHz	39.06 kHz
1	0	1	0	$f_{PRS}/2^{10}$	1.953 kHz	4.88 kHz	9.77 kHz	19.53 kHz
Other than above				Setting prohibited				

Caution Make sure POWER6 = 0 when rewriting TPS63 to TPS60.

Remarks 1. f_{PRS}: Peripheral hardware clock frequency

2. TMC506: Bit 6 of 8-bit timer mode control register 50 (TMC50)
TMC501: Bit 1 of TMC50

14.4.3 DALI mode

This mode is used to perform slave transmission/reception of DALI (Digital Addressable Lighting Interface).

DALI performs communication using the following protocol.

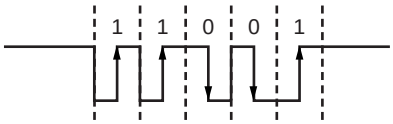
(1) Data structure

<1> Bit definition

A falling edge is bit-defined as “0” and a rising edge as “1”, because DALI communication uses Manchester code.

If no communication is performed, DALI communication is fixed to the high level.

Figure 14-26. Bit Definition

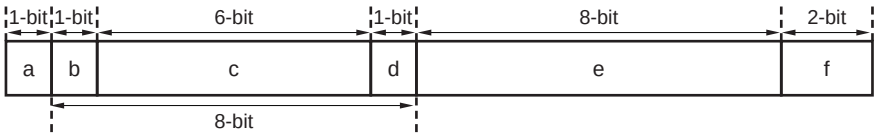


<2> Frame

- Forward frame

This is a frame used when transmitting from the master to a slave. A frame consists of 19 bits.

Figure 14-27. Forward-Frame Structure



a: Start bit

This indicates the start of the frame. It is always the same waveform as “1”.

b-d: Address byte

This specifies the transmission destination of the frame.

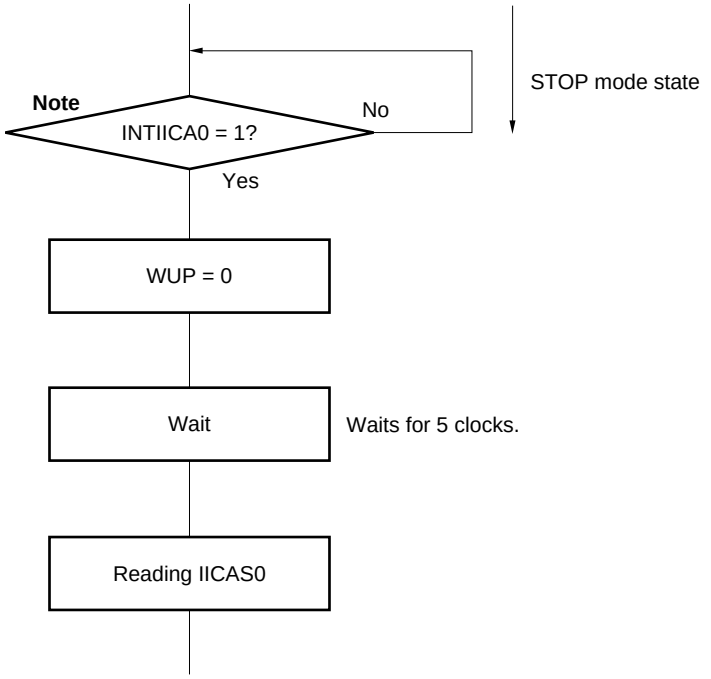
e: Data byte

This specifies a command.

f: Stop bit

This indicates the end of the frame. It is fixed to the high level.

Figure 15-24. Flow When Setting WUP = 0 upon Address Match (Including Extension Code Reception)

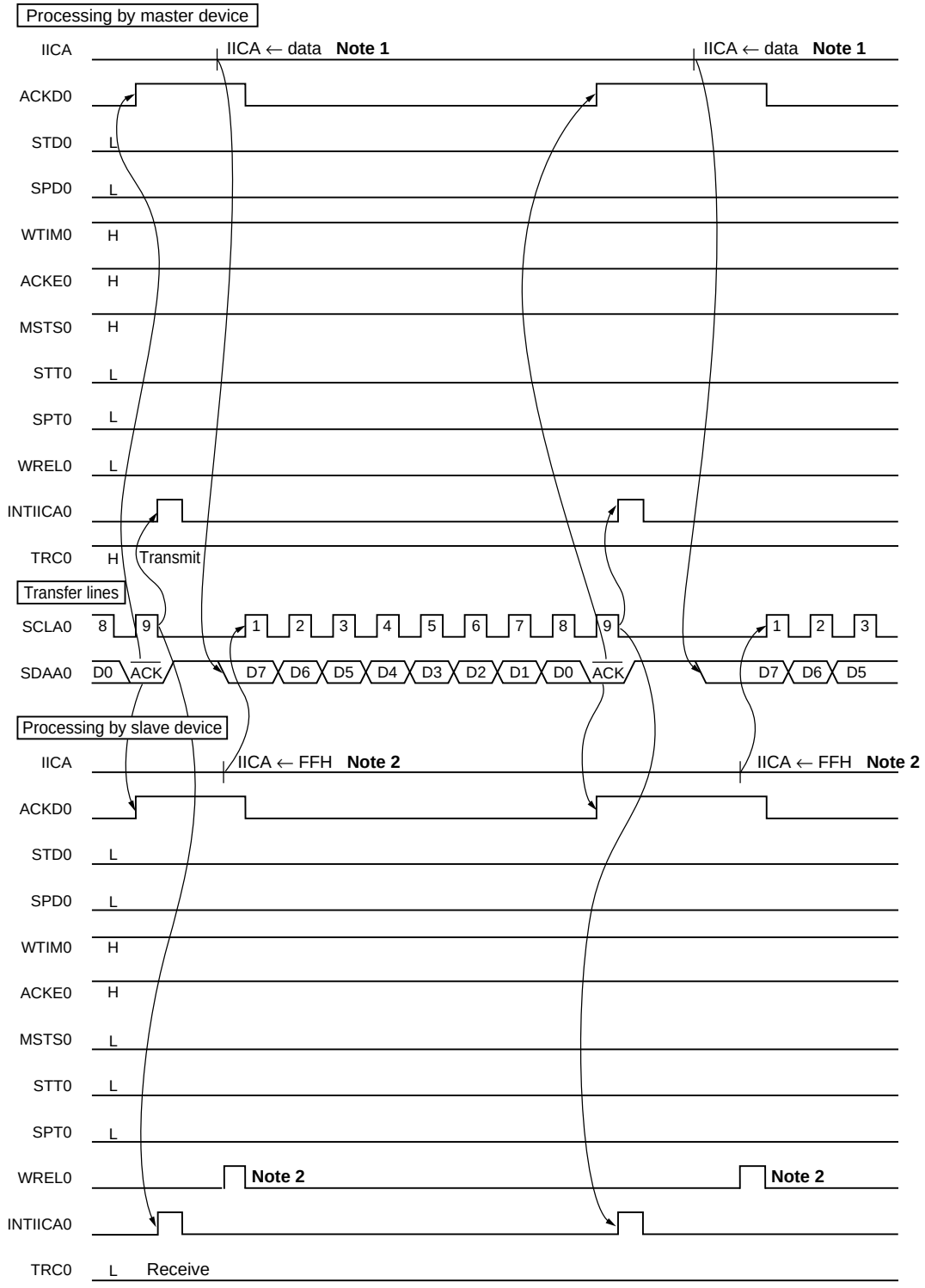


Note Perform the processing after “INTIICA0 = 1?” also when an INTIICA0 vector interrupt occurs.

Use the following flows to perform the processing to release the STOP mode other than by an interrupt request (INTIICA0) generated from serial interface IICA.

Figure 15-33. Example of Master to Slave Communication
(When 9-Clock Wait Is Selected for Both Master and Slave) (2/3)

(2) Data



Notes 1. Write data to IICA, not setting WREL0, in order to cancel a wait state during master transmission.

2. To cancel slave wait, write “FFH” to IICA or set WREL0.

18.3 Registers Controlling Interrupt Functions

The following 7 types of registers are used to control the interrupt functions.

- Interrupt request flag registers (IF0L, IF0H, IF1L, IF1H)
- Interrupt mask flag registers (MK0L, MK0H, MK1L, MK1H)
- Priority specification flag registers (PR0L, PR0H, PR1L, PR1H)
- Port alternate switch control registers (MUXSEL)
- External interrupt rising edge enable registers 0, 1 (EGPCTL0, EGPCTL1)
- External interrupt falling edge enable registers 0, 1 (EGNCTL0, EGNCTL1)
- Program status word (PSW)

Table 18-2 shows a list of interrupt request flags, interrupt mask flags, and priority specification flags corresponding to interrupt request sources.

Table 18-2. Flags Corresponding to Interrupt Request Sources

IY2	IA2	IB2		Interrupt Source	Interrupt Request Flag		Interrupt Mask Flag		Priority Specification Flag	
						Register		Register		Register
16 pins	20 pins	30 pins	32 pins							
√	√	√	√	INTLVI	LVIIF	IF0L	LVIMK	MK0L	LVIPR	PR0L
√	√	√	√	INTP0	PIF0		PMK0		PPR0	
–	–	√	–	INTP1	PIF1		PMK1		PPR1	
√	√	√	√	INTP2	PIF2		PMK2		PPR2	
√	√	√	√	INTP3	PIF3		PMK3		PPR3	
√	√	√	√	INTP4	PIF4		PMK4		PPR4	
–	–	√	√	INTP5	PIF5		PMK5		PPR5	
–	√	√	√	INTSRE6	SREIF6		SREMK6		SREPR6	
–	√	√	√	INTSR6	SRIF6	IF0H	SRMK6	MK0H	SRPR6	PR0H
–	√	√	√	INTST6	STIF6		STMK6		STPR6	
–	–	√	√	INTCSI11	CSIIF11		CSIMK11		CSIPR11	
√	√	√	√	INTTMH1	TMIFH1		TMMKH1		TMPRH1	
√	√	√	√	INTTMX0	TMIFX0		TMMKX0		TMPRX0	
√	√	√	√	INTTMX1	TMIFX1		TMMKX1		TMPRX1	
√	√	√	√	INTTM000	TMIF000		TMMK000		TMPR000	
√	√	√	√	INTTM010	TMIF010		TMMK010		TMPR010	
√	√	√	√	INTAD	ADIF	IF1L	ADMK	MK1L	ADPR	PR1L
√	√	√	√	INTTM51[Note]	TMIF51		TMMK51		TMPR51	
√	√	√	√	INTCMP0	CMPIF0		CMPMK0		CMPPR0	
√	√	√	√	INTCMP1	CMPIF1		CMPMK1		CMPPR1	
√	√	√	√	INTCMP2	CMPIF2		CMPMK2		CMPPR2	
–	√	√	√	INTIICA0	IICAIF0	IF1H	IICAMK0	MK1H	IICAPR0	PR1H

Note When 8-bit timer/event counter 51 is used in the carrier generator mode, an interrupt is generated upon the timing when the INTTM5H1 signal is generated (refer to **Figure 9-13 Transfer Timing**).

Figure 19-2. Format of Oscillation Stabilization Time Select Register (OSTS)

Address: FFA4H After reset: 05H R/W

Symbol	7	6	5	4	3	2	1	0
OSTS	0	0	0	0	0	OSTS2	OSTS1	OSTS0

OSTS2	OSTS1	OSTS0	Oscillation stabilization time selection	
				f_X = 10 MHz
0	0	1	$2^{11}/f_X$	204.8 μs
0	1	0	$2^{13}/f_X$	819.2 μs
0	1	1	$2^{14}/f_X$	1.64 ms
1	0	0	$2^{15}/f_X$	3.27 ms
1	0	1	$2^{16}/f_X$	6.55 ms
Other than above			Setting prohibited	

Cautions 1. To set the STOP mode when the X1 clock is used as the CPU clock, set OSTS before executing the STOP instruction.

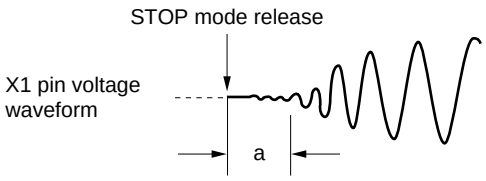
2. Do not change the value of the OSTS register during the X1 clock oscillation stabilization time.

3. The oscillation stabilization time counter counts up to the oscillation stabilization time set by OSTS. If the STOP mode is entered and then released while the internal high-speed oscillation clock is being used as the CPU clock, set the oscillation stabilization time as follows.

- **Desired OSTC oscillation stabilization time ≤ Oscillation stabilization time set by OSTS**

Note, therefore, that only the status up to the oscillation stabilization time set by OSTS is set to OSTC after STOP mode is released.

4. The X1 clock oscillation stabilization wait time does not include the time until clock oscillation starts ("a" below).



Remark f_X: X1 clock oscillation frequency

19.2 Standby Function Operation

19.2.1 HALT mode

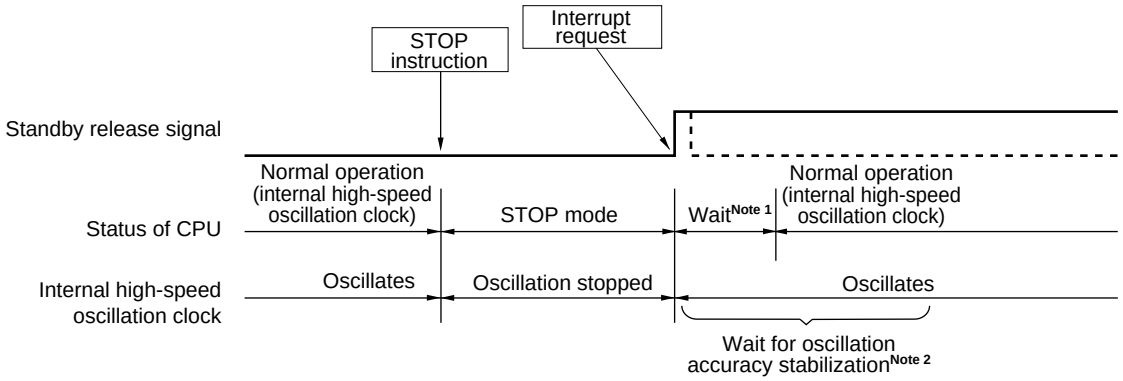
(1) HALT mode

The HALT mode is set by executing the HALT instruction. HALT mode can be set regardless of whether the CPU clock before the setting was the high-speed system clock or internal high-speed oscillation clock.

The operating statuses in the HALT mode are shown below.

Figure 19-6. STOP Mode Release by Interrupt Request Generation (2/2)

(3) When internal high-speed oscillation clock is used as CPU clock



Notes 1. The wait time is as follows:

- When vectored interrupt servicing is carried out: 17 or 18 clocks
- When vectored interrupt servicing is not carried out: 11 or 12 clocks

2. The wait time for oscillation accuracy stabilization is as follows:

- RMC register = 00H: 102 to 407 μs
- RMC register = 56H: 120 to 481 μs

Remark The broken lines indicate the case when the interrupt request that has released the standby mode is acknowledged.

(b) Release by reset signal generation

When the reset signal is generated, STOP mode is released, and then, as in the case with a normal reset operation, the program is executed after branching to the reset vector address.

Figure 24-1. Format of Option Byte (3/3)

Address: 0083H/1083H[Note]

7	6	5	4	3	2	1	0
0	0	0	1	1	1	OCDPSEL	0

OCDPSEL	Pin selection used during on-chip debugging
0	TOOLC1/P31, TOOLD1/P32
1	TOOLC0/X1, TOOLD0/X2

Note Set a value that is the same as that of 0083H to 1083H because 0083H and 1083H are switched during the boot swap operation.

Caution Be sure to clear bits 7 to 5 and 0 to "0" and set bits 4 to 2 to "1".

Address: 0084H/1084H[Note]

7	6	5	4	3	2	1	0
0	0	0	0	0	0	OCDEN1	OCDEN0

OCDEN1	OCDEN0	On-chip debug operation control
0	0	Operation disabled
0	1	Setting prohibited
1	0	Operation enabled. Does not erase data of the flash memory in case authentication of the on-chip debug security ID fails.
1	1	Operation enabled. Erases data of the flash memory in case authentication of the on-chip debug security ID fails.

Note Set a value that is the same as that of 0084H to 1084H because 0084H and 1084H are switched during the boot swap operation.

Caution Be sure to clear bits 7 to 2 to "0".

Remark For the on-chip debug security ID, refer to **CHAPTER 26 ON-CHIP DEBUG FUNCTION**.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

28.4.2 Serial interface

(T_A = –40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = AV_{SS} = 0 V)

(a) UART6/DALI (dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					625	kbps

(b) IICA

Parameter	Symbol	Conditions	Standard Mode		High-Speed Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode: f_{PRS} ≥ 3.5 MHz, Normal mode: f_{PRS} ≥ 1 MHz	0	100	0	400	kHz
Setup time of start condition and stop condition	$t_{SU: STA}$		4.7	–	0.6	–	μs
Hold time[Note 1]	$t_{HD: STA}$		4.0	–	0.6	–	μs
Hold time when SCLA0 = "L"	t_{LOW}		4.7	–	1.3	–	μs
Hold time when SCLA0 = "H"	t_{HIGH}		4.0	–	0.6	–	μs
Data setup time (reception)	$t_{SU: DAT}$		250	–	100	–	ns
Data hold time (transmission)[Notes 2,3]	$t_{HD: DAT}$		0	3.45	0	0.9	μs
Setup time of stop condition	$t_{SU: STO}$		4.0	–	0.6	–	μs
Bus free time between stop condition and start condition	t_{BUF}		4.7	–	1.3	–	μs
Rise time of SDAA0 and SCLA0 signals	t_R			1000	20+ 0.1C_b	300	ns
Fall time of SDAA0 and SCLA0 signals	t_F			300	20+ 0.1C_b	300	ns
Total load capacitance value of each communication line (SCLA0, SDAA0)	C_b			400		400	pF

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the $\overline{ACK}$ (acknowledge) timing.

3. The data hold time differs depending on the setting of the IICA low-level width setting register (IICWL).

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

28.5.4 Operational amplifier

(T_A = –40 to +105°C, 2.7 V ≤ AV_{REF} ≤ V_{DD} ≤ 5.5 V, V_{SS} = AV_{SS} = 0 V, Output load: R_L = 47 kΩ, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input offset voltage	V_{IOP}	V_{BIAS} = 1/2 V_{DD}, AV_{REF} = 3.0 V			±10	mV
Output voltage, high	V_{OHOP0}	AV_{REF} = 3.0 V/2.2 V, I_{OH} = – 500 μA	AV_{REF} – 0.2			V
Output voltage, low	V_{OLOP0}	AV_{REF} = 3.0 V/2.2 V, I_{OL} = 500 μA			0.1	V
Common-mode input voltage	V_{ICMOP0}	AV_{REF} = 3.0 V/2.2 V	0		AV_{REF} – 0.6	V
Slew rate	SR_{OP0}	AV_{REF} = 3.0 V		1.8		V/μs
		AV_{REF} = 5.0 V		2.0		V/μs
Input noise spectral density (Inoise)		AV_{REF} = 3.0 V, V_{IN} = 0.1 V, f = 1 kHz		73		nV / √Hz
		AV_{REF} = 3.0 V, V_{IN} = AV_{REF}/2 V, f = 1 kHz		60		
		AV_{REF} = 3.0 V, V_{IN} = AV_{REF} –0.6 V, f = 1 kHz		55		
Phase margin		AV_{REF} = 3.0 V		40		deg
Large-amplitude voltage gain	AV_{OP0}	AV_{REF} = 3.0 V		100		dB
Gain-bandwidth product	GBW_{OP0}	AV_{REF} = 5.0 V/3.0 V		3.0		MHz
Operation stabilization wait time[Note]	t_{OP0}	AV_{REF} = 3.0 V		10		μs

Note Time required until a state is entered where the DC and AC specifications of the operational amplifier 0 are satisfied after the operational amplifier 0 operation has been enabled (OPAMP0E = 1).