Renesas Electronics America Inc - UPD78F0756MC-CAB-AX Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	3-Wire SIO, DALI, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	22
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	30-LSSOP (0.240", 6.10mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0756mc-cab-ax

Table 4-5. Port Functions (78K0/IB2 (32 Pins))

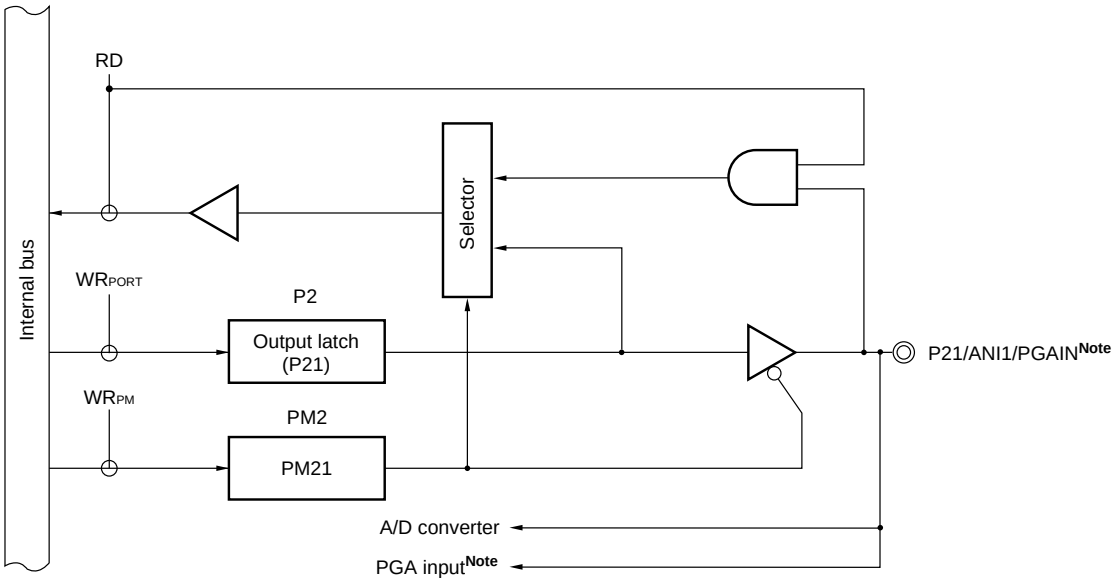
Function Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0. 3-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TI000/INTP0/<TOH1>/<TI51>
P02				$\overline{\text{SSI11}}$/INTP5
P20	I/O	Port 2. 8-bit I/O port. Input/output can be specified in 1-bit units.	Analog input	ANI0/AMP-Note
P21				ANI1/AMPOUTNote/PGAINNote
P22				ANI2/AMP+Note
P23				ANI3/CMP2+
P24				ANI4/CMP0+
P25				ANI5/CMP1+
P26				ANI6/CMPCOM
P27				ANI7
P31	I/O	Port 3. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TOX00/INTP2/TOOLC1
P32				TOX01/INTP3/TOOLD1
P33				TOX10
P34				TOX11/INTP4/<TOH1>/<TI51>
P35				$\overline{\text{SCK11}}$
P36				SI11
P37				SO11
P60	I/O	Port 6. 2-bit I/O port. Input/output can be specified in 1-bit units. Input can be set to SMBus input buffer in 1-bit units. Output can be set to N-ch open-drain output (V_{DD} tolerance). Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SCLA0/TxD6
P61				SDAA0/RxD6
P70	I/O	Port 7. 1-bit I/O port. Input/output can be specified in 1-bit units.	Analog input	ANI8
P121	Input	Port 12. 3-bit input port. For only P125, use of an on-chip pull-up resistor can be specified by a software setting.	Input port	X1/TOOLC0/<TI000>/<INTP0>
P122				X2/EXCLK/TOOLD0
P125				$\overline{\text{RESET}}$

Note μPD78F0755, 78F0756 (products with operational amplifier) only

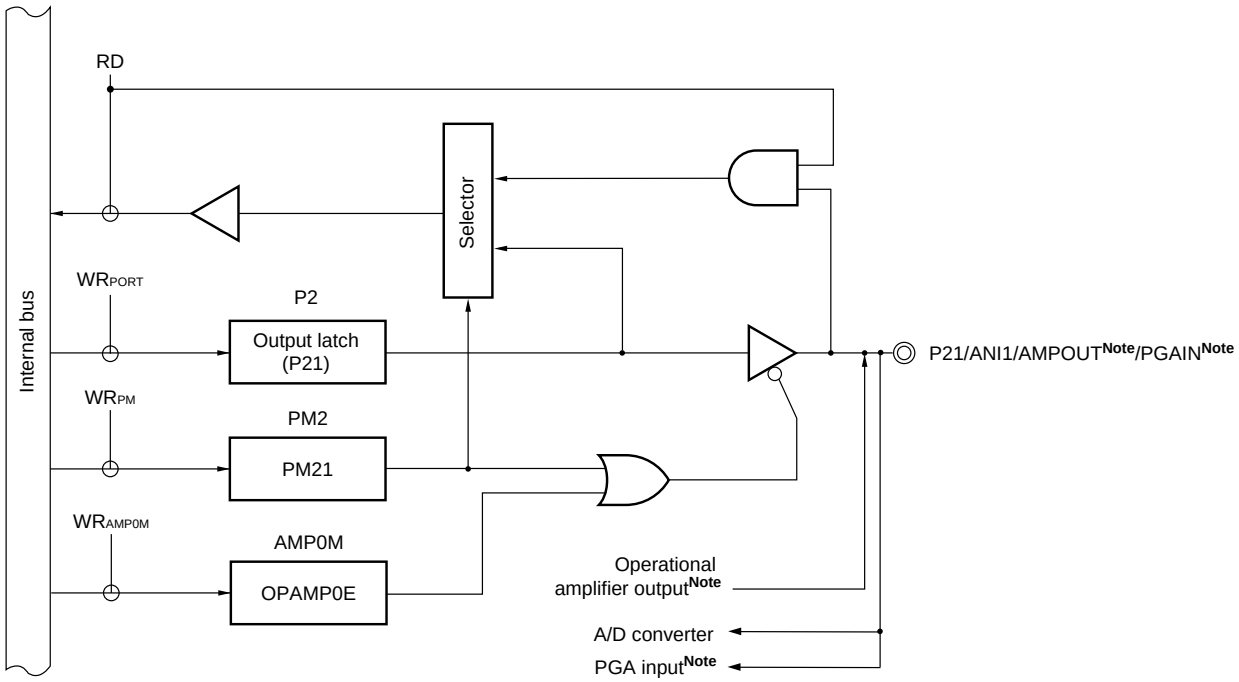
Remark Functions in angle brackets < > can be assigned by setting the input switch control register (MUXSEL).

Figure 4-5. Block Diagram of P21

(1) 78K0/IY2



(2) 78K0/IA2, 78K0/IB2



P2: Port register 2
PM2: Port mode register 2
AMP0M: Operational amplifier 0 control register
RD: Read signal
WR××: Write signal

Note Products with operational amplifier only

Remark PGA: Programmable Gain Amplifier

Table 4-15. Settings of Port Mode Register and Output Latch When Using Alternate Function (78K0/IB2 (30 pins)) (1/2)

Pin Name	Alternate Function		PM××	P××
	Function Name	I/O		
P00	TI000	Input	1	×
	INTP0	Input	1	×
P01	TI010	Input	1	×
	TO00	Output	0	0
P02	$\overline{SSI11}$	Input	1	×
	INTP5	Input	1	×
P20	ANI0Note 1	Input	1	×
	AMP-Notes 1, 2	Input	1	×
P21	ANI1Note 3	Input	1	×
	AMPOUTNotes 2, 3	Output	1	×
	PGAINNotes 2, 3	Input	1	×
P22	ANI2Note 1	Input	1	×
	AMP+Notes 1, 2	Input	1	×
P23	ANI3 Note 4	Input	1	×
	CMP2+Note 4	Input	1	×
P24	ANI4Note 4	Input	1	×
	CMP0+Note 4	Input	1	×
P25	ANI5Note 4	Input	1	×
	CMP1+Note 4	Input	1	×
P26	ANI6Note 5	Input	1	×
	CMPCOMNote 5	Input	1	×
P27	ANI7Note 6	Input	1	×
P30	INTP1	Input	1	×
	TI51	Input	1	×
	TOH1	Output	0	0

Notes 1. The pin function can be selected by using ADPC0 register, PM2 register, ADS register, and OPAMP0E bit. Refer to **Table 4-7** in **4.2.2 Port 2**.

2. μPD 78F0755, 78F0756 (products with operational amplifier) only

3. The pin function can be selected by using ADPC0 register, PM2 register, ADS register, OPAMP0E bit, and PGAEN bit. Refer to **Table 4-8** in **4.2.2 Port 2**.

4. The pin function can be selected by using ADPC0 register, PM2 register, ADS register, and CMPmEN (m = 0-2) bit. Refer to **Table 4-9** in **4.2.2 Port 2**.

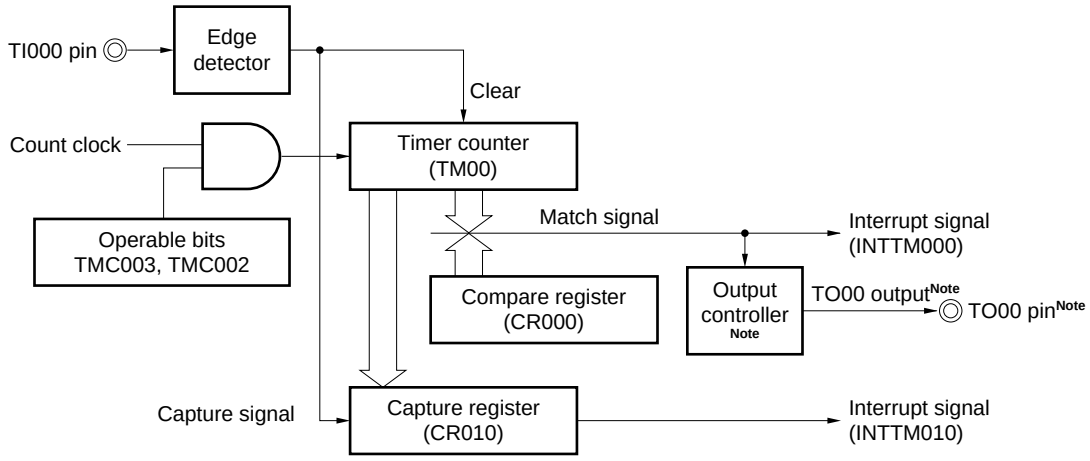
5. The pin function can be selected by using ADPC0 register, PM2 register, ADS register, and CmMODSEL1, CmMODSEL0 (m = 0-2) bit. Refer to **Table 4-10** in **4.2.2 Port 2**.

6. The pin function can be selected by using ADPC0 register, PM2 register, and ADS register. Refer to **Table 4-11** in **4.2.2 Port 2**.

Remark ×: Don't care
PM××: Port mode register
P××: Port output latch

(2) Operation in clear & start mode entered by TI000 pin valid edge input
(CR000: compare register, CR010: capture register)

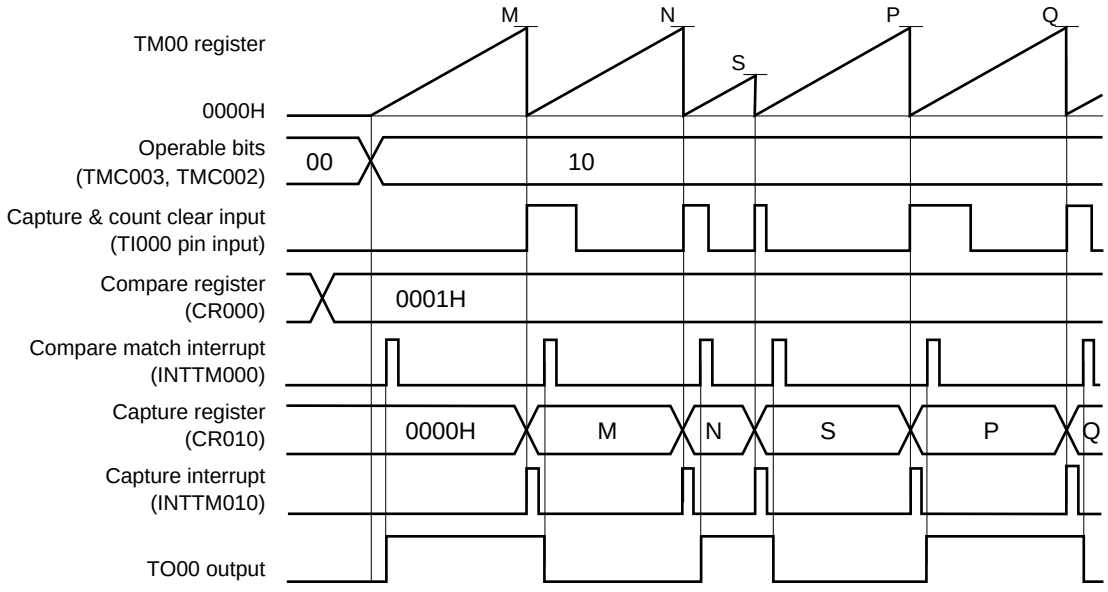
Figure 7-25. Block Diagram of Clear & Start Mode Entered by TI000 Pin Valid Edge Input (CR000: Compare Register, CR010: Capture Register)



Note 78K0/IB2 (30 pins) only

Figure 7-26. Timing Example of Clear & Start Mode Entered by TI000 Pin Valid Edge Input (CR000: Compare Register, CR010: Capture Register) (1/2)

(a) TOC00 = 13H, PRM00 = 10H, CRC00 = 04H, TMC00 = 08H, CR000 = 0001H



This is an application example where the TO00 output level is inverted when the count value has been captured & cleared.

The count value is captured to CR010 and TM00 is cleared (to 0000H) when the valid edge of the TI000 pin is detected. When the count value of TM00 is 0001H, a compare match interrupt signal (INTTM000) is generated, and the TO00 output level is inverted.

Figure 9-4. Format of 8-Bit Timer H Mode Register 1 (TMHMD1)

Address: FF6CH After reset: 00H R/W

	<7>	6	5	4	3	2	<1>	<0>
TMHMD1	TMHE1	CKS12	CKS11	CKS10	TMMD11	TMMD10	TOLEV1	TOEN1

TMHE1	Timer operation enable
0	Stops timer count operation (counter is cleared to 0)
1	Enables timer count operation (count operation started by inputting clock)

CKS12	CKS11	CKS10	Count clock selection				
				f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 10 MHz	f_{PRS} = 20 MHz (when using PLL)
0	0	0	f_{PRS}	2 MHz	5 MHz	10 MHz	20 MHz
0	0	1	$f_{PRS}/2^2$	500 kHz	1.25 MHz	2.5 MHz	5 MHz
0	1	0	$f_{PRS}/2^4$	125 kHz	312.5 kHz	625 kHz	1.25 MHz
0	1	1	$f_{PRS}/2^6$	31.25 kHz	78.13 kHz	156.25 kHz	312.5 kHz
1	0	0	$f_{PRS}/2^{12}$	0.49 kHz	1.22 kHz	2.44 kHz	4.88 kHz
1	0	1	$f_{IL}/2^6$	0.47 kHz (TYP.)			
1	1	0	$f_{IL}/2^{15}$	0.92 Hz (TYP.)			
1	1	1	f_{IL}	30 kHz (TYP.)			

TMMD11	TMMD10	Timer operation mode
0	0	Interval timer mode
0	1	Carrier generator mode
1	0	PWM output mode
1	1	Setting prohibited

TOLEV1	Timer output level control (in default mode)
0	Low level
1	High level

TOEN1	Timer output control
0	Disables output
1	Enables output

Cautions 1. When TMHE1 = 1, setting the other bits of TMHMD1 is prohibited. However, TMHMD1 can be refreshed (the same value is written).

2. In the PWM output mode and carrier generator mode, be sure to set the 8-bit timer H compare register 11 (CMP11) when starting the timer count operation (TMHE1 = 1) after the timer count operation was stopped (TMHE1 = 0) (be sure to set again even if setting the same value to CMP11).

3. When the carrier generator mode is used, set so that the count clock frequency of TMH1 becomes more than 6 times the count clock frequency of TM51.

When using P20/AMP-/ANI0 to P27/ANI7, and P70/ANI8, set the registers according to the pin function to be used (refer to **Tables 11-3** to **11-8**).

Table 11-3. Setting Functions of P20/ANI0/AMP-, P22/ANI2/AMP+ Pins

ADPC0 Register	PM2 Register	OPAMP0E bit [Note]	ADS Register (n = 0, 2)	P20/ANI0/AMP-, P22/ANI2/AMP+ Pins
Digital I/O selection	Input mode	–	Selects ANIn.	Setting prohibited
			Does not select ANIn.	Digital input
	Output mode	–	Selects ANIn.	Setting prohibited
			Does not select ANIn.	Digital output
Analog input selection	Input mode	0	Selects ANIn.	Analog input (to be converted into digital signal)
			Does not select ANIn.	Analog input (not to be converted into digital signal)
		1	Selects ANIn.	Analog input (to be converted into digital signal), and operational amplifier input
			Does not select ANIn.	Operational amplifier input
	Output mode	–	–	Setting prohibited

Note 78K0/IA2, 78K0/IB2 only

Remark ADPC0: A/D port configuration register 0
PM2: Port mode register 2
OPAMP0E: Bit 7 of operational amplifier 0 control register (AMP0M)
ADS: Analog input channel specification register

(5) Full-scale error

This shows the difference between the actual measurement value of the analog input voltage and the theoretical value (Full-scale − 3/2LSB) when the digital output changes from 1.....110 to 1.....111.

(6) Integral linearity error

This shows the degree to which the conversion characteristics deviate from the ideal linear relationship. It expresses the maximum value of the difference between the actual measurement value and the ideal straight line when the zero-scale error and full-scale error are 0.

(7) Differential linearity error

While the ideal width of code output is 1LSB, this indicates the difference between the actual measurement value and the ideal value.

Figure 11-21. Zero-Scale Error

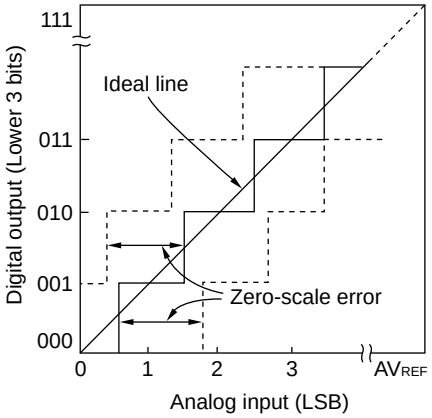


Figure 11-22. Full-Scale Error

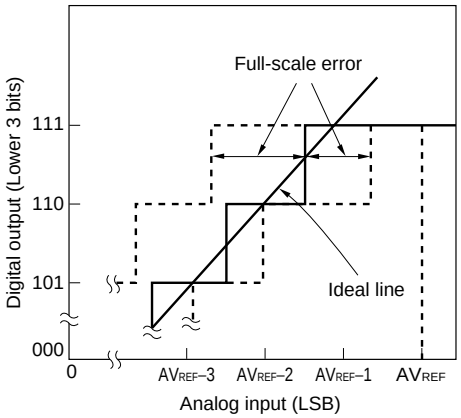


Figure 11-23. Integral Linearity Error

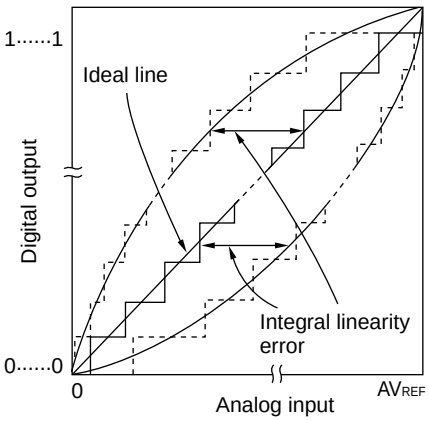
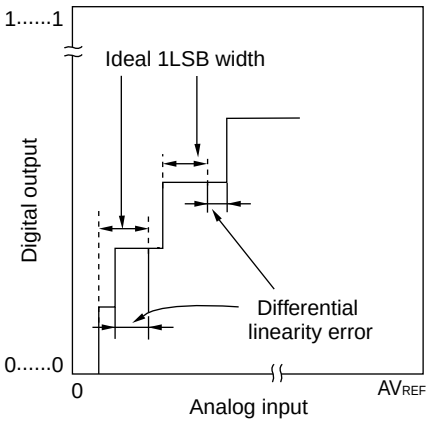


Figure 11-24. Differential Linearity Error



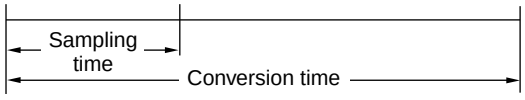
(8) Conversion time

This expresses the time from the start of sampling to when the digital output is obtained.

The sampling time is included in the conversion time in the characteristics table.

(9) Sampling time

This is the time the analog switch is turned on for the analog voltage to be sampled by the sample & hold circuit.



CHAPTER 12 OPERATIONAL AMPLIFIER

Item	78K0/IY2	78K0/IA2	78K0/IB2	
	16 Pins	20 Pins	30 Pins	32 Pins
Operational amplifier (products with operational amplifier only)	1 ch (PGA mode only)	1 ch (Single AMP mode and PGA mode)		

12.1 Function of Operational Amplifier

Operational amplifier is mounted onto products with operational amplifier of the 78K0/Ix2 microcontrollers. The operational amplifier has the following modes.

- **Single AMP mode**[Note]
  Operational amplifier has two input pins (the AMP- pin and the AMP+ pin) and one output pin (the AMPOUT pin), and can be used as single-power supply amplifier that can be externally connected.
  The amplified voltage can be used as an analog input of the A/D converter, because the AMPOUT pin is alternatively used with analog input pin of the A/D converter.

  Note Products with operational amplifier of the 78K0/IA2, 78K0/IB2 only.

- **PGA (Programmable gain amplifier) mode**
  In this mode, the analog voltage input from the PGAIN pin is amplified within the microcontroller. The gain can be selected from four types (×4, ×8, ×16, ×32).
  The amplified voltage can be used as an analog input of the A/D converter.

The relationship between the register settings and pins is shown below.

Table 14-2. Relationship Between Register Settings and Pins

POWER6	TXE6	RXE6	PM60	P60	PM61	P61	POM60	POM61	UART6 Operation	Pin Function	
										TxD6/ SCLA0/ P60	RxD6/ SDAA0/ P61
0	0	0	×Note	×Note	×Note	×Note	×Note	×Note	Stop	P60	P61
			0	1	0	1	1	1		SCLA0	SDAA0
1	0	1	×Note	×Note	1	×	×Note	×	Reception	P60	RxD6
	1	0	0	1	×Note	×Note	0	×Note	Transmission	TxD6	P61
	1	1	0	1	1	×	0	×	Transmission/ reception	TxD6	RxD6

Note Can be set as port function.

Remark ×: don't care
POWER6: Bit 7 of UART/DALI operation mode register 6 (ASIM6)
TXE6: Bit 6 of ASIM6
RXE6: Bit 5 of ASIM6
PM6×: Port mode register
P6×: Port output latch
POM60, POM61: Bits 0 and 1 of Port output mode register 6 (POM6)

Example: Frequency of base clock = 10 MHz = 10,000,000 Hz
Set value of MDL67 to MDL60 bits of BRGC6 register = 00100001B (k = 33)
Target baud rate = 153600 bps

Baud rate (UART) = 10 M / (2 × 33)
= 10000000 / (2 × 33) = 151,515 [bps]

Error = (151515/153600 − 1) × 100
= −1.357 [%]

(3) Example of setting baud rate

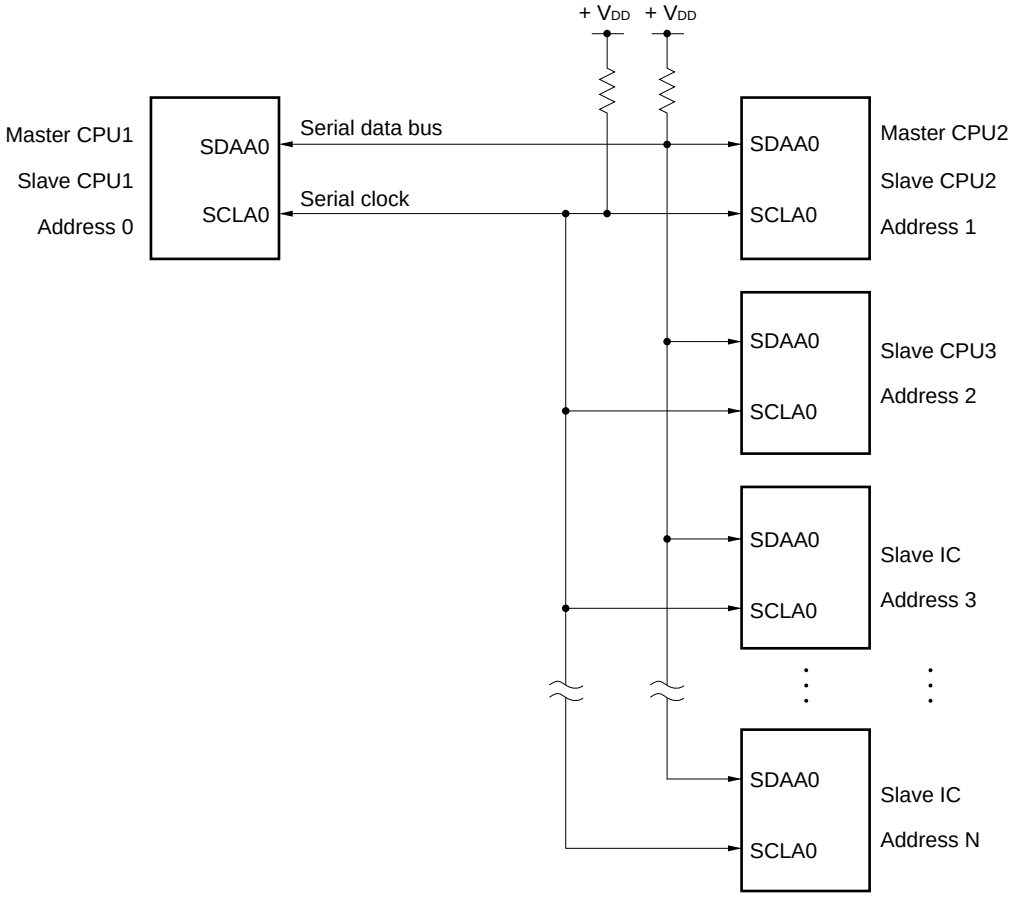
Table 14-6. Set Data of Baud Rate Generator

Baud Rate [bps]	f_{PRS} = 2.0 MHz				f_{PRS} = 5.0 MHz				f_{PRS} = 10.0 MHz				f_{PRS} = 20.0 MHz (when using PLL)			
	TPS63-TPS60	k	Calculated Value	ERR [%]	TPS63-TPS60	k	Calculated Value	ERR [%]	TPS63-TPS60	k	Calculated Value	ERR [%]	TPS63-TPS60	k	Calculated Value	ERR [%]
300	8H	13	301	0.16	7H	65	301	0.16	8H	65	301	0.16	9H	65	301	0.16
600	7H	13	601	0.16	6H	65	601	0.16	7H	65	601	0.16	8H	65	601	0.16
1200	6H	13	1202	0.16	5H	65	1202	0.16	6H	65	1202	0.16	7H	65	1202	0.16
2400	5H	13	2404	0.16	4H	65	2404	0.16	5H	65	2404	0.16	6H	65	2404	0.16
4800	4H	13	4808	0.16	3H	65	4808	0.16	4H	65	4808	0.16	5H	65	4808	0.16
9600	3H	13	9615	0.16	2H	65	9615	0.16	3H	65	9615	0.16	4H	65	9615	0.16
19200	2H	13	19231	0.16	1H	65	19231	0.16	2H	65	19231	0.16	3H	65	19231	0.16
24000	1H	21	23810	−0.79	3H	13	24038	0.16	4H	13	24038	0.16	5H	13	24038	0.16
31250	1H	16	31250	0	4H	5	31250	0	5H	5	31250	0	6H	5	31250	0
38400	1H	13	38462	0.16	0H	65	38462	0.16	1H	65	38462	0.16	2H	65	38462	0.16
48000	0H	21	47619	−0.79	2H	13	48077	0.16	3H	13	48077	0.16	4H	13	48077	0.16
76800	0H	13	76923	0.16	0H	33	75758	−1.36	0H	65	76923	0.16	1H	65	76923	0.16
115200	0H	9	111111	−3.55	1H	11	113636	−1.36	0H	43	116279	0.94	0H	87	116279	−0.22
153600	−	−	−	−	1H	8	156250	1.73	0H	33	151515	−1.36	1H	33	151515	−1.36
312500	−	−	−	−	0H	8	312500	0	1H	8	312500	0	2H	8	312500	0
625000	−	−	−	−	0H	4	625000	0	1H	4	625000	0	2H	4	625000	0

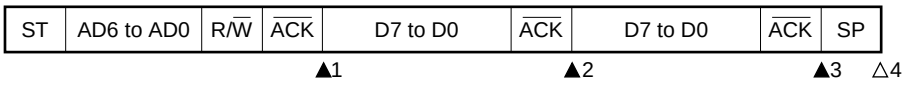
Remark TPS63 to TPS60: Bits 3 to 0 of clock selection register 6 (CKSR6) (setting of base clock (f_{XCLK6}))
k: Value set by MDL67 to MDL60 bits of baud rate generator control register 6 (BRGC6) (k = 4, 5, 6, ..., 255)
f_{PRS}: Peripheral hardware clock frequency
ERR: Baud rate error

Figure 15-2 shows a serial bus configuration example.

Figure 15-2. Serial Bus Configuration Example Using I^2C Bus



(ii) When WTIM0 = 1



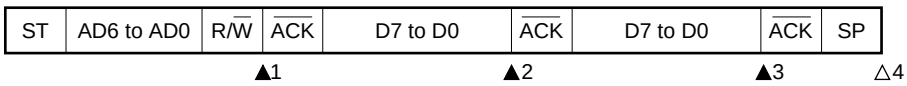
▲1 ▲2 ▲3 △4

▲1: IICAS0 = 0101×110B
▲2: IICAS0 = 0001×100B
▲3: IICAS0 = 0001××00B
△4: IICAS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

(b) When arbitration loss occurs during transmission of extension code

(i) When WTIM0 = 0



▲1 ▲2 ▲3 △4

▲1: IICAS0 = 0110×010B
▲2: IICAS0 = 0010×000B
▲3: IICAS0 = 0010×000B
△4: IICAS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

18.4 Interrupt Servicing Operations

18.4.1 Maskable interrupt acknowledgment

A maskable interrupt becomes acknowledgeable when the interrupt request flag is set to 1 and the mask (MK) flag corresponding to that interrupt request is cleared to 0. A vectored interrupt request is acknowledged if interrupts are in the interrupt enabled state (when the IE flag is set to 1). However, a low-priority interrupt request is not acknowledged during servicing of a higher priority interrupt request (when the ISP flag is reset to 0).

The times from generation of a maskable interrupt request until vectored interrupt servicing is performed are listed in Table 18-4 below.

For the interrupt request acknowledgment timing, refer to **Figures 18-15** and **18-16**.

Table 18-4. Time from Generation of Maskable Interrupt Request Until Servicing

	Minimum Time	Maximum Time[Note]
When ××PR = 0	7 clocks	32 clocks
When ××PR = 1	8 clocks	33 clocks

Note If an interrupt request is generated just before a divide instruction, the wait time becomes longer.

Remark 1 clock: $1/f_{CPU}$ (f_{CPU}: CPU clock)

If two or more maskable interrupt requests are generated simultaneously, the request with a higher priority level specified in the priority specification flag is acknowledged first. If two or more interrupts requests have the same priority level, the request with the highest default priority is acknowledged first.

An interrupt request that is held pending is acknowledged when it becomes acknowledgeable.

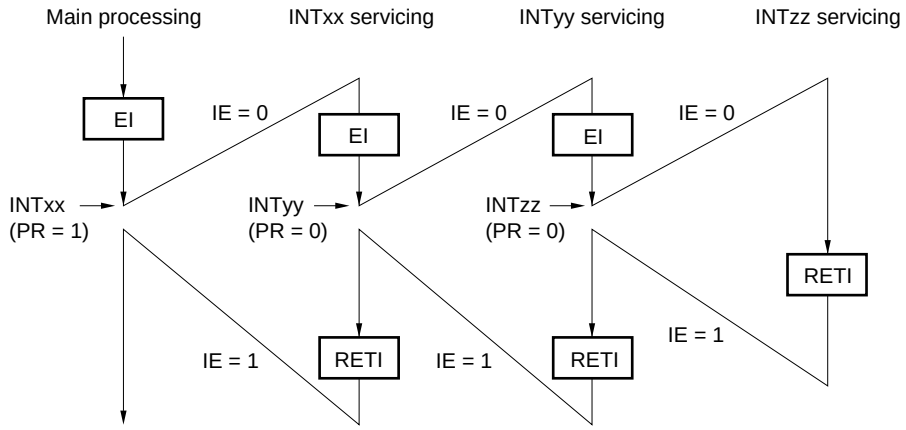
Figure 18-14 shows the interrupt request acknowledgment algorithm.

If a maskable interrupt request is acknowledged, the contents are saved into the stacks in the order of PSW, then PC, the IE flag is reset (0), and the contents of the priority specification flag corresponding to the acknowledged interrupt are transferred to the ISP flag. The vector table data determined for each interrupt request is the loaded into the PC and branched.

Restoring from an interrupt is possible by using the RETI instruction.

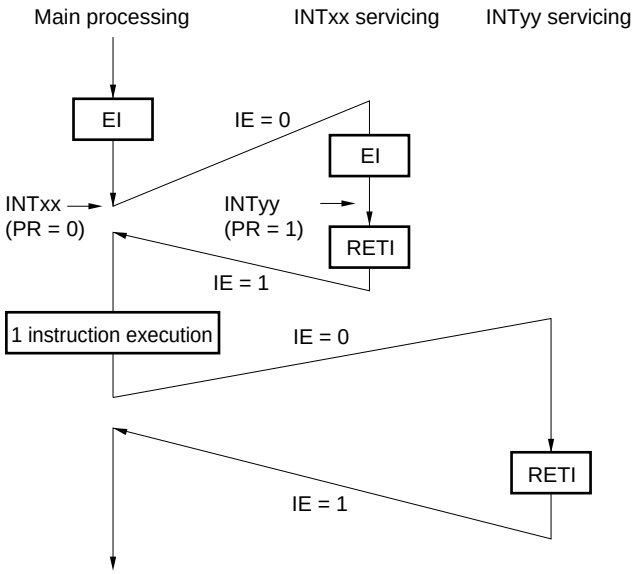
Figure 18-17. Examples of Multiple Interrupt Servicing (1/2)

Example 1. Multiple interrupt servicing occurs twice



During servicing of interrupt INTxx, two interrupt requests, INTyy and INTzz, are acknowledged, and multiple interrupt servicing takes place. Before each interrupt request is acknowledged, the EI instruction must always be issued to enable interrupt request acknowledgment.

Example 2. Multiple interrupt servicing does not occur due to priority control

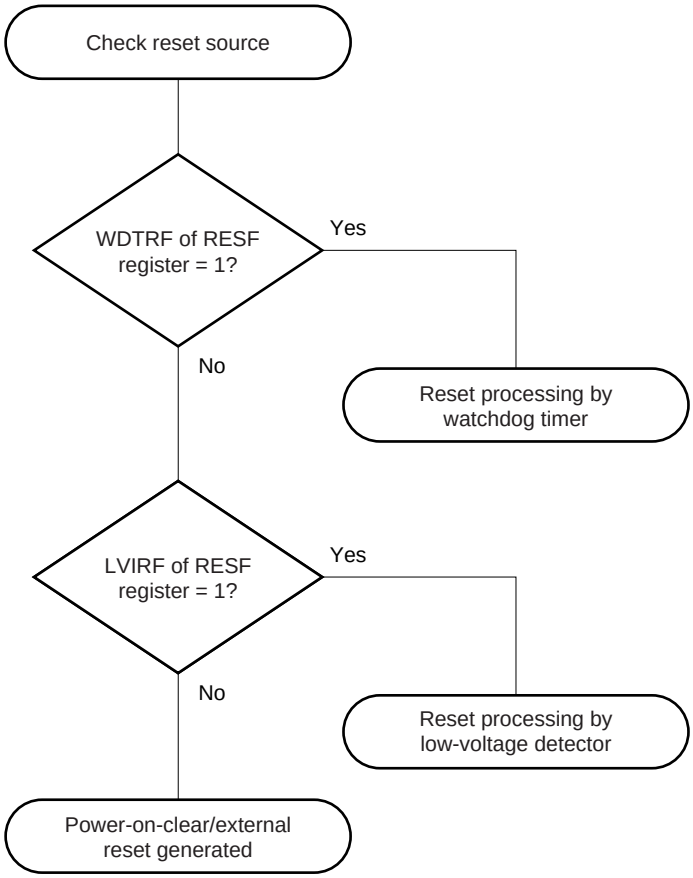


Interrupt request INTyy issued during servicing of interrupt INTxx is not acknowledged because its priority is lower than that of INTxx, and multiple interrupt servicing does not take place. The INTyy interrupt request is held pending, and is acknowledged following execution of one main processing instruction.

PR = 0: Higher priority level
PR = 1: Lower priority level
IE = 0: Interrupt request acknowledgment disabled

Figure 21-3. Example of Software Processing After Reset Release (2/2)

• Checking reset source

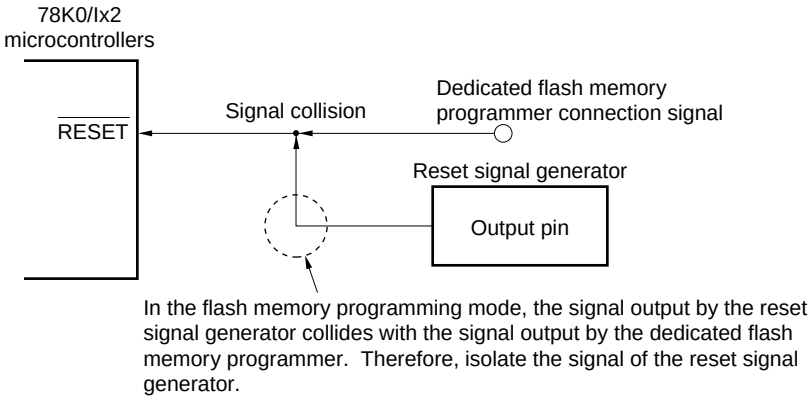


25.4.2 $\overline{\text{RESET}}$ pin

If the reset signal of the dedicated flash memory programmer is connected to the $\overline{\text{RESET}}$ pin that is connected to the reset signal generator on the board, signal collision takes place. To prevent this collision, isolate the connection with the reset signal generator.

If the reset signal is input from the user system while the flash memory programming mode is set, the flash memory will not be correctly programmed. Do not input any signal other than the reset signal of the dedicated flash memory programmer.

Figure 25-4. Signal Collision ($\overline{\text{RESET}}$ Pin)



25.4.3 Port pins

When the flash memory programming mode is set, all the pins not used for flash memory programming enter the same status as that immediately after reset. If external devices connected to the ports do not recognize the port status immediately after reset, the port pin must be connected to V_{DD} or V_{SS} via a resistor.

25.4.4 REGC pin

Connect the REGC pin to V_{DD} via a capacitor (0.47 to 1 μF) in the same manner as during normal operation. However, when using the STOP mode that has been entered since operation of the internal high-speed oscillation clock and external main system clock, 0.47 μF is recommended. Also, use a capacitor with good characteristics, since it is used to stabilize internal voltage.

25.4.5 Other signal pins

Connect X1 and X2 in the same status as in the normal operation mode.

Remark In the flash memory programming mode, the internal high-speed oscillation clock (f_{IH}) is used.

25.4.6 Power supply

To use the supply voltage output of the flash memory programmer, connect the V_{DD} pin to V_{DD} of the flash memory programmer, and the V_{SS} pin to GND of the flash memory programmer.

To use the on-board supply voltage, connect in compliance with the normal operation mode.

However, be sure to connect the V_{DD} and V_{SS} pins to V_{DD} and GND of the flash memory programmer to use the power monitor function with the flash memory programmer, even when using the on-board supply voltage.

Supply the same other power supplies (AV_{REF} and AV_{SS}) as those in the normal operation mode.

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag
				Note 1	Note 2		Z AC CY
8-bit operation	**OR**	A, #byte	2	4	–	A ← A ∨ byte	×
		saddr, #byte	3	6	8	(saddr) ← (saddr) ∨ byte	×
		A, r Note 3	2	4	–	A ← A ∨ r	×
		r, A	2	4	–	r ← r ∨ A	×
		A, saddr	2	4	5	A ← A ∨ (saddr)	×
		A, !addr16	3	8	9	A ← A ∨ (addr16)	×
		A, [HL]	1	4	5	A ← A ∨ (HL)	×
		A, [HL + byte]	2	8	9	A ← A ∨ (HL + byte)	×
		A, [HL + B]	2	8	9	A ← A ∨ (HL + B)	×
		A, [HL + C]	2	8	9	A ← A ∨ (HL + C)	×
	XOR	A, #byte	2	4	–	A ← A ⊻ byte	×
		saddr, #byte	3	6	8	(saddr) ← (saddr) ⊻ byte	×
		A, r Note 3	2	4	–	A ← A ⊻ r	×
		r, A	2	4	–	r ← r ⊻ A	×
		A, saddr	2	4	5	A ← A ⊻ (saddr)	×
		A, !addr16	3	8	9	A ← A ⊻ (addr16)	×
		A, [HL]	1	4	5	A ← A ⊻ (HL)	×
		A, [HL + byte]	2	8	9	A ← A ⊻ (HL + byte)	×
		A, [HL + B]	2	8	9	A ← A ⊻ (HL + B)	×
		A, [HL + C]	2	8	9	A ← A ⊻ (HL + C)	×
	CMP	A, #byte	2	4	–	A – byte	× × ×
		saddr, #byte	3	6	8	(saddr) – byte	× × ×
		A, r Note 3	2	4	–	A – r	× × ×
		r, A	2	4	–	r – A	× × ×
		A, saddr	2	4	5	A – (saddr)	× × ×
		A, !addr16	3	8	9	A – (addr16)	× × ×
		A, [HL]	1	4	5	A – (HL)	× × ×
		A, [HL + byte]	2	8	9	A – (HL + byte)	× × ×
		A, [HL + B]	2	8	9	A – (HL + B)	× × ×
		A, [HL + C]	2	8	9	A – (HL + C)	× × ×

Notes 1. When the internal high-speed RAM area is accessed or for an instruction with no data access

2. When an area except the internal high-speed RAM area is accessed

3. Except “r = A”

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

2. This clock cycle applies to the internal ROM program.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(T_A = –40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P37, P121, P122, P125		0.7V_{DD}		V_{DD}	V
	V_{IH2}	P20 to P27, P70	AV_{REF} = V_{DD}	0.7AV_{REF}		AV_{REF}	V
	V_{IH3}	P60, P61 (I/O port mode)		0.7V_{DD}		V_{DD}	V
	V_{IH4}	P00 to P02, P30 to P36, $\overline{\text{RESET}}$, EXCLK		0.8V_{DD}		V_{DD}	V
	V_{IH5}	P60, P61 (SMBus input mode)	3.4 V ≤ V_{DD} ≤ 5.5 V	0.8V_{DD}			V
			2.7 V ≤ V_{DD} < 3.4 V	2.1			V
	V_{IH6}	X1, X2		V_{DD} – 0.1		V_{DD}	V
Input voltage, low	V_{IL1}	P37, P121, P122, P125		0		0.3V_{DD}	V
	V_{IL2}	P20 to P27, P70	AV_{REF} = V_{DD}	0		0.3AV_{REF}	V
	V_{IL3}	P60, P61 (I/O port mode)		0		0.3V_{DD}	V
	V_{IL4}	P00 to P02, P30 to P36, $\overline{\text{RESET}}$, EXCLK		0		0.2V_{DD}	V
	V_{IL5}	P60, P61 (SMBus input mode)	3.4 V ≤ V_{DD} ≤ 5.5 V	0		0.2V_{DD}	V
			2.7 V ≤ V_{DD} < 3.4 V	0		0.8	V
	V_{IL6}	X1, X2		0		0.1	V
Output voltage, high	V_{OH1}	P00 to P02, P30 to P37, P60, P61	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = –3.0 mA	V_{DD} – 0.7			V
			2.7 V ≤ V_{DD} < 4.0 V, I_{OH1} = –2.5 mA	V_{DD} – 0.5			V
	V_{OH2}	P20 to P27, P70	AV_{REF} = V_{DD}, I_{OH2} = –100 μA	V_{DD} – 0.5			V

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Caution For P122/EXCLK, the value of V_{IH} and V_{IL} differs according to the input port mode or external clock mode.
Make sure to satisfy the DC characteristics of EXCLK in external clock input mode.

(5/7)

Edition	Description	Chapter
3rd Edition	Modification of **(4) 0083H/1083H** in **24.1 Functions of Option Bytes**	**CHAPTER 24 OPTION BYTE**
	Modification of **Figure 24-1. Format of Option Byte (3/3)**	
	Modification of **Figure 25-2 Environment for Writing Program to Flash Memory**	**CHAPTER 25 FLASH MEMORY**
	Modification of **Table 25-2 Pin Connection**	
	Modification of **25.4.1 TOOL pins**	
	Addition of **25.4.7 On-board writing when connecting crystal/ceramic resonator**	
	Modification of **25.5.2 Flash memory programming mode**	
	Addition of **25.7 Processing Time for Each Command When PG-FP5 Is Used (Reference)**	
	Modification of **Cautions 2** to **4** and **Remark** in **25.8 Flash Memory Programming by Self Programming**	
	Addition of **25.8.1 Register controlling self programming mode** and **25.8.2 Flow of self programming (Rewriting Flash Memory)**	
	Modification of **Caution** in **25.8.3 Boot swap function**	
	Addition of **25.9 Creating ROM Code to Place Order for Previously Written Product**	
	Addition of **Caution 2** to **26.1 Connecting QB-MINI2 to 78K0/Ix2 Microcontrollers**	**CHAPTER 26 ON-CHIP DEBUG FUNCTION**
	Modification of **Figure 26-1 Connection Example of QB-MINI2 and 78K0/Ix2 Microcontrollers**	
	Modification of **26.2 On-Chip Debug Security ID**	
	Addition of **26.3 Securing of User Resources**	
	Revision of chapter	**CHAPTER 28 ELECTRICAL SPECIFICATIONS**
	Modification of **Table 30-1 Surface Mounting Type Soldering Conditions**	**CHAPTER 30 RECOMMENDED SOLDERING CONDITIONS**
	Modification of **Table 31-1. Registers That Generate Wait and Number of CPU Wait Clocks (2/2)**	**CHAPTER 31 CAUTIONS FOR WAIT**
	Modification of **Notes 3** and **4** in **Figure A-1 Development Tool Configuration (1/2)**	**APPENDIX A DEVELOPMENT TOOLS**
	Modification of **Note 5** in **Figure A-1 Development Tool Configuration (2/2)**	
	Addition of **Note 1** to **A.3.1 When using flash memory programmer PG-FP5 and FL-PR5**	
	Addition of the product name of system simulator to **A.5 Debugging Tools (Software)**	
	Addition of chapter	**APPENDIX B REGISTER INDEX**
	Addition of **C.2 Revision History of Preceding Editions**	**APPENDIX C REVISION HISTORY**
4th Edition	Addition of 32-pin products to 78K0/IB2	**Throughout**
	Change URL of Renesas Electronics website	
	Deletion of "(To be prepared)" and change of document no. of related documents	**How to Use This Manual**
	Addition of 20-pin plastic SOP (7.62 mm (300)) and 32-pin plastic WQFN (fine pitch) (5 x 5) to **1.2 Ordering Information**	**CHAPTER 1 OUTLINE**
	Addition of 20-pin plastic SOP (7.62 mm (300)) and 32-pin plastic WQFN (fine pitch) (5 x 5) to **1.3 Pin Configuration (Top View)**	
	Change of Port 12 of 30-pin plastic SSOP (7.62 mm (300))	

78K0/Ix2

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