



Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

| | |
|----------------------------|---|
| Product Status | Active |
| Core Processor | Coldfire V1 |
| Core Size | 32-Bit Single-Core |
| Speed | 50MHz |
| Connectivity | I ² C, SCI, SPI |
| Peripherals | LVD, PWM, WDT |
| Number of I/O | 36 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | A/D 9x12b |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-LQFP |
| Supplier Device Package | 44-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf51ac128ccfger |

1 MCF51AC256 Family Configurations

1.1 Device Comparison

The MCF51AC256 series is summarized in Table 1.

Table 1. MCF51AC256 Series Device Comparison

| Feature | MCF51AC256A | | MCF51AC256B | | | MCF51AC128A | | MCF51AC128C | | |
|---|-------------|--------|-------------|--------|--------|-----------------------|--------|-------------|--------|--------|
| | 80-pin | 64-pin | 80-pin | 64-pin | 44-pin | 80-pin | 64-pin | 80-pin | 64-pin | 44-pin |
| Flash memory size (Kbytes) | 256 | | | | | 128 | | | | |
| RAM size (Kbytes) | 32 | | | | | 32 or 16 ¹ | | | | |
| V1 ColdFire core with BDM (background debug module) | Yes | | | | | | | | | |
| ACMP1 (analog comparator) | Yes | | | | | | | | | |
| ACMP2 (analog comparator) | Yes | | Yes | | No | Yes | | | | No |
| ADC (analog-to-digital converter) channels (12-bit) | 24 | 20 | 24 | 20 | 9 | 24 | 20 | 24 | 20 | 9 |
| CAN (controller area network) | Yes | | No | | | Yes | | No | | |
| COP (computer operating properly) | Yes | | | | | | | | | |
| CRC (cyclic redundancy check) | Yes | | | | | | | | | |
| RTI | Yes | | | | | | | | | |
| DBG (debug) | Yes | | | | | | | | | |
| IIC1 (inter-integrated circuit) | Yes | | | | | | | | | |
| IRQ (interrupt request input) | Yes | | | | | | | | | |
| INTC (interrupt controller) | Yes | | | | | | | | | |
| KBI (keyboard interrupts) | Yes | | | | | | | | | |
| LVD (low-voltage detector) | Yes | | | | | | | | | |
| MCG (multipurpose clock generator) | Yes | | | | | | | | | |
| OSC (crystal oscillator) | Yes | | | | | | | | | |
| Port I/O ² | 69 | 54 | 69 | 54 | 36 | 69 | 54 | 69 | 54 | 36 |
| RGPIO (rapid general-purpose I/O) | 16 | | | | 12 | 16 | | | | 12 |
| SCI1, SCI2 (serial communications interfaces) | Yes | | | | | | | | | |
| SPI1 (serial peripheral interface) | Yes | | | | | | | | | |
| SPI2 (serial peripheral interface) | Yes | No | Yes | No | | Yes | No | Yes | No | |
| FTM1 (flexible timer module) channels | 6 | | | | 4 | 6 | | | | 4 |
| FTM2 channels | 6 | 2 | 6 | 2 | 2 | 6 | 2 | 6 | 2 | 2 |

Table 1. MCF51AC256 Series Device Comparison (continued)

| Feature | MCF51AC256A | | MCF51AC256B | | | MCF51AC128A | | MCF51AC128C | | |
|---|-------------|--------|-------------|--------|--------|-------------|--------|-------------|--------|--------|
| | 80-pin | 64-pin | 80-pin | 64-pin | 44-pin | 80-pin | 64-pin | 80-pin | 64-pin | 44-pin |
| TPM3 (timer pulse-width modulator) channels | 2 | | | | | | | | | |
| VBUS (debug visibility bus) | Yes | No | Yes | No | | Yes | No | Yes | No | |

¹ The members of MCF51AC128A with CAN support have 32 KB RAM. The other members have 16 KB RAM.

² Up to 16 pins on Ports E and F are shared with the ColdFire Rapid GPIO module.

1.2 Block Diagram

Figure 1 shows the connections between the MCF51AC256 series pins and modules.

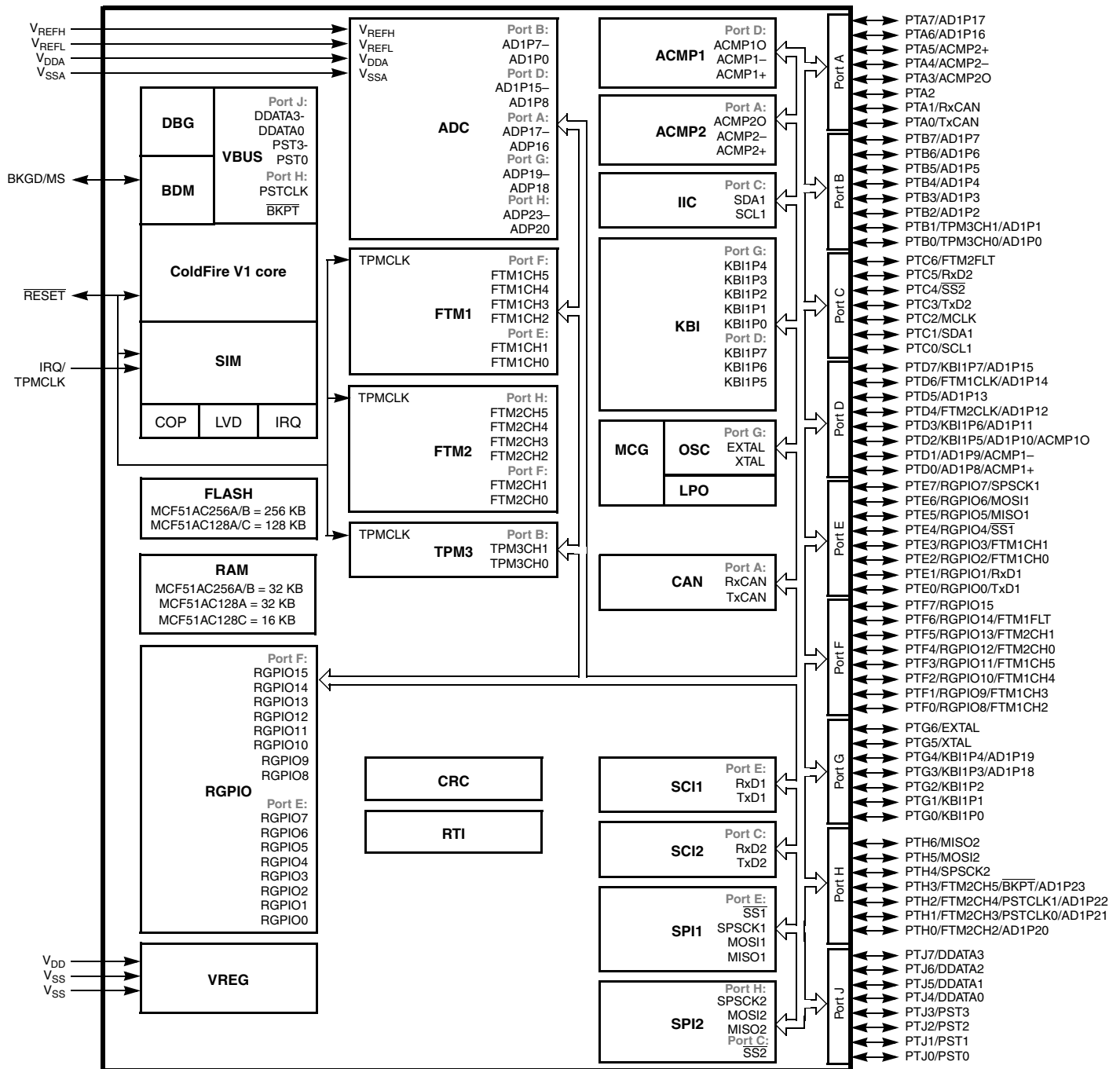


Figure 1. MCF51AC256 Series Block Diagram

1.3 Features

Table 2 describes the functional units of the MCF51AC256 series.

Table 2. MCF51AC256 Series Functional Units

| Functional Unit | Function |
|--|--|
| CF1 Core (V1 ColdFire core) | Executes programs and interrupt handlers |
| BDM (background debug module) | Provides single pin debugging interface (part of the V1 ColdFire core) |
| DBG (debug) | Provides debugging and emulation capabilities (part of the V1 ColdFire core) |
| VBUS (debug visibility bus) | Allows for real-time program traces (part of the V1 ColdFire core) |
| SIM (system integration module) | Controls resets and chip level interfaces between modules |
| Flash (flash memory) | Provides storage for program code, constants and variables |
| RAM (random-access memory) | Provides storage for program variables |
| RGPIO (rapid general-purpose input/output) | Allows for I/O port access at CPU clock speeds |
| VREG (voltage regulator) | Controls power management across the device |
| COP (computer operating properly) | Monitors a countdown timer and generates a reset if the timer is not regularly reset by the software |
| LVD (low-voltage detect) | Monitors internal and external supply voltage levels, and generates a reset or interrupt when the voltages are too low |
| CF1_INTIC (interrupt controller) | Controls and prioritizes all device interrupts |
| ADC (analog-to-digital converter) | Measures analog voltages at up to 12 bits of resolution |
| FTM1, FTM2 (flexible timer/pulse-width modulators) | Provides a variety of timing-based features |
| TPM3 (timer/pulse-width modulator) | Provides a variety of timing-based features |
| CRC (cyclic redundancy check) | Accelerates computation of CRC values for ranges of memory |
| ACMP1, ACMP2 (analog comparators) | Compares two analog inputs |
| IIC (inter-integrated circuit) | Supports standard IIC communications protocol |
| KBI (keyboard interrupt) | Provides pin interrupt capabilities |
| MCG (multipurpose clock generator) | Provides clocking options for the device, including a phase-locked loop (PLL) and frequency-locked loop (FLL) for multiplying slower reference clock sources |
| OSC (crystal oscillator) | Allows a crystal or ceramic resonator to be used as the system clock source or reference clock for the PLL or FLL |
| LPO (low-power oscillator) | Provides a second clock source for COP and RTI. |
| CAN (controller area network) | Supports standard CAN communications protocol |
| SCI1, SCI2 (serial communications interfaces) | Serial communications UARTs capable of supporting RS-232 and LIN protocols |
| SPI1 (8-bit serial peripheral interfaces) | Provides 8-bit 4-pin synchronous serial interface |
| SPI2 (16-bit serial peripheral interfaces) | Provides 16-bit 4-pin synchronous serial interface with FIFO |

MCF51AC256 Family Configurations

- Double-buffered transmit and receive
- Serial clock phase and polarity options
- Slave select output
- Selectable MSB-first or LSB-first shifting
- 16-bit and FIFO operations in SPI2
- Input/Output
 - 69 GPIOs
 - 8 keyboard interrupt pins with selectable polarity
 - Hysteresis and configurable pull-up device on all input pins; Configurable slew rate and drive strength on all output pins
 - 16-bits Rapid GPIO pins connected to the processor's local 32-bit platform bus with set, clear, and faster toggle functionality

1.4 Part Numbers

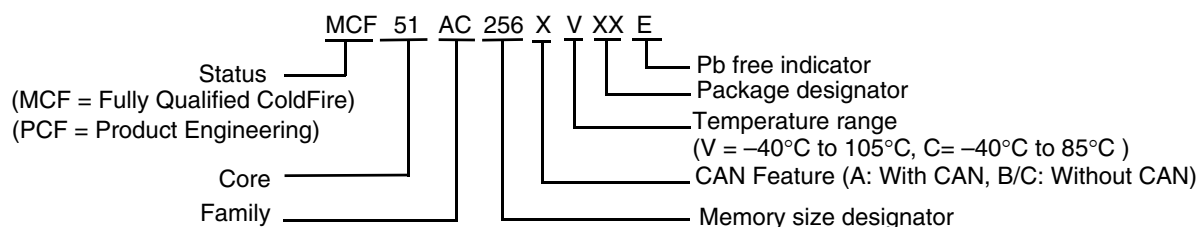


Table 3. Orderable Part Number Summary

| Freescall Part Number | Description | Flash / SRAM (Kbytes) | Package | Temperature |
|-----------------------|---|-----------------------|---------|----------------|
| MCF51AC256AVFUE | MCF51AC256 ColdFire Microcontroller with CAN | 256 / 32 | 64 QFP | -40°C to 105°C |
| MCF51AC256BVFUE | MCF51AC256 ColdFire Microcontroller without CAN | 256 / 32 | 64 QFP | -40°C to 105°C |
| MCF51AC256AVLKE | MCF51AC256 ColdFire Microcontroller with CAN | 256 / 32 | 80 LQFP | -40°C to 105°C |
| MCF51AC256BVLKE | MCF51AC256 ColdFire Microcontroller without CAN | 256 / 32 | 80 LQFP | -40°C to 105°C |
| MCF51AC256AVPUE | MCF51AC256 ColdFire Microcontroller with CAN | 256 / 32 | 64 LQFP | -40°C to 105°C |
| MCF51AC256BVPUE | MCF51AC256 ColdFire Microcontroller without CAN | 256 / 32 | 64 LQFP | -40°C to 105°C |
| MCF51AC128AVFUE | MCF51AC128 ColdFire Microcontroller with CAN | 128 / 32 | 64 QFP | -40°C to 105°C |
| MCF51AC128CVFUE | MCF51AC128 ColdFire Microcontroller without CAN | 128 / 16 | 64 QFP | -40°C to 105°C |
| MCF51AC128AVLKE | MCF51AC128 ColdFire Microcontroller with CAN | 128 / 32 | 80 LQFP | -40°C to 105°C |
| MCF51AC128CVLKE | MCF51AC128 ColdFire Microcontroller without CAN | 128 / 16 | 80 LQFP | -40°C to 105°C |
| MCF51AC128AVPUE | MCF51AC128 ColdFire Microcontroller with CAN | 128 / 32 | 64 LQFP | -40°C to 105°C |
| MCF51AC128CVPUE | MCF51AC128 ColdFire Microcontroller without CAN | 128 / 16 | 64 LQFP | -40°C to 105°C |
| MCF51AC256ACFUE | MCF51AC256 ColdFire Microcontroller with CAN | 256 / 32 | 64 QFP | -40°C to 85°C |
| MCF51AC256BCFUE | MCF51AC256 ColdFire Microcontroller without CAN | 256 / 32 | 64 QFP | -40°C to 85°C |
| MCF51AC256ACLKE | MCF51AC256 ColdFire Microcontroller with CAN | 256 / 32 | 80 LQFP | -40°C to 85°C |
| MCF51AC256BCLKE | MCF51AC256 ColdFire Microcontroller without CAN | 256 / 32 | 80 LQFP | -40°C to 85°C |

Table 3. Orderable Part Number Summary

| | | | | |
|-----------------|---|----------|---------|---------------|
| MCF51AC256ACPUE | MCF51AC256 ColdFire Microcontroller with CAN | 256 / 32 | 64 LQFP | –40°C to 85°C |
| MCF51AC256BCPUE | MCF51AC256 ColdFire Microcontroller without CAN | 256 / 32 | 64 LQFP | –40°C to 85°C |
| MCF51AC256BCFGE | MCF51AC256 ColdFire Microcontroller without CAN | 256/32 | 44 LQFP | –40°C to 85°C |
| MCF51AC128ACFUE | MCF51AC128 ColdFire Microcontroller with CAN | 128 / 32 | 64 QFP | –40°C to 85°C |
| MCF51AC128CCFUE | MCF51AC128 ColdFire Microcontroller without CAN | 128 / 16 | 64 QFP | –40°C to 85°C |
| MCF51AC128ACLKE | MCF51AC128 ColdFire Microcontroller with CAN | 128 / 32 | 80 LQFP | –40°C to 85°C |
| MCF51AC128CCLKE | MCF51AC128 ColdFire Microcontroller without CAN | 128 / 16 | 80 LQFP | –40°C to 85°C |
| MCF51AC128ACPUE | MCF51AC128 ColdFire Microcontroller with CAN | 128 / 32 | 64 LQFP | –40°C to 85°C |
| MCF51AC128CCPUE | MCF51AC128 ColdFire Microcontroller without CAN | 128 / 16 | 64 LQFP | –40°C to 85°C |
| MCF51AC128CCFGE | MCF51AC128 ColdFire Microcontroller without CAN | 128 / 16 | 44 LQFP | –40°C to 85°C |

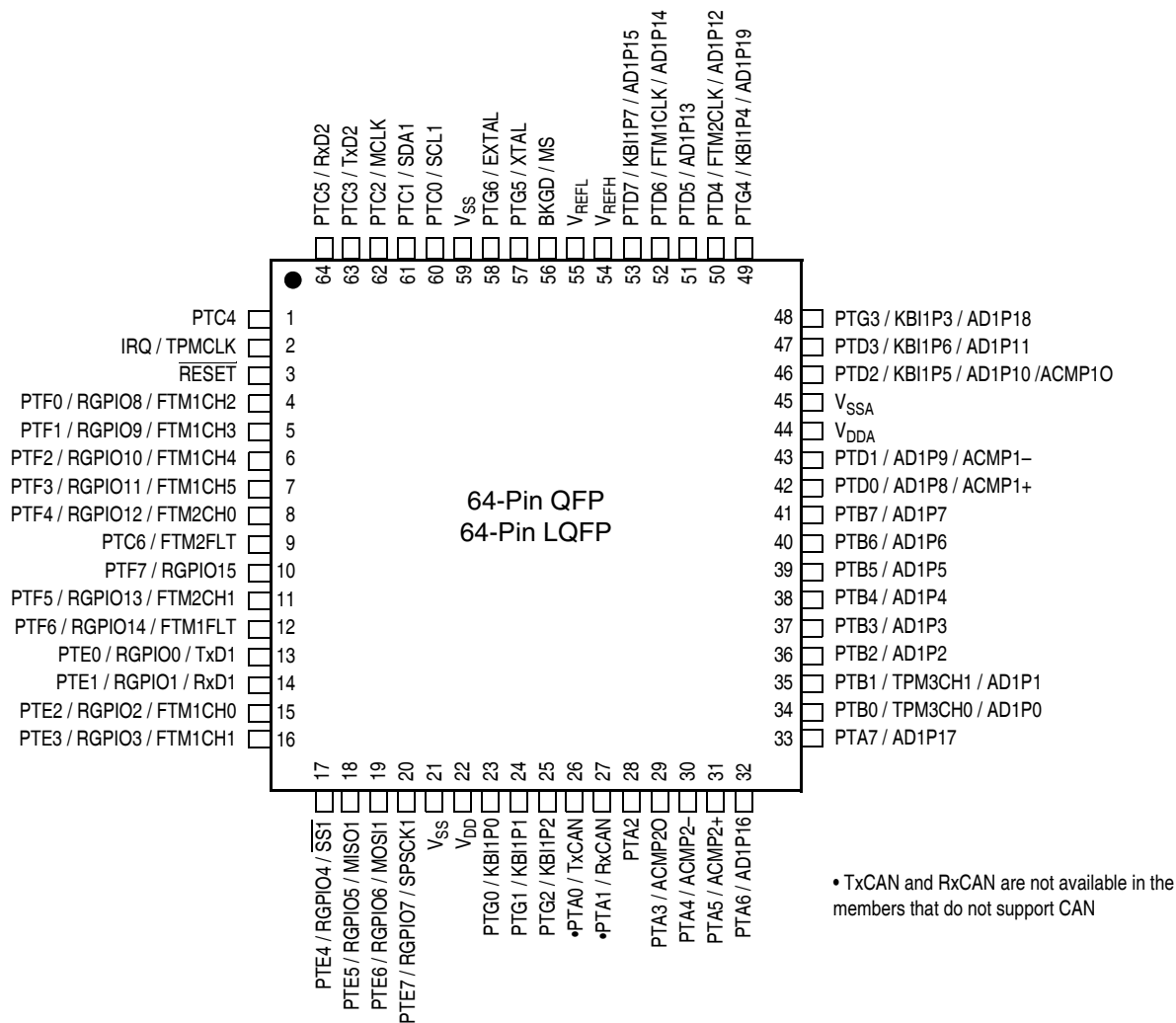
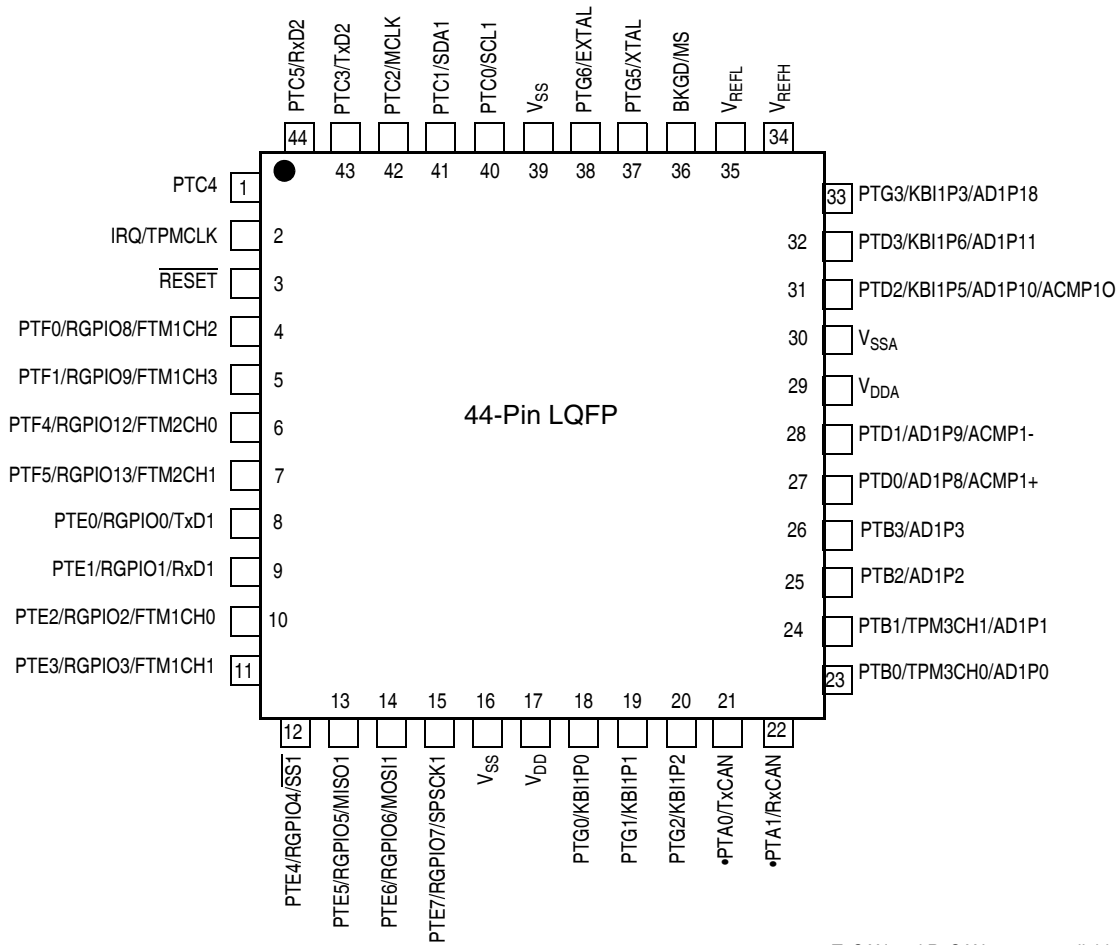


Figure 3. MCF51AC256 Series ColdFire Microcontroller 64-Pin QFP/LQFP

Figure 4 shows the pinout of the 44-pin LQFP.



• TxCAN and RxCAN are not available in the members that do not support CAN

Figure 4. MCF51AC256 Series ColdFire Microcontroller 44-Pin LQFP

Table 4 shows the package pin assignments.

Table 4. Pin Availability by Package Pin-Count

| Pin Number | | | Lowest <-- Priority --> Highest | | | |
|------------|----|----|---------------------------------|---------------------|---------|-------|
| 80 | 64 | 44 | Port Pin | Alt 1 | Alt 2 | Alt 3 |
| 1 | 1 | 1 | PTC4 | SS2 | | |
| 2 | 2 | 2 | IRQ | TPMCLK ¹ | | |
| 3 | 3 | 3 | RESET | | | |
| 4 | 4 | 4 | PTF0 | RGPIO8 | FTM1CH2 | |
| 5 | 5 | 5 | PTF1 | RGPIO9 | FTM1CH3 | |
| 6 | 6 | — | PTF2 | RGPIO10 | FTM1CH4 | |
| 7 | 7 | — | PTF3 | RGPIO11 | FTM1CH5 | |

Table 4. Pin Availability by Package Pin-Count (continued)

| Pin Number | | | Lowest <-- Priority --> Highest | | | |
|------------|----|----|---------------------------------|--------------------|---------|--------|
| 80 | 64 | 44 | Port Pin | Alt 1 | Alt 2 | Alt 3 |
| 8 | 8 | 6 | PTF4 | RGPIO12 | FTM2CH0 | |
| 9 | 9 | — | PTC6 | FTM2FLT | | |
| 10 | 10 | — | PTF7 | RGPIO15 | | |
| 11 | 11 | 7 | PTF5 | RGPIO13 | FTM2CH1 | |
| 12 | 12 | — | PTF6 | RGPIO14 | FTM1FLT | |
| 13 | — | — | PTJ0 | PST0 | | |
| 14 | — | — | PTJ1 | PST1 | | |
| 15 | — | — | PTJ2 | PST2 | | |
| 16 | — | — | PTJ3 | PST3 | | |
| 17 | 13 | 8 | PTE0 | RGPIO0 | TxD1 | |
| 18 | 14 | 9 | PTE1 | RGPIO1 | RxD1 | |
| 19 | 15 | 10 | PTE2 | RGPIO2 | FTM1CH0 | |
| 20 | 16 | 11 | PTE3 | RGPIO3 | FTM1CH1 | |
| 21 | 17 | 12 | PTE4 | RGPIO4 | SS1 | |
| 22 | 18 | 13 | PTE5 | RGPIO5 | MISO1 | |
| 23 | 19 | 14 | PTE6 | RGPIO6 | MOSI1 | |
| 24 | 20 | 15 | PTE7 | RGPIO7 | SPSCK1 | |
| 25 | 21 | 16 | V _{SS} | | | |
| 26 | 22 | 17 | V _{DD} | | | |
| 27 | — | — | PTJ4 | DDATA0 | | |
| 28 | — | — | PTJ5 | DDATA1 | | |
| 29 | — | — | PTJ6 | DDATA2 | | |
| 30 | — | — | PTJ7 | DDATA3 | | |
| 31 | 23 | 18 | PTG0 | KBI1P0 | | |
| 32 | 24 | 19 | PTG1 | KBI1P1 | | |
| 33 | 25 | 20 | PTG2 | KBI1P2 | | |
| 34 | 26 | 21 | PTA0 | TxCAN ² | | |
| 35 | 27 | 22 | PTA1 | RxCAN ³ | | |
| 36 | 28 | — | PTA2 | | | |
| 37 | 29 | — | PTA3 | ACMP20 | | |
| 38 | 30 | — | PTA4 | ACMP2– | | |
| 39 | 31 | — | PTA5 | ACMP2+ | | |
| 40 | 32 | — | PTA6 | AD1P16 | | |
| 41 | 33 | — | PTA7 | AD1P17 | | |
| 42 | — | — | PTH0 | FTM2CH2 | AD1P20 | |
| 43 | — | — | PTH1 | FTM2CH3 | PSTCLK0 | AD1P21 |
| 44 | — | — | PTH2 | FTM2CH4 | PSTCLK1 | AD1P22 |
| 45 | — | — | PTH3 | FTM2CH5 | BKPT | AD1P23 |
| 46 | 34 | 23 | PTB0 | TPM3CH0 | AD1P0 | |
| 47 | 35 | 24 | PTB1 | TPM3CH1 | AD1P1 | |
| 48 | 36 | 25 | PTB2 | AD1P2 | | |

- ¹ Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance
- ² Junction to Ambient Natural Convection
- ³ 1s — Single layer board, one signal layer
- ⁴ 2s2p — Four layer board, 2 signal and 2 power layers

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \text{Eqn. 1}$$

where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power

$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} \ll P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273^\circ\text{C}) \quad \text{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273^\circ\text{C}) + \theta_{JA} \times (P_D)^2 \quad \text{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A . Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A .

2.4 Electrostatic Discharge (ESD) Protection Characteristics

Although damage from static discharge is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with CDF-AEC-Q00 Stress Test Qualification for Automotive Grade Integrated Circuits. (<http://www.aecouncil.com/>) This device was qualified to AEC-Q100 Rev E.

A device is considered to have failed if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete dc parametric and functional testing is performed per the

Table 10. DC Characteristics (continued)

| Num | C | Parameter | Symbol | Min | Typical ¹ | Max | Unit |
|-----|---|---|-------------------|------------------------|----------------------|--------------------------|------|
| 3 | P | Output low voltage — Low Drive (PTxDSn = 0) 5 V, I _{Load} = 4 mA 3 V, I _{Load} = 2 mA 5 V, I _{Load} = 2 mA 3 V, I _{Load} = 1 mA | V _{OL} | — | — | 1.5 1.5 0.8 0.8 | V |
| | | Output low voltage — High Drive (PTxDSn = 1) 5 V, I _{Load} = 15 mA 3 V, I _{Load} = 8 mA 5 V, I _{Load} = 8 mA 3 V, I _{Load} = 4 mA | | — | — | 1.5 1.5 0.8 0.8 | |
| 4 | C | Output high current — Max total I _{OH} for all ports 5V 3V | I _{OHT} | — | — | 100 60 | mA |
| 5 | C | Output low current — Max total I _{OL} for all ports 5 V 3 V | I _{OLT} | — | — | 100 60 | mA |
| 6 | P | Input high voltage; all digital inputs | V _{IH} | 0.65 × V _{DD} | — | — | V |
| 7 | P | Input low voltage; all digital inputs | V _{IL} | — | — | 0.35 × V _{DD} | V |
| 8 | D | Input hysteresis; all digital inputs | V _{hys} | 0.06 × V _{DD} | — | — | mV |
| 9 | P | Input leakage current; input only pins ² | I _{in} | — | 0.1 | 1 | μA |
| 10 | P | High impedance (off-state) leakage current ² | I _{OZ} | — | 0.1 | 1 | μA |
| 11 | P | Internal pullup resistors ³ | R _{PU} | 20 | 45 | 65 | kΩ |
| 12 | P | Internal pulldown resistors ⁴ | R _{PD} | 20 | 45 | 65 | kΩ |
| 13 | C | Input capacitance; all non-supply pins | C _{In} | — | — | 8 | pF |
| 14 | P | POR rearm voltage | V _{POR} | 0.9 | 1.4 | 2.0 | V |
| 15 | D | POR rearm time | t _{POR} | 10 | — | — | μs |
| 16 | P | Low-voltage detection threshold — high range V _{DD} falling V _{DD} rising | V _{LVDH} | 4.2 4.27 | 4.35 4.4 | 4.5 4.6 | V |
| 17 | P | Low-voltage detection threshold — low range V _{DD} falling V _{DD} rising | V _{LVDL} | 2.48 2.5 | 2.68 2.7 | 2.7 2.72 | V |
| 18 | P | Low-voltage warning threshold — high range V _{DD} falling V _{DD} rising | V _{LVWH} | 4.2 4.27 | 4.4 4.45 | 4.5 4.6 | V |
| 19 | P | Low-voltage warning threshold low range V _{DD} falling V _{DD} rising | V _{LVWL} | 2.48 2.5 | 2.68 2.7 | 2.7 2.72 | V |
| 20 | T | Low-voltage inhibit reset/recover hysteresis 5 V 3 V | V _{hys} | — | 100 60 | — | mV |
| 21 | D | RAM retention voltage | V _{RAM} | — | 0.6 | 1.0 | V |

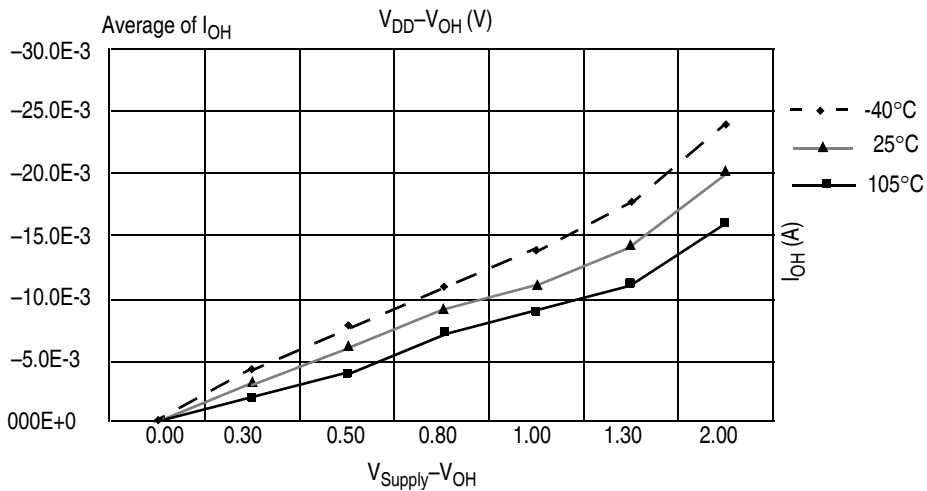


Figure 8. Typical I_{OH} vs. $V_{DD}-V_{OH}$ at $V_{DD} = 5\text{ V}$ (High Drive, $PTxDSn = 1$)

Figure 9. Typical Run I_{DD} vs. System Clock Freq. for FEI and FBE Modes

2.7 Analog Comparator (ACMP) Electricals

Table 12. Analog Comparator Electrical Specifications

| Num | C | Rating | Symbol | Min | Typical | Max | Unit |
|-----|---|---|-------------|----------------|---------|----------|---------|
| 1 | — | Supply voltage | V_{DD} | 2.7 | — | 5.5 | V |
| 2 | T | Supply current (active) | I_{DDAC} | — | 20 | 35 | μA |
| 3 | D | Analog input voltage | V_{AIN} | $V_{SS} - 0.3$ | — | V_{DD} | V |
| 4 | D | Analog input offset voltage | V_{AIO} | — | 20 | 40 | mV |
| 5 | D | Analog comparator hysteresis | V_H | 3.0 | 6.0 | 20.0 | mV |
| 6 | D | Analog input leakage current | I_{ALKG} | — | — | 1.0 | μA |
| 7 | D | Analog comparator initialization delay | t_{AINIT} | — | — | 1.0 | μs |
| 8 | P | Bandgap voltage reference factory trimmed at $V_{DD} = 5.3248$ V, Temp = 25 °C | V_{BG} | 1.18 | 1.20 | 1.21 | V |

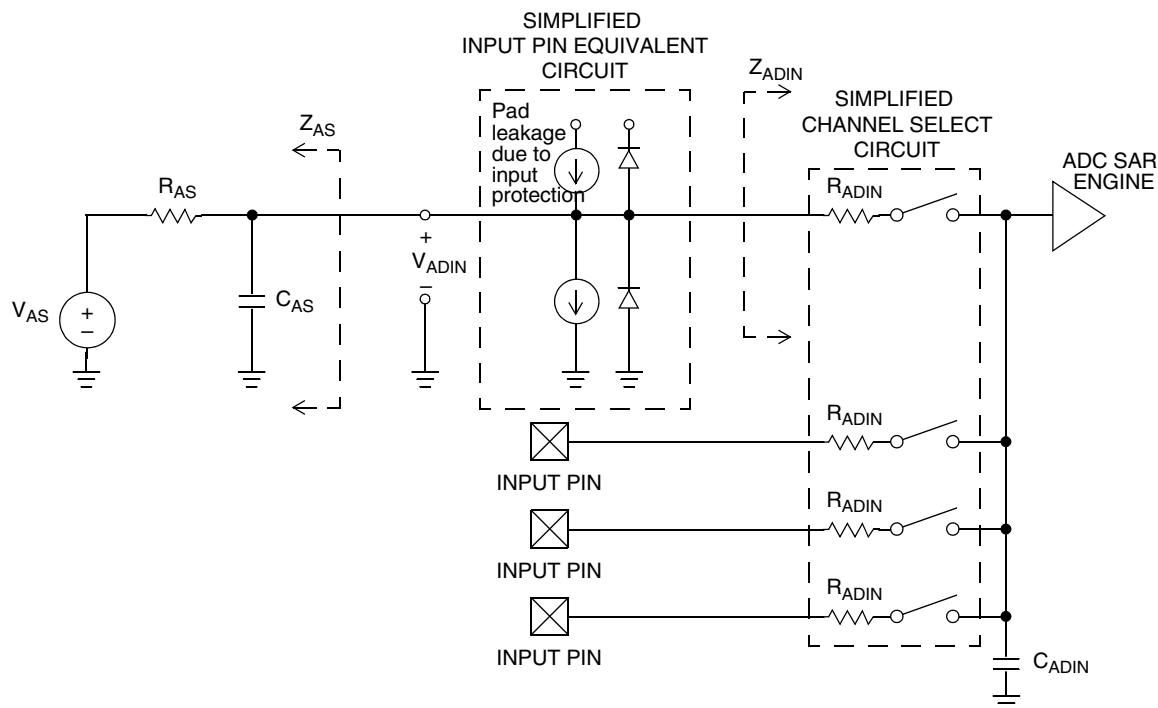


Figure 10. ADC Input Impedance Equivalency Diagram

 Table 14. 5 Volt 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

| Num | C | Characteristic | Conditions | Symb | Min | Typical ¹ | Max | Unit | Comment |
|-----|---|---|-------------------------|-------------|------|----------------------|-----|---------|---------------------------|
| 1 | T | Supply current ADLPC = 1 ADLSMP = 1 ADCO = 1 | | I_{DDA} | — | 133 | — | μA | |
| 2 | T | Supply current ADLPC = 1 ADLSM = 0 ADCO = 1 | | I_{DDA} | — | 218 | — | μA | |
| 3 | T | Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1 | | I_{DDA} | — | 327 | — | μA | |
| 4 | D | Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1 | | I_{DDA} | — | 0.582 | 1 | mA | |
| 5 | T | Supply current | Stop, reset, module off | I_{DDA} | — | 0.011 | 1 | μA | |
| 6 | P | ADC asynchronous clock source | High speed (ADLPC = 0) | f_{ADACK} | 2 | 3.3 | 5 | MHz | $t_{ADACK} = 1/f_{ADACK}$ |
| | | | Low power (ADLPC = 1) | | 1.25 | 2 | 3.3 | | |

Table 14. 5 Volt 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

| Num | C | Characteristic | Conditions | Symb | Min | Typical ¹ | Max | Unit | Comment |
|-----|---|---|---------------------------|--------------|-----|----------------------|------|------------------|--|
| 7 | P | Conversion time (including sample time) | Short sample (ADLSMP = 0) | t_{ADC} | — | 20 | — | ADCK cycles | See Table 10 for conversion time variances |
| | | | Long sample (ADLSMP = 1) | | — | 40 | — | | |
| 8 | T | Sample time | Short sample (ADLSMP = 0) | t_{ADS} | — | 3.5 | — | ADCK cycles | |
| | | | Long sample (ADLSMP = 1) | | — | 23.5 | — | | |
| 9 | T | Total unadjusted error | 12-bit mode | E_{TUE} | — | ±3.0 | — | LSB ² | Includes quantization |
| | P | | 10-bit mode | | — | ±1 | ±2.5 | | |
| | T | | 8-bit mode | | — | ±0.5 | ±1.0 | | |
| 10 | T | Differential non-linearity | 12-bit mode | DNL | — | ±1.75 | — | LSB ² | |
| | P | | 10-bit mode ³ | | — | ±0.5 | ±1.0 | | |
| | T | | 8-bit mode ³ | | — | ±0.3 | ±0.5 | | |
| 11 | T | Integral non-linearity | 12-bit mode | INL | — | ±1.5 | — | LSB ² | |
| | T | | 10-bit mode | | — | ±0.5 | ±1.0 | | |
| | T | | 8-bit mode | | — | ±0.3 | ±0.5 | | |
| 12 | T | Zero-scale error | 12-bit mode | E_{ZS} | — | ±1.5 | — | LSB ² | $V_{ADIN} = V_{SSA}$ |
| | P | | 10-bit mode | | — | ±0.5 | ±1.5 | | |
| | T | | 8-bit mode | | — | ±0.5 | ±0.5 | | |
| 13 | T | Full-scale error | 12-bit mode | E_{FS} | — | ±1 | — | LSB ² | $V_{ADIN} = V_{DDA}$ |
| | P | | 10-bit mode | | — | ±0.5 | ±1 | | |
| | T | | 8-bit mode | | — | ±0.5 | ±0.5 | | |
| 14 | D | Quantization error | 12-bit mode | E_Q | — | −1 to 0 | — | LSB ² | |
| | | | 10-bit mode | | — | — | ±0.5 | | |
| | | | 8-bit mode | | — | — | ±0.5 | | |
| 15 | D | Input leakage error | 12-bit mode | E_{IL} | — | ±1 | — | LSB ² | Pad leakage ^{4*} R_{AS} |
| | | | 10-bit mode | | — | ±0.2 | ±2.5 | | |
| | | | 8-bit mode | | — | ±0.1 | ±1 | | |
| 16 | D | Temp sensor voltage | 25°C | V_{TEMP25} | — | 1.396 | — | V | |
| 17 | D | Temp sensor slope | −40 °C–25 °C | m | — | 3.266 | — | mV/°C | |
| | | | 25 °C–85 °C | | — | 3.638 | — | | |

¹ Typical values assume $V_{DDA} = 5.0$ V, Temp = 25 °C, $f_{ADCK} = 1.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

² 1 LSB = $(V_{REFH} - V_{REFL})/2^N$.

³ Monotonicity and No-Missing-Codes guaranteed in 10-bit and 8-bit modes

⁴ Based on input pad leakage current. Refer to pad electricals.

2.9 External Oscillator (XOSC) Characteristics

Table 15. Oscillator Electrical Specifications (Temperature Range = –40 to 105 °C Ambient)

| Num | C | Rating | Symbol | Min | Typical ¹ | Max | Unit |
|-----|---|--|----------------|---|----------------------|------|------|
| 1 | C | Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) | | | | | |
| | | Low range (RANGE = 0) | f_{lo} | 32 | — | 38.4 | kHz |
| | | High range (RANGE = 1) FEE or FBE mode ² | f_{hi-ll} | 1 | — | 5 | MHz |
| | | High range (RANGE = 1) PEE or PBE mode ³ | f_{hi-pll} | 1 | — | 16 | MHz |
| | | High range (RANGE = 1, HGO = 1) BLPE mode | f_{hi-hgo} | 1 | — | 16 | MHz |
| | | High range (RANGE = 1, HGO = 0) BLPE mode | f_{hi-lp} | 1 | — | 8 | MHz |
| 2 | — | Load capacitors | C_1 C_2 | See crystal or resonator manufacturer's recommendation. | | | |
| 3 | — | Feedback resistor | R_F | | 10 | | MΩ |
| | | Low range (32 kHz to 38.4 kHz) High range (1 MHz to 16 MHz) | | | 1 | | |
| 4 | — | Series resistor | R_S | | | | kΩ |
| | | Low range, low gain (RANGE = 0, HGO = 0) | | — | 0 | — | |
| | | Low range, high gain (RANGE = 0, HGO = 1) | | — | 100 | — | |
| | | High range, low gain (RANGE = 1, HGO = 0) | | — | 0 | — | |
| | | High range, high gain (RANGE = 1, HGO = 1) | | — | 0 | 0 | |
| | | ≥ 8 MHz | | — | 0 | 0 | |
| 5 | T | Crystal start-up time ⁴ | | | | | ms |
| | | Low range, low gain (RANGE = 0, HGO = 0) | $t_{CSTL-LP}$ | — | 200 | — | |
| | | Low range, high gain (RANGE = 0, HGO = 1) | $t_{CSTL-HGO}$ | — | 400 | — | |
| | | High range, low gain (RANGE = 1, HGO = 0) ⁵ | $t_{CSTH-LP}$ | — | 5 | — | |
| | | High range, high gain (RANGE = 1, HGO = 1) ⁵ | $t_{CSTH-HGO}$ | — | 15 | — | |
| | | | | | | | |
| 6 | T | Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) | | | | | MHz |
| | | FEE or FBE mode ² | f_{extal} | 0.03125 | — | 5 | |
| | | PEE or PBE mode ³ | | 1 | — | 16 | |
| | | BLPE mode | | 0 | — | 40 | |

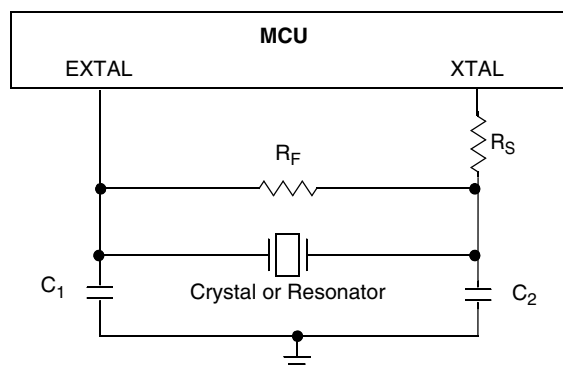
¹ Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.

² When MCG is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.

³ When MCG is configured for PEE or PBE mode, input clock source must be divisible using RDIV to within the range of 1 MHz to 2 MHz.

⁴ This parameter is characterized and not tested on each device. Proper PC board layout procedures must be followed to achieve specifications.

⁵ 4 MHz crystal



2.10 MCG Specifications

Table 16. MCG Frequency Specifications (Temperature Range = -40 to 105 °C Ambient)

| Num | C | Rating | Symbol | Min | Typical ¹ | Max | Unit |
|-----|---|---|--------------------------|-------|----------------------|---------|-------------|
| 1 | C | Internal reference frequency — factory trimmed at $V_{DD} = 5\text{ V}$ and temperature = 25 °C | f_{int_ft} | — | 32.768 | — | kHz |
| 2 | C | Average internal reference frequency — untrimmed | f_{int_ut} | 31.25 | — | 39.0625 | kHz |
| 3 | T | Internal reference startup time | t_{irefst} | — | 60 | 100 | μs |
| 4 | C | DCO output frequency range — untrimmed ² | f_{dco_ut} | 16 | — | 20 | MHz |
| | C | | | 32 | — | 40 | |
| | C | | | 48 | — | 60 | |
| 5 | P | DCO output frequency ² reference = 32768Hz and DMX32 = 1 | f_{dco_DMX32} | — | 16.82 | — | MHz |
| | P | | | — | 33.69 | — | |
| | P | | | — | 50.48 | — | |
| 6 | D | Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM) | $\Delta f_{dco_res_t}$ | — | ±0.1 | ±0.2 | % f_{dco} |
| 7 | D | Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM) | $\Delta f_{dco_res_t}$ | — | ±0.2 | ±0.4 | % f_{dco} |
| 8 | D | Total deviation of trimmed DCO output frequency over voltage and temperature | Δf_{dco_t} | — | 0.5 -1.0 | ±2 | % f_{dco} |
| 9 | D | Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0–70 °C | Δf_{dco_t} | — | ±0.5 | ±1 | % f_{dco} |
| 10 | D | FLL acquisition time ³ | $t_{fll_acquire}$ | — | — | 1 | ms |
| 11 | D | PLL acquisition time ⁴ | $t_{pll_acquire}$ | — | — | 1 | ms |
| 12 | D | Long term jitter of DCO output clock (averaged over 2ms interval) ⁵ | C_{jitter} | — | 0.02 | 0.2 | % f_{dco} |
| 13 | D | VCO operating frequency | f_{vco} | 7.0 | — | 55.0 | MHz |
| 16 | D | Jitter of PLL output clock measured over 625 ns ⁶ | $f_{pll_jitter_625ns}$ | — | 0.566 ⁶ | — | % f_{pll} |
| 17 | D | Lock entry frequency tolerance ⁷ | D_{lock} | ±1.49 | — | ±2.98 | % |

2.11.1 Control Timing

Table 17. Control Timing

| Num | C | Parameter | Symbol | Min | Typical ¹ | Max | Unit |
|-----|---|---|----------------------|-----------------------------|----------------------|------|---------|
| 1 | D | Bus frequency ($t_{cyc} = 1/f_{Bus}$) | f_{Bus} | dc | — | 24 | MHz |
| 2 | D | Internal low-power oscillator period | t_{LPO} | 800 | — | 1500 | μs |
| 3 | D | External reset pulse width ² ($t_{cyc} = 1/f_{Self_reset}$) | t_{extrst} | 100 | — | — | ns |
| 4 | D | Reset low drive | t_{rstdrv} | $66 \times t_{cyc}$ | — | — | ns |
| 5 | D | Active background debug mode latch setup time | t_{MSSU} | 500 | — | — | ns |
| 6 | D | Active background debug mode latch hold time | t_{MSH} | 100 | — | — | ns |
| 7 | D | IRQ pulse width Asynchronous path ² Synchronous path ³ | t_{ILIH}, t_{IHIL} | 100 $1.5 \times t_{cyc}$ | — | — | ns |
| 8 | D | KBIPx pulse width Asynchronous path ² Synchronous path ³ | t_{ILIH}, t_{IHIL} | 100 $1.5 \times t_{cyc}$ | — | — | ns |
| 9 | D | Port rise and fall time (load = 50 pF) ⁴ Slew rate control disabled (PTxSE = 0), Low Drive Slew rate control enabled (PTxSE = 1), Low Drive Slew rate control disabled (PTxSE = 0), Low Drive Slew rate control enabled (PTxSE = 1), Low Drive | t_{Rise}, t_{Fall} | — — — — | 11 35 40 75 | — | ns |

¹ Typical values are based on characterization data at $V_{DD} = 5.0 V$, 25 °C unless otherwise stated.

² This is the shortest pulse that is guaranteed to be recognized as a reset pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

³ This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

⁴ Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40 °C to 105 °C.

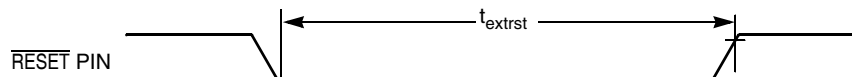


Figure 11. Reset Timing

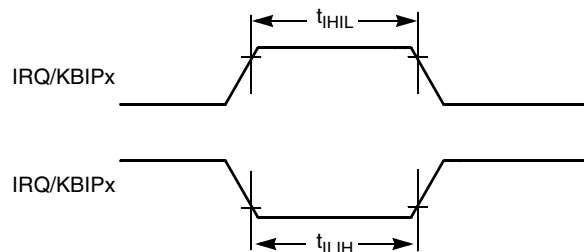
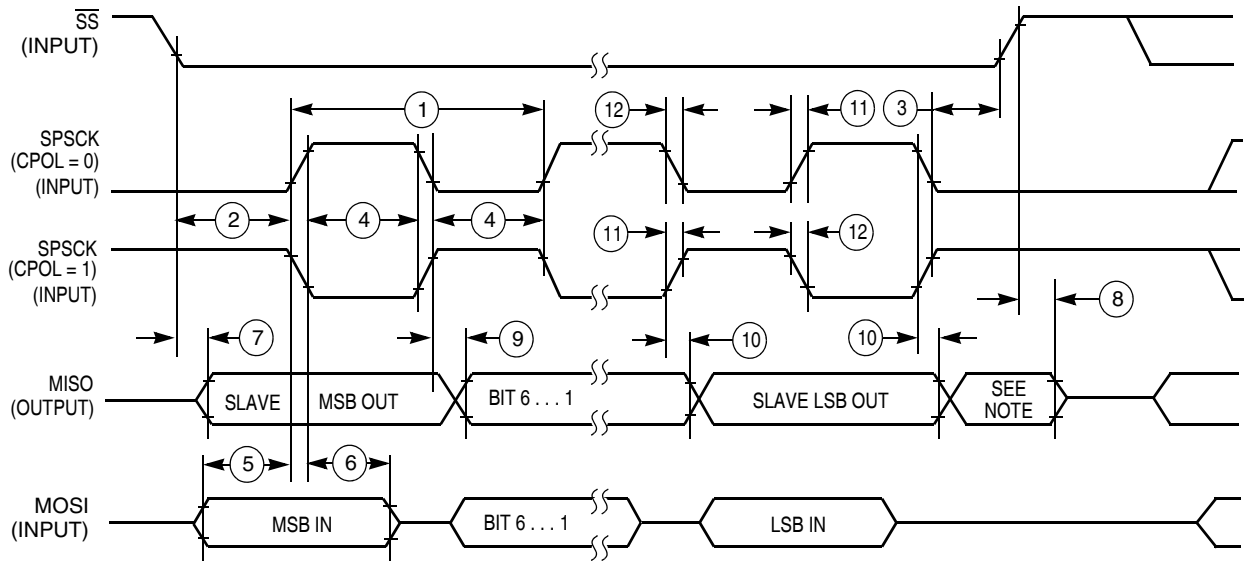
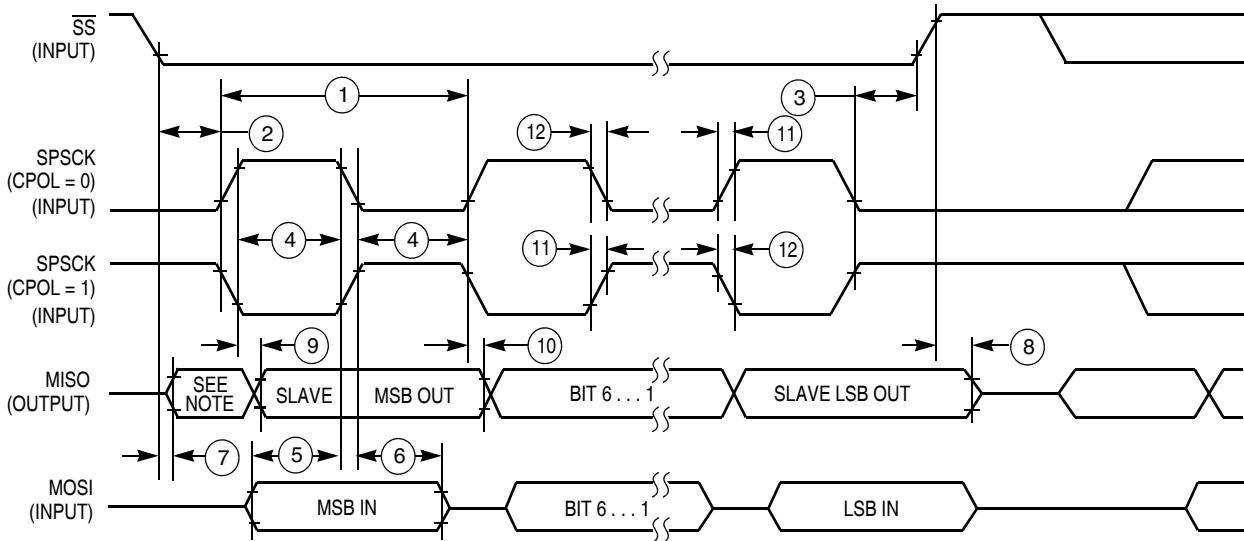


Figure 12. IRQ/KBIPx Timing



NOTE:
1. Not defined but normally MSB of character just received

Figure 17. SPI Slave Timing (CPHA = 0)



NOTE:
1. Not defined but normally LSB of character just received

Figure 18. SPI Slave Timing (CPHA = 1)

2.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the Flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see Chapter 4, “Memory.”

Table 21. Flash Characteristics

| Num | C | Characteristic | Symbol | Min | Typical ¹ | Max | Unit |
|-----|---|---|-------------------------|-------------|----------------------|--------|-------------------|
| 1 | — | Supply voltage for program/erase | $V_{\text{prog/erase}}$ | 2.7 | — | 5.5 | V |
| 2 | — | Supply voltage for read operation | V_{Read} | 2.7 | — | 5.5 | V |
| 3 | — | Internal FCLK frequency ² | f_{FCLK} | 150 | — | 200 | kHz |
| 4 | — | Internal FCLK period (1/FCLK) | t_{Fcyd} | 5 | — | 6.67 | μs |
| 5 | — | Byte program time (random location) ² | t_{prog} | 9 | | | t_{Fcyd} |
| 6 | — | Byte program time (burst mode) ² | t_{Burst} | 4 | | | t_{Fcyd} |
| 7 | — | Page erase time ³ | t_{Page} | 4000 | | | t_{Fcyd} |
| 8 | — | Mass erase time ² | t_{Mass} | 20,000 | | | t_{Fcyd} |
| 9 | C | Program/erase endurance ⁴ T_L to $T_H = -40\text{ }^{\circ}\text{C}$ to $105\text{ }^{\circ}\text{C}$ $T = 25\text{ }^{\circ}\text{C}$ | — | 10,000 — | — 100,000 | — — | cycles |
| 10 | C | Data retention ⁵ | $t_{\text{D-ret}}$ | 15 | 100 | — | years |

¹ Typical values are based on characterization data at $V_{\text{DD}} = 5.0\text{ V}$, $25\text{ }^{\circ}\text{C}$ unless otherwise stated.

² The frequency of this clock is controlled by a software setting.

³ These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

⁴ **Typical endurance for flash** was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale Semiconductor defines typical endurance, please refer to Engineering Bulletin EB619/D, *Typical Endurance for Nonvolatile Memory*.

⁵ **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to $25\text{ }^{\circ}\text{C}$ using the Arrhenius equation. For additional information on how Freescale Semiconductor defines typical data retention, please refer to Engineering Bulletin EB618/D, *Typical Data Retention for Nonvolatile Memory*.

2.14 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

2.14.1 Radiated Emissions

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM Cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (North and East). For more detailed information concerning the evaluation results, conditions and setup, please refer to the EMC Evaluation Report for this device.