Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	-
Core Size	-
Speed	-
Connectivity	-
Peripherals	-
Number of I/O	-
Program Memory Size	-
Program Memory Type	-
EEPROM Size	-
RAM Size	-
Voltage - Supply (Vcc/Vdd)	-
Data Converters	-
Oscillator Type	-
Operating Temperature	-
Mounting Type	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf51ac128cclke

Table of Contents

List of Figures

List of Tables

Table 1. MCF51AC256 Series Device Comparison (continued)

Feature	MCF51AC256A		MCF51AC256B			MCF51AC128A		MCF51AC128C		
	80-pin	64-pin	80-pin	64-pin	44-pin	80-pin	64-pin	80-pin	64-pin	44-pin
TPM3 (timer pulse-width modulator) channels	2									
VBUS (debug visibility bus)	Yes	No	Yes	No		Yes	No	Yes	No	

1 The members of MCF51AC128A with CAN support have 32 KB RAM. The other members have 16 KB RAM.

2 Up to 16 pins on Ports E and F are shared with the ColdFire Rapid GPIO module.

1.2 Block Diagram

Figure 1 shows the connections between the MCF51AC256 series pins and modules.

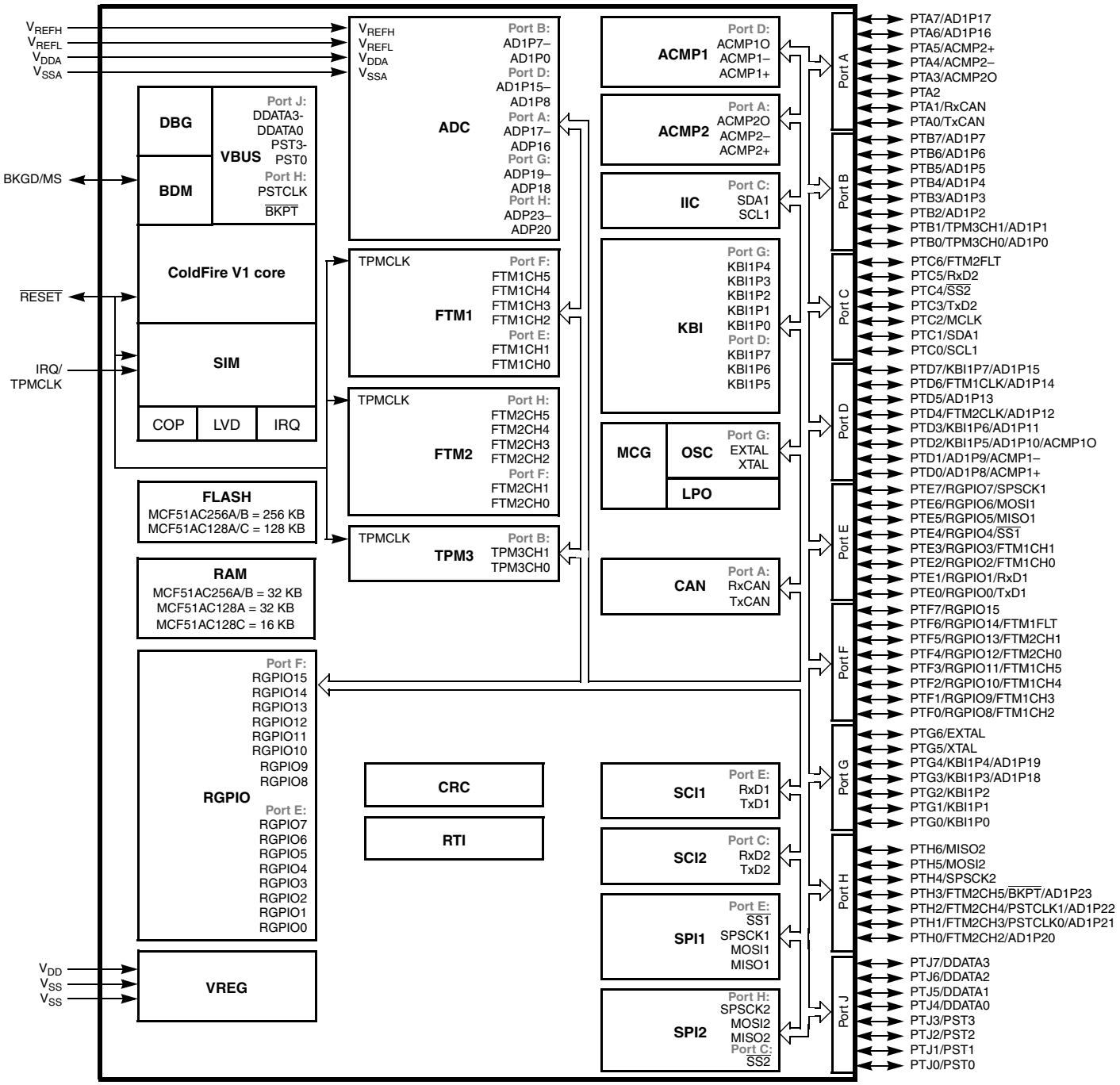


Figure 1. MCF51AC256 Series Block Diagram

1.3.1 Feature List

- 32-bit Version 1 ColdFire® central processor unit (CPU)
  - Up to 50.33 MHz at 2.7 V – 5.5 V
  - Provide 0.94 Dhrystone 2.1 DMIPS per MHz performance when running from internal RAM (0.76 DMIPS per MHz when running from flash)
  - Implements instruction set revision C (ISA_C)
- On-chip memory
  - Up to 256 KB flash memory read/program/erase over full operating voltage and temperature
  - Up to 32 KB static random access memory (SRAM)
  - Security circuitry to prevent unauthorized access to SRAM and flash contents
- Power-Saving Modes
  - Three low-power stop plus wait modes
  - Peripheral clock enable register can disable clocks to unused modules, reducing currents; allows clocks to remain enabled to specific peripherals in stop3 mode
- System protection features
  - Watchdog computer operating properly (COP) reset with options to run from independent LPO clock or bus clock
  - Low-voltage detection with reset or interrupt
  - Illegal opcode and illegal address detection with programmable reset or exception response
  - Flash block protection
- Debug support
  - Single-wire background debug interface
  - Real-time debug support, with 6 hardware breakpoints (4 PC, 1 address pair and 1 data) that can be configured into a 1- or 2-level trigger
  - On-chip trace buffer provides programmable start/stop recording conditions plus support for continuous or PC-profiling modes
  - Support for real-time program (and optional partial data) trace using the debug visibility bus
- V1 ColdFire interrupt controller (CF1_INTC)
  - Support of 40 peripheral I/O interrupt requests plus seven software (one per level) interrupt requests
  - Fixed association between interrupt request source and level plus priority, up to two requests can be remapped to the highest maskable level + priority
  - Unique vector number for each interrupt source
  - Support for service routine interrupt acknowledge (software IACK) read cycles for improved system performance
- Multipurpose clock generator (MCG)
  - Oscillator (XOSC); loop-control Pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
  - LPO clock as an optional independent clock source for COP and RTI
  - FLL/PLL controlled by internal or external reference

- Inter-integrated circuit (IIC)
  - Compatible with IIC bus standard
  - Multi-master operation
  - Software programmable for one of 64 different serial clock frequencies
  - Interrupt driven byte-by-byte data transfer
  - Arbitration lost interrupt with automatic mode switching from master to slave
  - Calling address identification interrupt
  - Bus busy detection
  - 10-bit address extension
- Controller area network (CAN)
  - Implementation of the CAN protocol — Version 2.0A/B
    - Standard and extended data frames
    - Zero to eight bytes data length
    - Programmable bit rate up to 1 Mbps
    - Support for remote frames
  - Five receive buffers with FIFO storage scheme
  - Three transmit buffers with internal prioritization using a “local priority” concept
  - Flexible maskable identifier filter supports two full-size (32-bit) extended identifier filters, four 16-bit filters, or eight 8-bit filters
  - Programmable wakeup functionality with integrated low-pass filter
  - Programmable loopback mode supports self-test operation
  - Programmable listen-only mode for monitoring of CAN bus
  - Programmable bus-off recovery functionality
  - Separate signalling and interrupt capabilities for all CAN receiver and transmitter error states (warning, error passive, bus-off)
  - Internal timer for time-stamping of received and transmitted messages
- Serial communications interfaces (SCI)
  - Full-duplex, standard non-return-to-zero (NRZ) format
  - Double-buffered transmitter and receiver with separate enables
  - Programmable baud rates (13-bit modulo divider)
  - Interrupt-driven or polled operation
  - Hardware parity generation and checking
  - Programmable 8-bit or 9-bit character length
  - Receiver wakeup by idle-line or address-mark
  - Optional 13-bit break character generation / 11-bit break character detection
  - Selectable transmitter output polarity
- Serial peripheral interfaces (SPI)
  - Master or slave mode operation
  - Full-duplex or single-wire bidirectional option
  - Programmable transmit bit rate

Table 3. Orderable Part Number Summary

MCF51AC256ACPUE	MCF51AC256 ColdFire Microcontroller with CAN	256 / 32	64 LQFP	–40°C to 85°C
MCF51AC256BCPUE	MCF51AC256 ColdFire Microcontroller without CAN	256 / 32	64 LQFP	–40°C to 85°C
MCF51AC256BCFGE	MCF51AC256 ColdFire Microcontroller without CAN	256/32	44 LQFP	–40°C to 85°C
MCF51AC128ACFUE	MCF51AC128 ColdFire Microcontroller with CAN	128 / 32	64 QFP	–40°C to 85°C
MCF51AC128CCFUE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	64 QFP	–40°C to 85°C
MCF51AC128ACLKE	MCF51AC128 ColdFire Microcontroller with CAN	128 / 32	80 LQFP	–40°C to 85°C
MCF51AC128CCLKE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	80 LQFP	–40°C to 85°CC
MCF51AC128ACPUE	MCF51AC128 ColdFire Microcontroller with CAN	128 / 32	64 LQFP	–40°C to 85°C
MCF51AC128CCPUE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	64 LQFP	–40°C to 85°C
MCF51AC128CCFGE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	44 LQFP	–40°C to 85°C

1.5 Pinouts and Packaging

Figure 2 shows the pinout of the 80-pin LQFP.

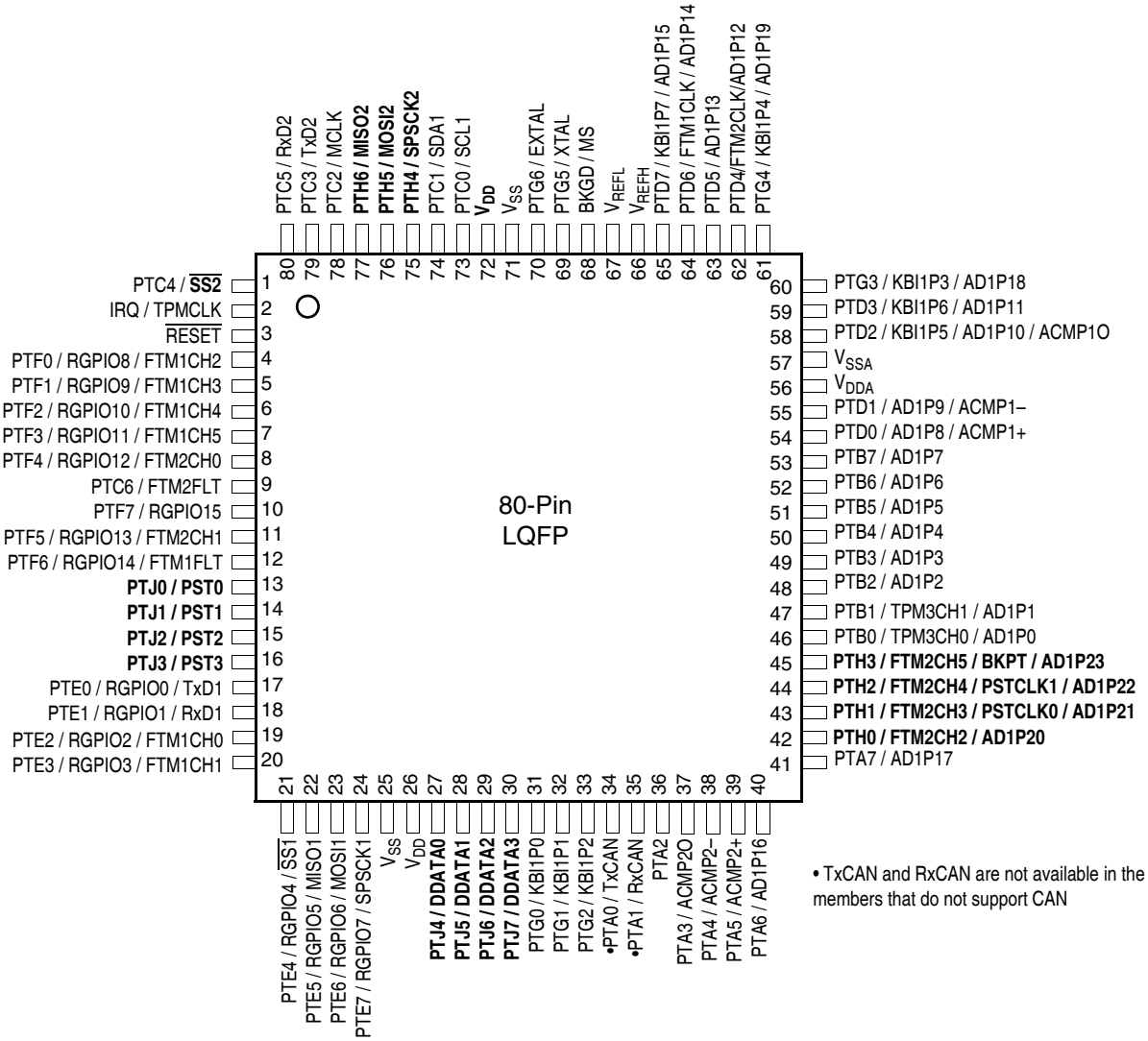


Figure 2. MCF51AC256 Series ColdFire Microcontroller 80-Pin LQFP

Figure 3 shows the pinout of the 64-pin LQFP and QFP.

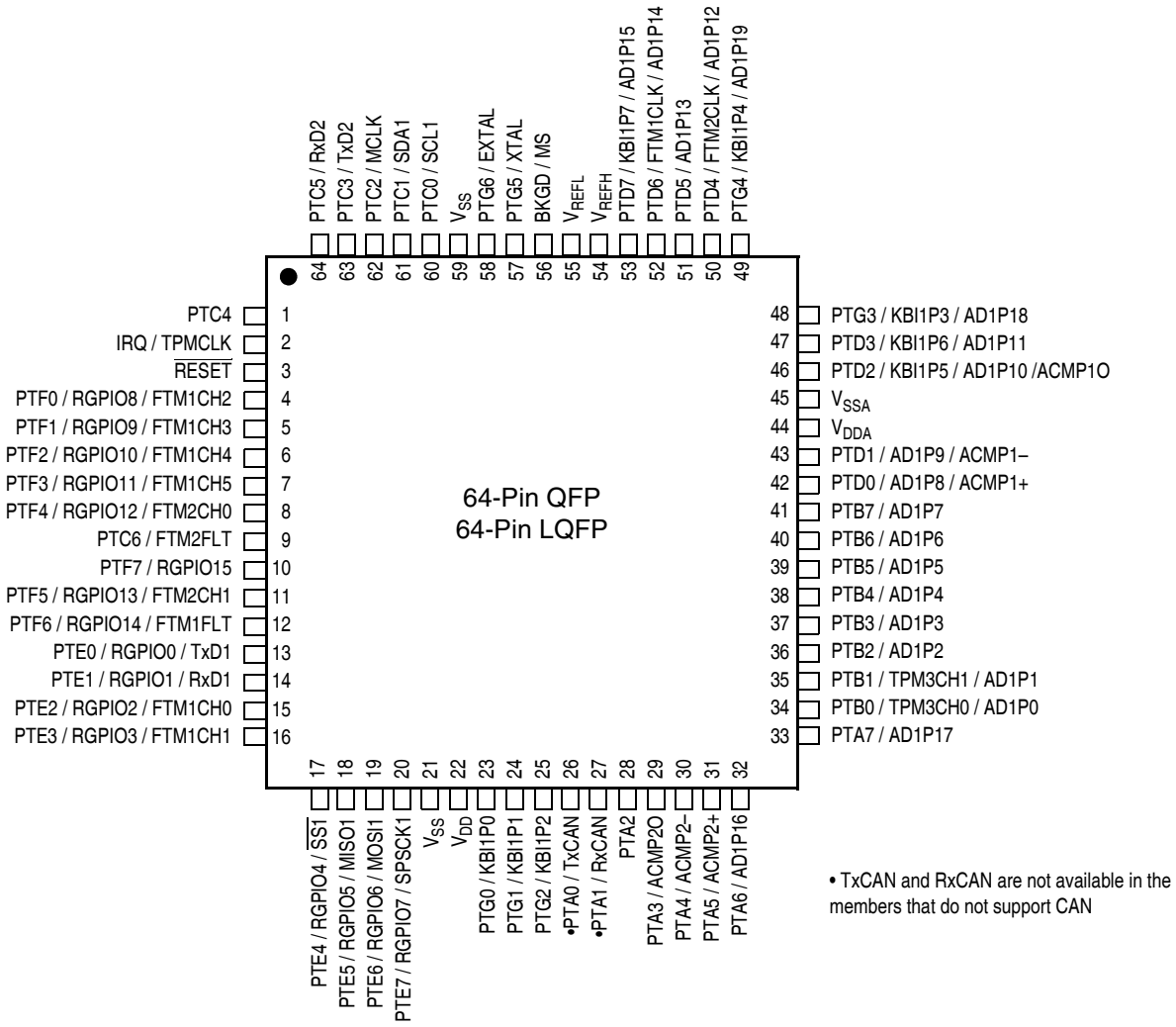


Figure 3. MCF51AC256 Series ColdFire Microcontroller 64-Pin QFP/LQFP

Figure 4 shows the pinout of the 44-pin LQFP.

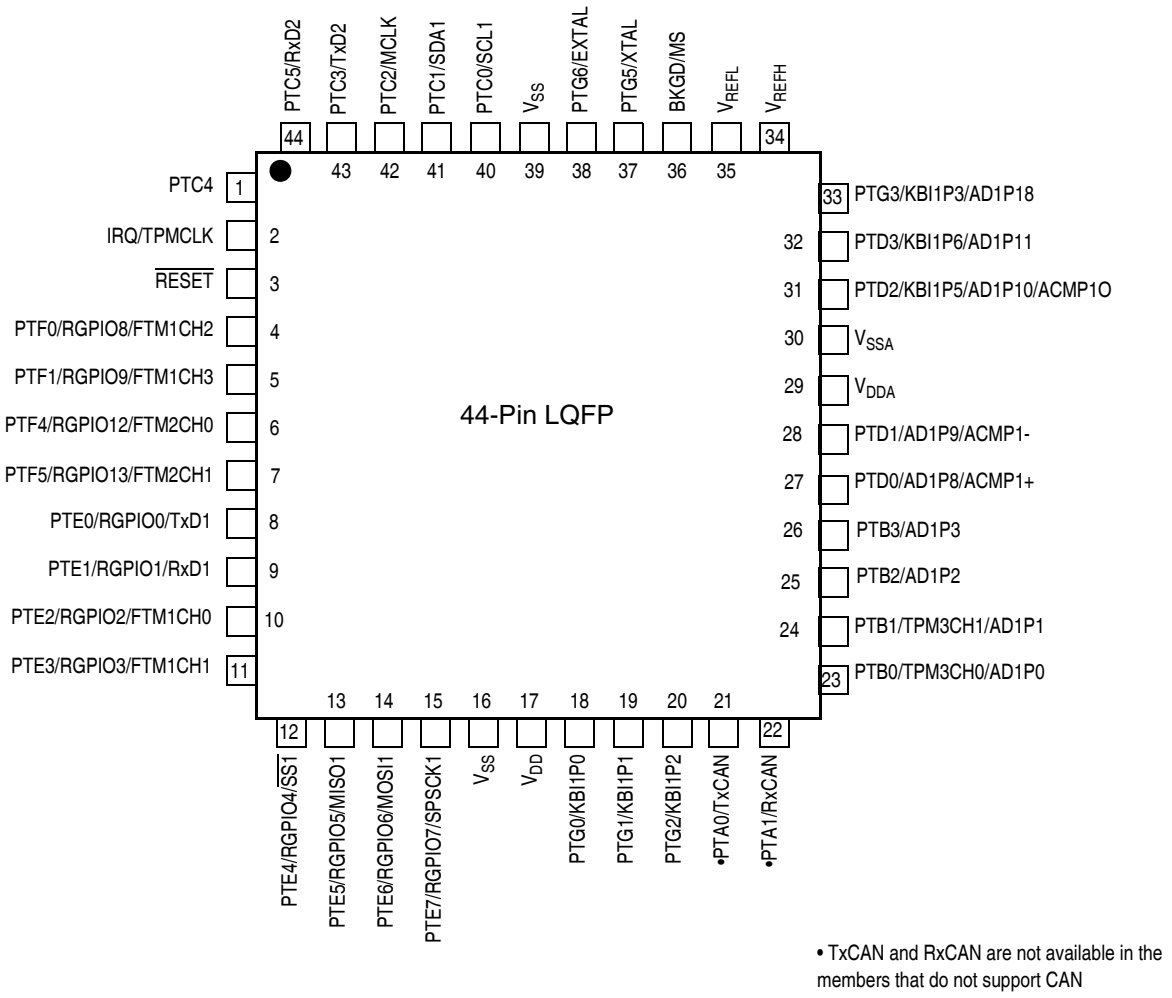


Figure 4. MCF51AC256 Series ColdFire Microcontroller 44-Pin LQFP

Table 4 shows the package pin assignments.

Table 4. Pin Availability by Package Pin-Count

Pin Number			Lowest <-- Priority --> Highest			
80	64	44	Port Pin	Alt 1	Alt 2	Alt 3
1	1	1	PTC4	$\overline{SS2}$		
2	2	2	IRQ	TPMCLK[1]		
3	3	3	$\overline{RESET}$			
4	4	4	PTF0	RGPIO8	FTM1CH2	
5	5	5	PTF1	RGPIO9	FTM1CH3	
6	6	—	PTF2	RGPIO10	FTM1CH4	
7	7	—	PTF3	RGPIO11	FTM1CH5	

Table 4. Pin Availability by Package Pin-Count (continued)

Pin Number			Lowest <-- Priority --> Highest			
80	64	44	Port Pin	Alt 1	Alt 2	Alt 3
8	8	6	PTF4	RGPIO12	FTM2CH0	
9	9	—	PTC6	FTM2FLT		
10	10	—	PTF7	RGPIO15		
11	11	7	PTF5	RGPIO13	FTM2CH1	
12	12	—	PTF6	RGPIO14	FTM1FLT	
13	—	—	PTJ0	PST0		
14	—	—	PTJ1	PST1		
15	—	—	PTJ2	PST2		
16	—	—	PTJ3	PST3		
17	13	8	PTE0	RGPIO0	TxD1	
18	14	9	PTE1	RGPIO1	RxD1	
19	15	10	PTE2	RGPIO2	FTM1CH0	
20	16	11	PTE3	RGPIO3	FTM1CH1	
21	17	12	PTE4	RGPIO4	$\overline{SS1}$	
22	18	13	PTE5	RGPIO5	MISO1	
23	19	14	PTE6	RGPIO6	MOSI1	
24	20	15	PTE7	RGPIO7	SPSCK1	
25	21	16	V_{SS}			
26	22	17	V_{DD}			
27	—	—	PTJ4	DDATA0		
28	—	—	PTJ5	DDATA1		
29	—	—	PTJ6	DDATA2		
30	—	—	PTJ7	DDATA3		
31	23	18	PTG0	KBI1P0		
32	24	19	PTG1	KBI1P1		
33	25	20	PTG2	KBI1P2		
34	26	21	PTA0	TxCAN[2]		
35	27	22	PTA1	RxCAN[3]		
36	28	—	PTA2			
37	29	—	PTA3	ACMP2O		
38	30	—	PTA4	ACMP2–		
39	31	—	PTA5	ACMP2+		
40	32	—	PTA6	AD1P16		
41	33	—	PTA7	AD1P17		
42	—	—	PTH0	FTM2CH2	AD1P20	
43	—	—	PTH1	FTM2CH3	PSTCLK0	AD1P21
44	—	—	PTH2	FTM2CH4	PSTCLK1	AD1P22
45	—	—	PTH3	FTM2CH5	BKPT	AD1P23
46	34	23	PTB0	TPM3CH0	AD1P0	
47	35	24	PTB1	TPM3CH1	AD1P1	
48	36	25	PTB2	AD1P2		

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance

2 Junction to Ambient Natural Convection

3 1s — Single layer board, one signal layer

4 2s2p — Four layer board, 2 signal and 2 power layers

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power

$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

2.4 Electrostatic Discharge (ESD) Protection Characteristics

Although damage from static discharge is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with CDF-AEC-Q00 Stress Test Qualification for Automotive Grade Integrated Circuits. (http://www.aecouncil.com/) This device was qualified to AEC-Q100 Rev E.

A device is considered to have failed if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete dc parametric and functional testing is performed per the

applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 8. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human body	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulse per pin	—	3	
Charge device model	Series resistance	R1	0	Ω
	Storage capacitance	C	0	pF
	Number of pulse per pin	—	3	—
Latch-up	Minimum input voltage limit	—	–2.5	V
	Maximum input voltage limit	—	7.5	V

Table 9. ESD and Latch-Up Protection Characteristics

Num	Rating	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	±2000	—	V
2	Charge device model (CDM)	V_{CDM}	±500	—	V
3	Latch-up current at T_A = 85 °C	I_{LAT}	±100	—	mA

2.5 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

Table 10. DC Characteristics

Num	C	Parameter	Symbol	Min	Typical[1]	Max	Unit
1	—	Operating voltage		2.7	—	5.5	V
2	P	Output high voltage — Low drive (PTxDSn = 0) 5 V, I_{Load} = –4 mA 3 V, I_{Load} = –2 mA 5 V, I_{Load} = –2 mA 3 V, I_{Load} = –1 mA	V_{OH}	 V_{DD} – 1.5 V_{DD} – 1.5 V_{DD} – 0.8 V_{DD} – 0.8	 — — — —	 — — — —	V
		Output high voltage — High drive (PTxDSn = 1) 5 V, I_{Load} = –15 mA 3 V, I_{Load} = –8 mA 5 V, I_{Load} = –8 mA 3 V, I_{Load} = –4 mA		 V_{DD} – 1.5 V_{DD} – 1.5 V_{DD} – 0.8 V_{DD} – 0.8	 — — — —	 — — — —	

Table 10. DC Characteristics (continued)

Num	C	Parameter	Symbol	Min	Typical[1]	Max	Unit
3	P	Output low voltage — Low Drive (PTxDSn = 0) 5 V, I_{Load} = 4 mA 3 V, I_{Load} = 2 mA 5 V, I_{Load} = 2 mA 3 V, I_{Load} = 1 mA	V_{OL}	—	—	1.5 1.5 0.8 0.8	V
		Output low voltage — High Drive (PTxDSn = 1) 5 V, I_{Load} = 15 mA 3 V, I_{Load} = 8 mA 5 V, I_{Load} = 8 mA 3 V, I_{Load} = 4 mA		—	—	1.5 1.5 0.8 0.8	
4	C	Output high current — Max total I_{OH} for all ports 5V 3V	I_{OHT}	—	—	100 60	mA
5	C	Output low current — Max total I_{OL} for all ports 5 V 3 V	I_{OLT}	—	—	100 60	mA
6	P	Input high voltage; all digital inputs	V_{IH}	0.65 × V_{DD}	—	—	V
7	P	Input low voltage; all digital inputs	V_{IL}	—	—	0.35 × V_{DD}	V
8	D	Input hysteresis; all digital inputs	V_{hys}	0.06 × V_{DD}	—	—	mV
9	P	Input leakage current; input only pins[2]	$\|I_{In}\|$	—	0.1	1	µA
10	P	High impedance (off-state) leakage current[2]	$\|I_{OZ}\|$	—	0.1	1	µA
11	P	Internal pullup resistors[3]	R_{PU}	20	45	65	kΩ
12	P	Internal pulldown resistors[4]	R_{PD}	20	45	65	kΩ
13	C	Input capacitance; all non-supply pins	C_{In}	—	—	8	pF
14	P	POR rearm voltage	V_{POR}	0.9	1.4	2.0	V
15	D	POR rearm time	t_{POR}	10	—	—	µs
16	P	Low-voltage detection threshold — high range V_{DD} falling V_{DD} rising	V_{LVDH}	4.2 4.27	4.35 4.4	4.5 4.6	V
17	P	Low-voltage detection threshold — low range V_{DD} falling V_{DD} rising	V_{LVDL}	2.48 2.5	2.68 2.7	2.7 2.72	V
18	P	Low-voltage warning threshold — high range V_{DD} falling V_{DD} rising	V_{LVWH}	4.2 4.27	4.4 4.45	4.5 4.6	V
19	P	Low-voltage warning threshold low range V_{DD} falling V_{DD} rising	V_{LVWL}	2.48 2.5	2.68 2.7	2.7 2.72	V
20	T	Low-voltage inhibit reset/recover hysteresis 5 V 3 V	V_{hys}	—	100 60	—	mV
21	D	RAM retention voltage	V_{RAM}	—	0.6	1.0	V

Table 10. DC Characteristics (continued)

Num	C	Parameter	Symbol	Min	Typical[1]	Max	Unit
22	D	DC injection current[5 6 7 8] (single pin limit) $V_{IN} > V_{DD}$ $V_{IN} < V_{SS}$	I_{IC}	 0 0	—	 2 –0.2	mA
		DC injection current (Total MCU limit, includes sum of all stressed pins) $V_{IN} > V_{DD}$ $V_{IN} < V_{SS}$		 0 0	—	 25 –5	mA

1 Typical values are based on characterization data at 25°C unless otherwise stated.

2 Measured with $V_{In} = V_{DD}$ or V_{SS}.

3 Measured with $V_{In} = V_{SS}$.

4 Measured with $V_{In} = V_{DD}$.

5 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

6 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

7 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

8 The $\overline{\text{RESET}}$ pin does not have a clamp diode to V_{DD}. Do not drive this pin above V_{DD}.

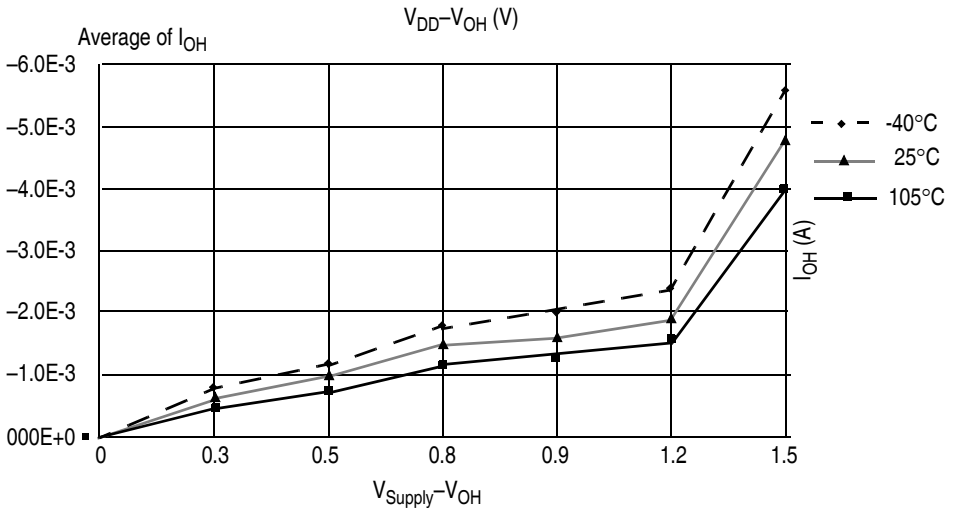
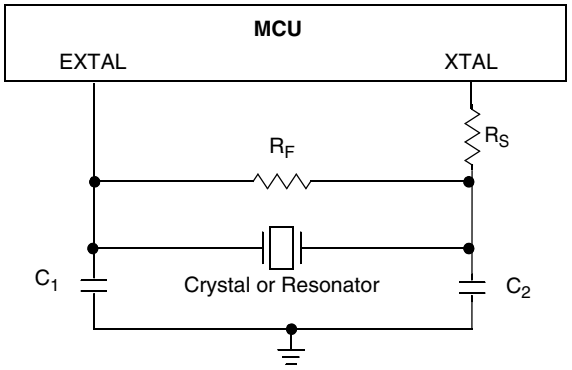


Figure 5. Typical I_{OH} vs. V_{DD}–V_{OH} at V_{DD} = 3 V (Low Drive, PTxDSn = 0)

2.6 Supply Current Characteristics

Table 11. Supply Current Characteristics

Num	C	Parameter		Symbol	V_{DD} (V)	Typical[1]	Max[2]	Unit
1	T	Run supply current measured at FEI mode, all modules off, system clock at:	2 MHz	RI_{DD}	5	2.27	—	mA
					3.3	2.24	—	
			4 MHz		5	3.67	—	
					3.3	3.64	—	
			8 MHz		5	6.55	—	
					3.3	6.54	—	
			16 MHz		5	11.90	—	
					3.3	11.85	—	
2	T	Run supply current measured at FEI mode, all modules on, system clock at:	2 MHz		5	3.28	—	
					3.3	3.26	—	
			4 MHz		5	4.33	—	
					3.3	4.32	—	
			8 MHz		5	8.17	—	
					3.3	8.05	—	
			16 MHz		5	14.8	—	
					3.3	14.74	—	
3	T	Run supply current measured at FBE mode, all modules off (RANGE = 1, HGO = 0), system clock at:	2 MHz		5	3.28	—	
					3.3	3.26	—	
			4 MHz		5	4.69	—	
					3.3	4.67	—	
			8 MHz		5	7.48	—	
					3.3	7.46	—	
			16 MHz		5	13.10	—	
					3.3	13.07	—	
4	T	Run supply current measured at FBE mode, all modules on (RANGE = 1, HGO = 0), system clock at:	2 MHz		5	3.64	—	
					3.3	3.63	—	
			4 MHz		5	5.38	—	
					3.3	5.35	—	
			8 MHz		5	8.65	—	
					3.3	8.64	—	
			16 MHz		5	15.55	—	
					3.3	15.40	—	



2.10 MCG Specifications

Table 16. MCG Frequency Specifications (Temperature Range = –40 to 105 °C Ambient)

Num	C	Rating		Symbol	Min	Typical[1]	Max	Unit
1	C	Internal reference frequency — factory trimmed at V_{DD} = 5 V and temperature = 25 °C		f_{int_ft}	—	32.768	—	kHz
2	C	Average internal reference frequency — untrimmed		f_{int_ut}	31.25	—	39.0625	kHz
3	T	Internal reference startup time		t_{irefst}	—	60	100	µs
4	C	DCO output frequency range — untrimmed [2]	Low range (DRS=00)	f_{dco_ut}	16	—	20	MHz
	C		Mid range (DRS=01)		32	—	40	
	C		High range (DRS=10)		48	—	60	
5	P	DCO output frequency[2] reference =32768Hz and DMX32 = 1	Low range (DRS=00)	f_{dco_DMX32}	—	16.82	—	MHz
	P		Mid range (DRS=01)		—	33.69	—	
	P		High range (DRS=10)		—	50.48	—	
6	D	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)		$\Delta f_{dco\_res\_t}$	—	±0.1	±0.2	$\%f_{dco}$
7	D	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)		$\Delta f_{dco\_res\_t}$	—	±0.2	±0.4	$\%f_{dco}$
8	D	Total deviation of trimmed DCO output frequency over voltage and temperature		Δf_{dco_t}	—	0.5 –1.0	±2	$\%f_{dco}$
9	D	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0–70 °C		Δf_{dco_t}	—	±0.5	±1	$\%f_{dco}$
10	D	FLL acquisition time[3]		$t_{fll\_acquire}$	—	—	1	ms
11	D	PLL acquisition time[4]		$t_{pll\_acquire}$	—	—	1	ms
12	D	Long term jitter of DCO output clock (averaged over 2ms interval) [5]		C_{Jitter}	—	0.02	0.2	$\%f_{dco}$
13	D	VCO operating frequency		f_{vco}	7.0	—	55.0	MHz
16	D	Jitter of PLL output clock measured over 625 ns[6]		$f_{pll\_jitter\_625ns}$	—	0.566[6]	—	$\%f_{pll}$
17	D	Lock entry frequency tolerance [7]		D_{lock}	±1.49	—	±2.98	%

Table 16. MCG Frequency Specifications (continued)(Temperature Range = –40 to 105 °C Ambient)

Num	C	Rating	Symbol	Min	Typical[1]	Max	Unit
18	D	Lock exit frequency tolerance [8]	D_{unl}	±4.47	—	±5.97	%
19	D	Lock time — FLL	t_{fll_lock}	—	—	$t_{fll\_acquire}$+ 1075(1/f_{int_t})	s
20	D	Lock time — PLL	t_{pll_lock}	—	—	$t_{pll\_acquire}$+ 1075(1/f_{pll_ref})	s
21	D	Loss of external clock minimum frequency — RANGE = 0	f_{loc_low}	(3/5) × f_{int}	—	—	kHz

1 Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.

2 The resulting bus clock frequency must not exceed the maximum specified bus clock frequency of the device.

3 This specification applies when the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

4 This specification applies when the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

5 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

6 625 ns represents 5 time quanta for CAN applications, under worst case conditions of 8 MHz CAN bus clock, 1 Mbps CAN bus speed, and 8 time quanta per bit for bit time settings. 5 time quanta is the minimum time between a synchronization edge and the sample point of a bit using 8 time quanta per bit.

7 Below D_{lock} minimum, the MCG enters lock. Above D_{lock} maximum, the MCG will not enter lock. But if the MCG is already in lock, then the MCG may stay in lock.

8 Below D_{unl} minimum, the MCG will not exit lock if already in lock. Above D_{unl} maximum, the MCG is guaranteed to exit lock.

2.11 AC Characteristics

This section describes ac timing characteristics for each peripheral system.

2.11.1 Control Timing

Table 17. Control Timing

Num	C	Parameter	Symbol	Min	Typical[1]	Max	Unit
1	D	Bus frequency (t_{cyc} = 1/f_{Bus})	f_{Bus}	dc	—	24	MHz
2	D	Internal low-power oscillator period	t_{LPO}	800	—	1500	µs
3	D	External reset pulse width[2] (t_{cyc} = 1/f_{Self_reset})	t_{extrst}	100	—	—	ns
4	D	Reset low drive	t_{rstdrv}	66 × t_{cyc}	—	—	ns
5	D	Active background debug mode latch setup time	t_{MSSU}	500	—	—	ns
6	D	Active background debug mode latch hold time	t_{MSH}	100	—	—	ns
7	D	IRQ pulse width Asynchronous path[2] Synchronous path[3]	t_{ILIH}, t_{IHIL}	 100 1.5 × t_{cyc}	—	—	ns
8	D	KBIPx pulse width Asynchronous path[2] Synchronous path[3]	t_{ILIH}, t_{IHIL}	 100 1.5 × t_{cyc}	—	—	ns
9	D	Port rise and fall time (load = 50 pF)[4] Slew rate control disabled (PTxSE = 0), Low Drive Slew rate control enabled (PTxSE = 1), Low Drive Slew rate control disabled (PTxSE = 0), Low Drive Slew rate control enabled (PTxSE = 1), Low Drive	t_{Rise}, t_{Fall}	 — — — —	 11 35 40 75	—	ns

1 Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.

2 This is the shortest pulse that is guaranteed to be recognized as a reset pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

3 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

4 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40 °C to 105 °C.

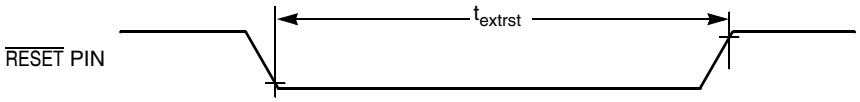


Figure 11. Reset Timing

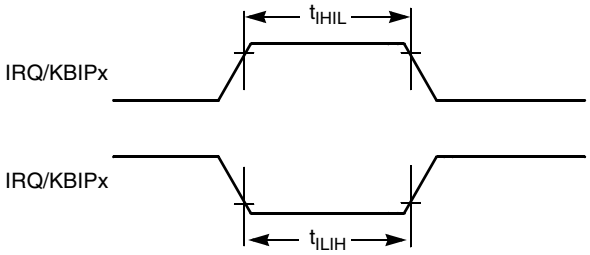


Figure 12. IRQ/KBIPx Timing

Table 21. Flash Characteristics

Num	C	Characteristic	Symbol	Min	Typical[1]	Max	Unit
1	—	Supply voltage for program/erase	$V_{prog/erase}$	2.7	—	5.5	V
2	—	Supply voltage for read operation	V_{Read}	2.7	—	5.5	V
3	—	Internal FCLK frequency[2]	f_{FCLK}	150	—	200	kHz
4	—	Internal FCLK period (1/FCLK)	t_{Fcyc}	5	—	6.67	µs
5	—	Byte program time (random location)[2]	t_{prog}	9			t_{Fcyc}
6	—	Byte program time (burst mode)[2]	t_{Burst}	4			t_{Fcyc}
7	—	Page erase time[3]	t_{Page}	4000			t_{Fcyc}
8	—	Mass erase time[2]	t_{Mass}	20,000			t_{Fcyc}
9	C	Program/erase endurance[4] T_L to T_H = –40 °C to 105 °C T = 25 °C	—	10,000 —	— 100,000	— —	cycles
10	C	Data retention[5]	t_{D_ret}	15	100	—	years

1 Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.

2 The frequency of this clock is controlled by a software setting.

3 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

4 **Typical endurance for flash** was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale Semiconductor defines typical endurance, please refer to Engineering Bulletin EB619/D, *Typical Endurance for Nonvolatile Memory.*

5 **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale Semiconductor defines typical data retention, please refer to Engineering Bulletin EB618/D, *Typical Data Retention for Nonvolatile Memory.*

2.14 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

2.14.1 Radiated Emissions

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM Cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (North and East). For more detailed information concerning the evaluation results, conditions and setup, please refer to the EMC Evaluation Report for this device.

3 Mechanical Outline Drawings

Table 22 provides the available package types and their document numbers. The latest package outline/mechanical drawings are available on the MCF51AC256 Series Product Summary pages at http://www.freescale.com.

To view the latest drawing, either:

- Click on the appropriate link in Table 22, or
- Open a browser to the FreescaleÆ website (http://www.freescale.com), and enter the appropriate document number (from Table 22) in the “Enter Keyword” search box at the top of the page.

Table 22. Package Information

Pin Count	Type	Document No.
80	LQFP	98ARL10530D
64	LQFP	98ASS23234W
64	QFP	98ASB42844B
44	LQFP	98ASS23225W