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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	LVD, PWM, WDT
Number of I/O	69
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf51ac256aclke

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1 MCF51AC256 Family Configurations

1.1 Device Comparison

The MCF51AC256 series is summarized in Table 1.

Table 1. MCF51AC256 Series Device Comparison

Feature	MCF51AC256A		MCF51AC256B			MCF51AC128A		MCF51AC128C		
	80-pin	64-pin	80-pin	64-pin	44-pin	80-pin	64-pin	80-pin	64-pin	44-pin
Flash memory size (Kbytes)	256					128				
RAM size (Kbytes)	32					32 or 16[1]				
V1 ColdFire core with BDM (background debug module)	Yes									
ACMP1 (analog comparator)	Yes									
ACMP2 (analog comparator)	Yes		Yes		No	Yes				No
ADC (analog-to-digital converter) channels (12-bit)	24	20	24	20	9	24	20	24	20	9
CAN (controller area network)	Yes		No			Yes		No		
COP (computer operating properly)	Yes									
CRC (cyclic redundancy check)	Yes									
RTI	Yes									
DBG (debug)	Yes									
IIC1 (inter-integrated circuit)	Yes									
IRQ (interrupt request input)	Yes									
INTC (interrupt controller)	Yes									
KBI (keyboard interrupts)	Yes									
LVD (low-voltage detector)	Yes									
MCG (multipurpose clock generator)	Yes									
OSC (crystal oscillator)	Yes									
Port I/O[2]	69	54	69	54	36	69	54	69	54	36
RGPIO (rapid general-purpose I/O)	16				12	16				12
SCI1, SCI2 (serial communications interfaces)	Yes									
SPI1 (serial peripheral interface)	Yes									
SPI2 (serial peripheral interface)	Yes	No	Yes	No		Yes	No	Yes	No	
FTM1 (flexible timer module) channels	6				4	6				4
FTM2 channels	6	2	6	2	2	6	2	6	2	2

  - Trimmable internal reference allows 0.2% resolution and 2% deviation
- Analog-to-digital converter (ADC)
  - 24 analog inputs with 12 bits resolution
  - Output formatted in 12-, 10- or 8-bit right-justified format
  - Single or continuous conversion (automatic return to idle after single conversion)
  - Operation in low-power modes for lower noise operation
  - Asynchronous clock source for lower noise operation
  - Automatic compare with interrupt for less-than, or greater-than or equal-to, programmable value
  - On-chip temperature sensor
- Flexible timer/pulse-width modulators (FTM)
  - 16-bit Free-running counter or a counter with initial and final value. The counting can be up and unsigned, up and signed, or up-down and unsigned
  - Up to 6 channels, and each channel can be configured for input capture, output compare or edge-aligned PWM mode, all channels can be configured for center-aligned PWM mode
    - Channels can operate as pairs with equal outputs, pairs with complimentary outputs or independent channels (with independent outputs)
    - Each pair of channels can be combined to generate a PWM signal (with independent control of both edges of PWM signal)
    - Deadtime insertion is available for each complementary pair
  - The load of the FTM registers which have write buffer can be synchronized; write protection for critical registers
  - Generation of the triggers to ADC (hardware trigger)
  - A fault input for global fault control
  - Backwards compatible with TPM
- Timer/pulse width modulator (TPM)
  - 16-bit free-running or modulo up/down count operation
  - Two channels, each channel may be input capture, output compare, or edge-aligned PWM
  - One interrupt per channel plus terminal count interrupt
- Cyclic redundancy check (CRC) generator
  - High speed hardware CRC generator circuit using 16-bit shift register
  - CRC16-CCITT compliancy with $x^{16} + x^{12} + x^5 + 1$ polynomial
  - Error detection for all single, double, odd, and most multi-bit errors
  - Programmable initial seed value
- Analog comparators (ACMP)
  - Full rail to rail supply operation
  - Selectable interrupt on rising edge, falling edge, or either rising or falling edges of comparator output
  - Option to compare to fixed internal bandgap reference voltage
  - Option to allow comparator output to be visible on a pin, ACMPxO

Table 3. Orderable Part Number Summary

MCF51AC256ACPUE	MCF51AC256 ColdFire Microcontroller with CAN	256 / 32	64 LQFP	–40°C to 85°C
MCF51AC256BCPUE	MCF51AC256 ColdFire Microcontroller without CAN	256 / 32	64 LQFP	–40°C to 85°C
MCF51AC256BCFGE	MCF51AC256 ColdFire Microcontroller without CAN	256/32	44 LQFP	–40°C to 85°C
MCF51AC128ACFUE	MCF51AC128 ColdFire Microcontroller with CAN	128 / 32	64 QFP	–40°C to 85°C
MCF51AC128CCFUE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	64 QFP	–40°C to 85°C
MCF51AC128ACLKE	MCF51AC128 ColdFire Microcontroller with CAN	128 / 32	80 LQFP	–40°C to 85°C
MCF51AC128CCLKE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	80 LQFP	–40°C to 85°CC
MCF51AC128ACPUE	MCF51AC128 ColdFire Microcontroller with CAN	128 / 32	64 LQFP	–40°C to 85°C
MCF51AC128CCPUE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	64 LQFP	–40°C to 85°C
MCF51AC128CCFGE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	44 LQFP	–40°C to 85°C

1.5 Pinouts and Packaging

Figure 2 shows the pinout of the 80-pin LQFP.

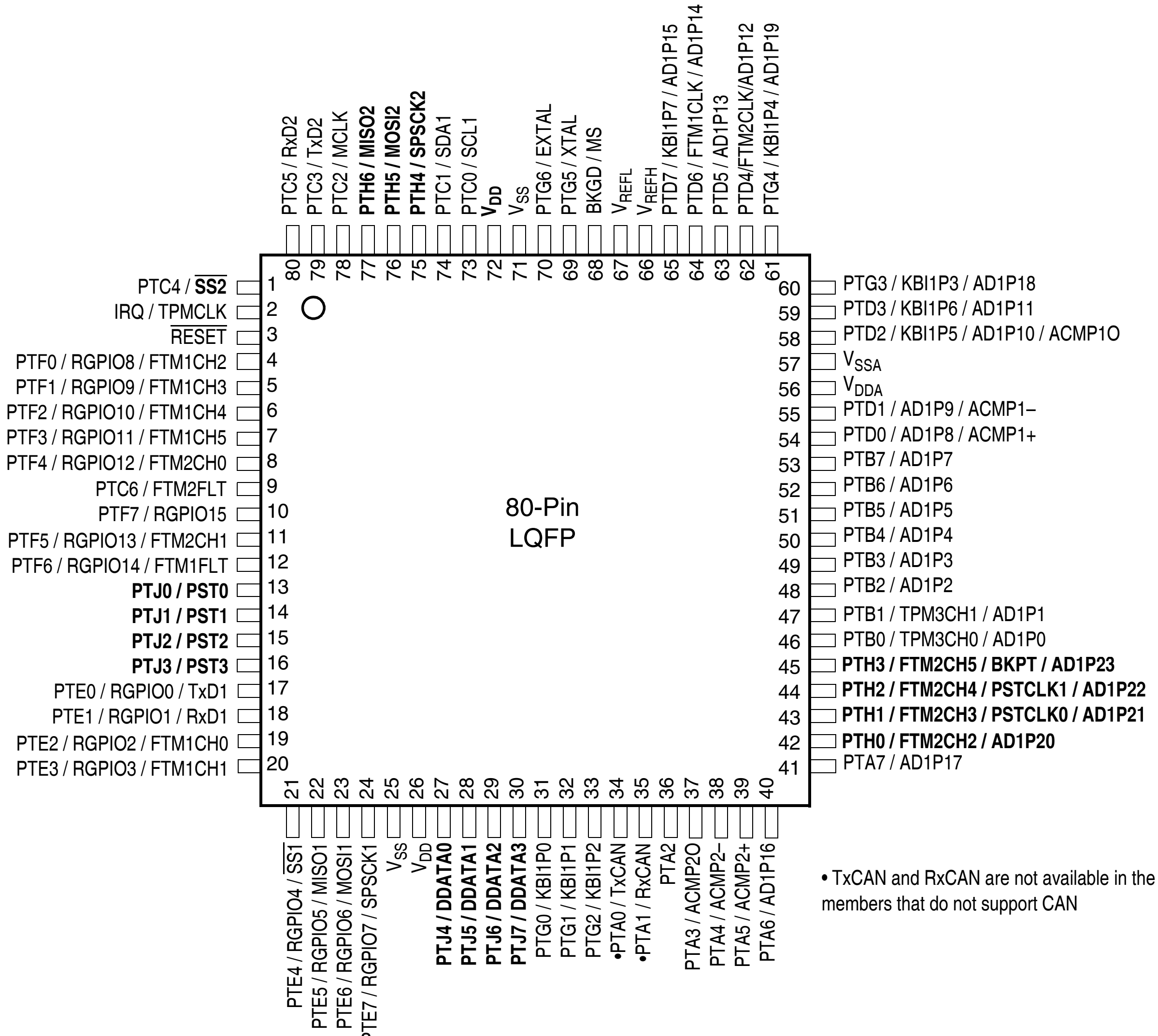


Figure 2. MCF51AC256 Series ColdFire Microcontroller 80-Pin LQFP

Figure 3 shows the pinout of the 64-pin LQFP and QFP.

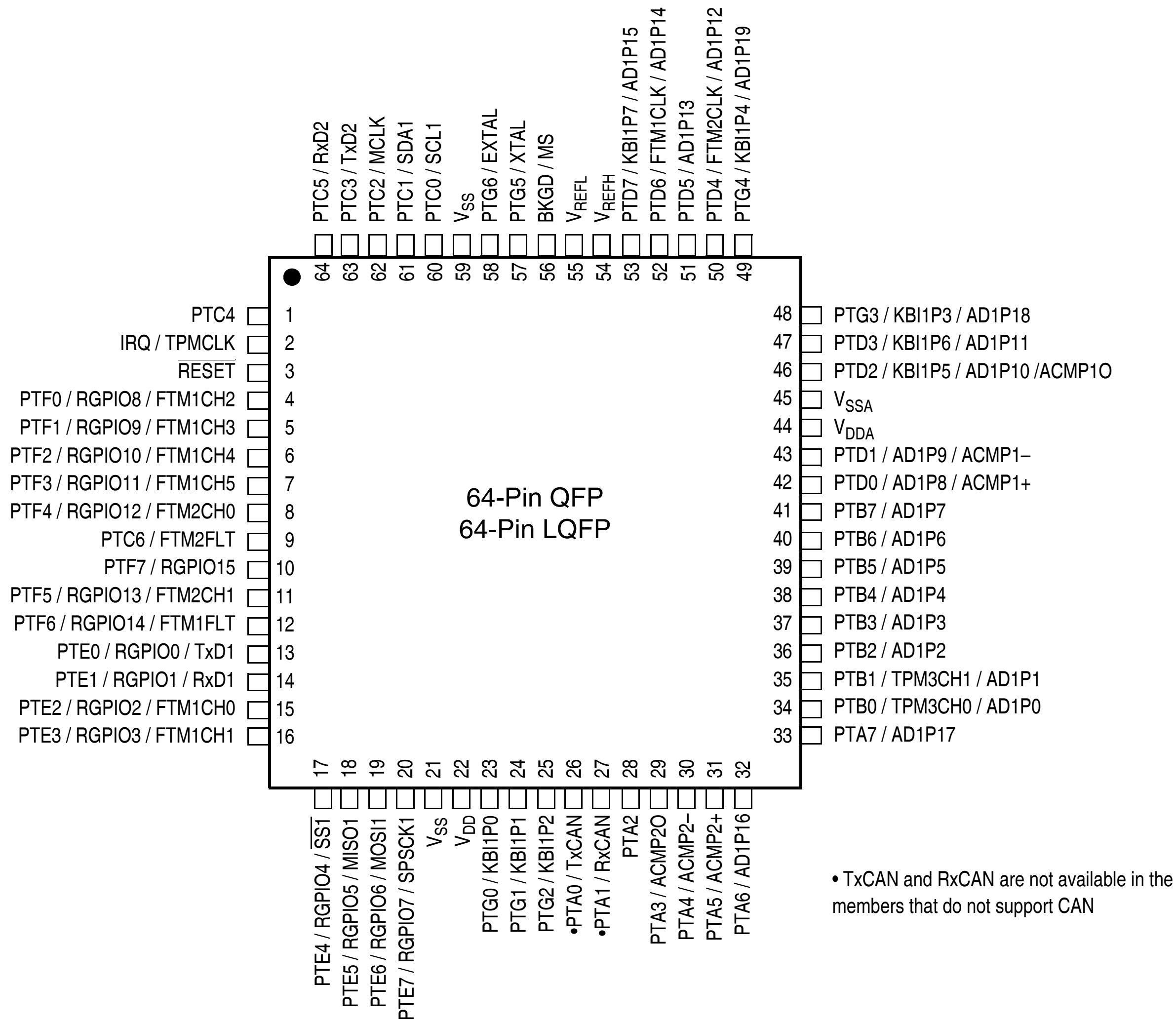


Figure 3. MCF51AC256 Series ColdFire Microcontroller 64-Pin QFP/LQFP

Figure 4 shows the pinout of the 44-pin LQFP.

Table 4. Pin Availability by Package Pin-Count (continued)

Pin Number			Lowest <-- Priority --> Highest			
80	**64**	**44**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**
8	8	6	PTF4	RGPIO12	FTM2CH0	
9	9	—	PTC6	FTM2FLT		
10	10	—	PTF7	RGPIO15		
11	11	7	PTF5	RGPIO13	FTM2CH1	
12	12	—	PTF6	RGPIO14	FTM1FLT	
13	—	—	PTJ0	PST0		
14	—	—	PTJ1	PST1		
15	—	—	PTJ2	PST2		
16	—	—	PTJ3	PST3		
17	13	8	PTE0	RGPIO0	TxD1	
18	14	9	PTE1	RGPIO1	RxD1	
19	15	10	PTE2	RGPIO2	FTM1CH0	
20	16	11	PTE3	RGPIO3	FTM1CH1	
21	17	12	PTE4	RGPIO4	$\overline{SS1}$	
22	18	13	PTE5	RGPIO5	MISO1	
23	19	14	PTE6	RGPIO6	MOSI1	
24	20	15	PTE7	RGPIO7	SPSCK1	
25	21	16	V_{SS}			
26	22	17	V_{DD}			
27	—	—	PTJ4	DDATA0		
28	—	—	PTJ5	DDATA1		
29	—	—	PTJ6	DDATA2		
30	—	—	PTJ7	DDATA3		
31	23	18	PTG0	KBI1P0		
32	24	19	PTG1	KBI1P1		
33	25	20	PTG2	KBI1P2		
34	26	21	PTA0	TxCAN[2]		
35	27	22	PTA1	RxCAN[3]		
36	28	—	PTA2			
37	29	—	PTA3	ACMP2O		
38	30	—	PTA4	ACMP2–		
39	31	—	PTA5	ACMP2+		
40	32	—	PTA6	AD1P16		
41	33	—	PTA7	AD1P17		
42	—	—	PTH0	FTM2CH2	AD1P20	
43	—	—	PTH1	FTM2CH3	PSTCLK0	AD1P21
44	—	—	PTH2	FTM2CH4	PSTCLK1	AD1P22
45	—	—	PTH3	FTM2CH5	BKPT	AD1P23
46	34	23	PTB0	TPM3CH0	AD1P0	
47	35	24	PTB1	TPM3CH1	AD1P1	
48	36	25	PTB2	AD1P2		

Table 6. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to 5.8	V
Input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1], [2], [3]	I_D	±25	mA
Maximum current into V_{DD}	I_{DD}	120	mA
Storage temperature	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low which would reduce overall power consumption.

2.3 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and it is user-determined rather than being controlled by the MCU design. In order to take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 7. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	–40 to 105	°C
Maximum junction temperature	T_J	150	°C
Thermal resistance [1,2,3,4] 80-pin LQFP 1s 2s2p 64-pin LQFP 1s 2s2p 64-pin QFP 1s 2s2p 44-pin LQFP 1s 2s2p	θ_{JA}	 51 38 59 41 50 36 67 45	°C/W

[1] Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance
[2] Junction to Ambient Natural Convection
[3] 1s — Single layer board, one signal layer
[4] 2s2p — Four layer board, 2 signal and 2 power layers

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \qquad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C
θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W
$P_D = P_{int} + P_{I/O}$
$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} \ll P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \qquad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \qquad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

2.4 Electrostatic Discharge (ESD) Protection Characteristics

Although damage from static discharge is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with CDF-AEC-Q00 Stress Test Qualification for Automotive Grade Integrated Circuits. (http://www.aecouncil.com/) This device was qualified to AEC-Q100 Rev E.

A device is considered to have failed if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete dc parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 8. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human body	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulse per pin	—	3	
Charge device model	Series resistance	R1	0	Ω
	Storage capacitance	C	0	pF
	Number of pulse per pin	—	3	—
Latch-up	Minimum input voltage limit	—	–2.5	V
	Maximum input voltage limit	—	7.5	V

Table 9. ESD and Latch-Up Protection Characteristics

Num	Rating	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	±2000	—	V
2	Charge device model (CDM)	V_{CDM}	±500	—	V
3	Latch-up current at T_A = 85 °C	I_{LAT}	±100	—	mA

2.5 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

Table 10. DC Characteristics

Num	C	Parameter	Symbol	Min	Typical[1]	Max	Unit
1	—	Operating voltage		2.7	—	5.5	V
2	P	Output high voltage — Low drive (PTxDSn = 0) 5 V, I_{Load} = –4 mA 3 V, I_{Load} = –2 mA 5 V, I_{Load} = –2 mA 3 V, I_{Load} = –1 mA	V_{OH}	 V_{DD} – 1.5 V_{DD} – 1.5 V_{DD} – 0.8 V_{DD} – 0.8	 — — — —	 — — — —	V
		Output high voltage — High drive (PTxDSn = 1) 5 V, I_{Load} = –15 mA 3 V, I_{Load} = –8 mA 5 V, I_{Load} = –8 mA 3 V, I_{Load} = –4 mA		 V_{DD} – 1.5 V_{DD} – 1.5 V_{DD} – 0.8 V_{DD} – 0.8	 — — — —	 — — — —	

Table 10. DC Characteristics (continued)

Num	C	Parameter	Symbol	Min	Typical[1]	Max	Unit
22	D	DC injection current[5 6 7 8] (single pin limit) $V_{IN} > V_{DD}$ $V_{IN} < V_{SS}$	I_{IC}	0 0	—	2 –0.2	mA
		DC injection current (Total MCU limit, includes sum of all stressed pins) $V_{IN} > V_{DD}$ $V_{IN} < V_{SS}$		0 0	—	25 –5	mA

1 Typical values are based on characterization data at 25°C unless otherwise stated.
2 Measured with $V_{In} = V_{DD}$ or V_{SS}.
3 Measured with $V_{In} = V_{SS}$.
4 Measured with $V_{In} = V_{DD}$.
5 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).
6 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.
7 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.
8 The $\overline{RESET}$ pin does not have a clamp diode to V_{DD}. Do not drive this pin above V_{DD}.

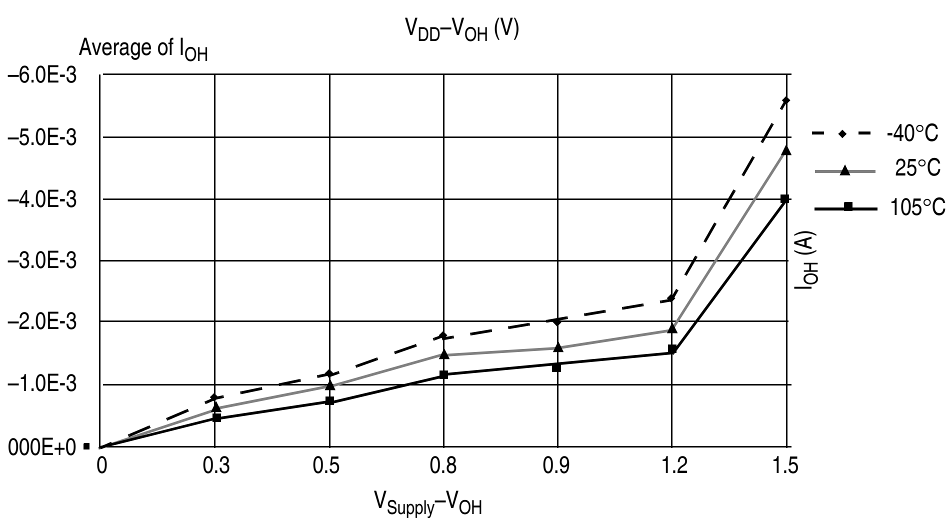


Figure 5. Typical I_{OH} vs. V_{DD}–V_{OH} at V_{DD} = 3 V (Low Drive, PTxDSn = 0)

Table 11. Supply Current Characteristics (continued)

Num	C	Parameter	Symbol	V_{DD} (V)	Typical[1]	Max[2]	Unit
5	C	Wait mode supply[3] current measured at (CPU clock = 2 MHz, f_{Bus} = 1 MHz)	WI_{DD}	5	1.3	2	mA
				3	1.29	2	
6	C	Wait mode supply[3] current measured at (CPU clock = 16 MHz, f_{Bus} = 8 MHz)		5	5.11	8	mA
				3	5.1	8	
7	C	Wait mode supply[3] current measured at (CPU clock = 50 MHz, f_{Bus} = 25 MHz)		5	15.24	25	mA
				3	15.2	25	
8	C	Stop2 mode supply current –40 °C 25 °C 120 °C	$S2I_{DD}$	5	1.40	2.5 2.5 200	µA
		–40 °C 25 °C 120 °C		3	1.16	2.5 2.5 200	µA
9	C	Stop3 mode supply current –40 °C 25 °C 120 °C	$S3I_{DD}$	5	1.60	2.5 2.5 220	µA
		–40 °C 25 °C 120 °C		3	1.35	2.5 2.5 220	µA
10	C	RTI adder to stop2 or stop3[3], 25 °C	$S23I_{DDRTI}$	5	300		nA
				3	300		nA
11	C	Adder to stop3 for oscillator enabled[4] (ERCLKEN =1 and EREFSTEN = 1)	$S3I_{DDOSC}$	5, 3	5		µA

1 Typicals are measured at 25 °C.

2 Values given here are preliminary estimates prior to completing characterization.

3 Most customers are expected to find that auto-wakeup from stop2 or stop3 can be used instead of the higher current wait mode.

4 Values given under the following conditions: low range operation (RANGE = 0), low power mode (HGO = 0).

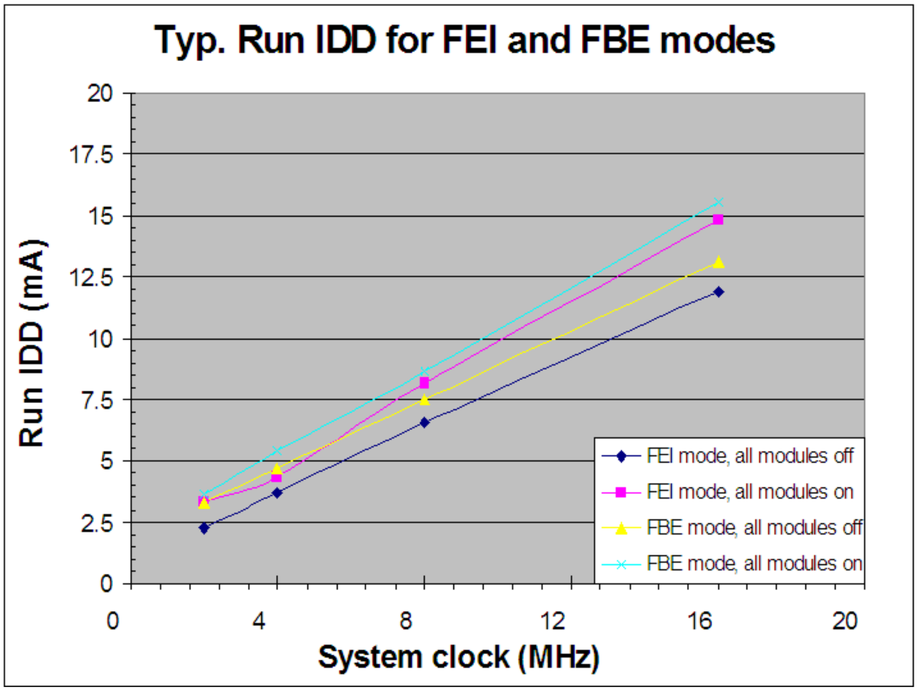
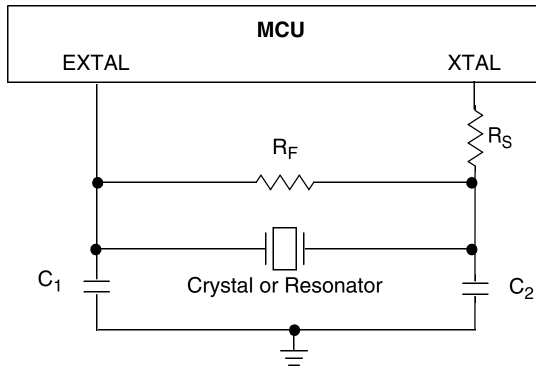


Figure 9. Typical Run I_{DD} vs. System Clock Freq. for FEI and FBE Modes

2.7 Analog Comparator (ACMP) Electricals

Table 12. Analog Comparator Electrical Specifications

Num	C	Rating	Symbol	Min	Typical	Max	Unit
1	—	Supply voltage	V_{DD}	2.7	—	5.5	V
2	T	Supply current (active)	I_{DDAC}	—	20	35	µA
3	D	Analog input voltage	V_{AIN}	V_{SS} – 0.3	—	V_{DD}	V
4	D	Analog input offset voltage	V_{AIO}	—	20	40	mV
5	D	Analog comparator hysteresis	V_H	3.0	6.0	20.0	mV
6	D	Analog input leakage current	I_{ALKG}	—	—	1.0	µA
7	D	Analog comparator initialization delay	t_{AINIT}	—	—	1.0	µs
8	P	Bandgap voltage reference factory trimmed at V_{DD} = 5.3248 V, Temp = 25 °C	V_{BG}	1.18	1.20	1.21	V



2.10 MCG Specifications

Table 16. MCG Frequency Specifications (Temperature Range = –40 to 105 °C Ambient)

Num	C	Rating		Symbol	Min	Typical[1]	Max	Unit
1	C	Internal reference frequency — factory trimmed at V_{DD} = 5 V and temperature = 25 °C		f_{int_ft}	—	32.768	—	kHz
2	C	Average internal reference frequency — untrimmed		f_{int_ut}	31.25	—	39.0625	kHz
3	T	Internal reference startup time		t_{irefst}	—	60	100	μs
4	C	DCO output frequency range — untrimmed [2]	Low range (DRS=00)	f_{dco_ut}	16	—	20	MHz
	C		Mid range (DRS=01)		32	—	40	
	C		High range (DRS=10)		48	—	60	
5	P	DCO output frequency[2] reference =32768Hz and DMX32 = 1	Low range (DRS=00)	f_{dco_DMX32}	—	16.82	—	MHz
	P		Mid range (DRS=01)		—	33.69	—	
	P		High range (DRS=10)		—	50.48	—	
6	D	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)		$\Delta f_{dco\_res\_t}$	—	±0.1	±0.2	$\%f_{dco}$
7	D	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)		$\Delta f_{dco\_res\_t}$	—	±0.2	±0.4	$\%f_{dco}$
8	D	Total deviation of trimmed DCO output frequency over voltage and temperature		Δf_{dco_t}	—	0.5 –1.0	±2	$\%f_{dco}$
9	D	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0–70 °C		Δf_{dco_t}	—	±0.5	±1	$\%f_{dco}$
10	D	FLL acquisition time[3]		$t_{fll\_acquire}$	—	—	1	ms
11	D	PLL acquisition time[4]		$t_{pll\_acquire}$	—	—	1	ms
12	D	Long term jitter of DCO output clock (averaged over 2ms interval) [5]		C_{Jitter}	—	0.02	0.2	$\%f_{dco}$
13	D	VCO operating frequency		f_{vco}	7.0	—	55.0	MHz
16	D	Jitter of PLL output clock measured over 625 ns[6]		$f_{pll\_jitter\_625ns}$	—	0.566[6]	—	$\%f_{pll}$
17	D	Lock entry frequency tolerance [7]		D_{lock}	±1.49	—	±2.98	%

Table 16. MCG Frequency Specifications (continued)(Temperature Range = –40 to 105 °C Ambient)

Num	C	Rating	Symbol	Min	Typical[1]	Max	Unit
18	D	Lock exit frequency tolerance [8]	D_{unl}	±4.47	—	±5.97	%
19	D	Lock time — FLL	t_{fll_lock}	—	—	$t_{fll\_acquire}$+ 1075(1/f_{int_t})	s
20	D	Lock time — PLL	t_{pll_lock}	—	—	$t_{pll\_acquire}$+ 1075(1/f_{pll_ref})	s
21	D	Loss of external clock minimum frequency — RANGE = 0	f_{loc_low}	(3/5) × f_{int}	—	—	kHz

1 Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2 The resulting bus clock frequency must not exceed the maximum specified bus clock frequency of the device.
3 This specification applies when the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
4 This specification applies when the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
5 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.
6 625 ns represents 5 time quanta for CAN applications, under worst case conditions of 8 MHz CAN bus clock, 1 Mbps CAN bus speed, and 8 time quanta per bit for bit time settings. 5 time quanta is the minimum time between a synchronization edge and the sample point of a bit using 8 time quanta per bit.
7 Below D_{lock} minimum, the MCG enters lock. Above D_{lock} maximum, the MCG will not enter lock. But if the MCG is already in lock, then the MCG may stay in lock.
8 Below D_{unl} minimum, the MCG will not exit lock if already in lock. Above D_{unl} maximum, the MCG is guaranteed to exit lock.

2.11 AC Characteristics

This section describes ac timing characteristics for each peripheral system.

2.11.2 Timer (TPM/FTM) Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 18. TPM/FTM Input Timing

NUM	C	Function	Symbol	Min	Max	Unit
1	—	External clock frequency	f_{TPMext}	DC	$f_{Bus}/4$	MHz
2	—	External clock period	t_{TPMext}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

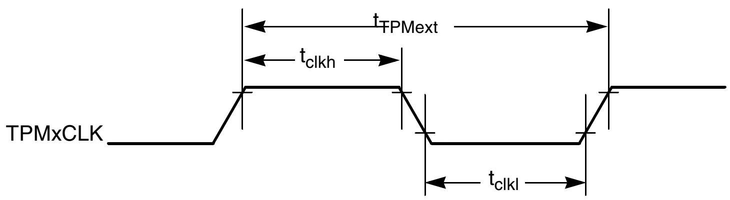


Figure 13. Timer External Clock

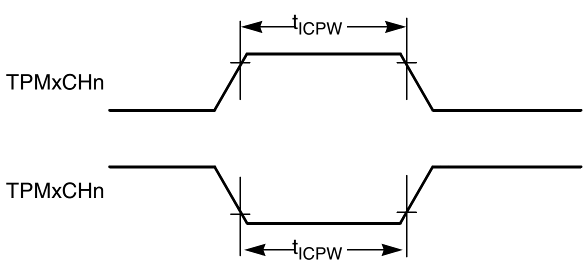


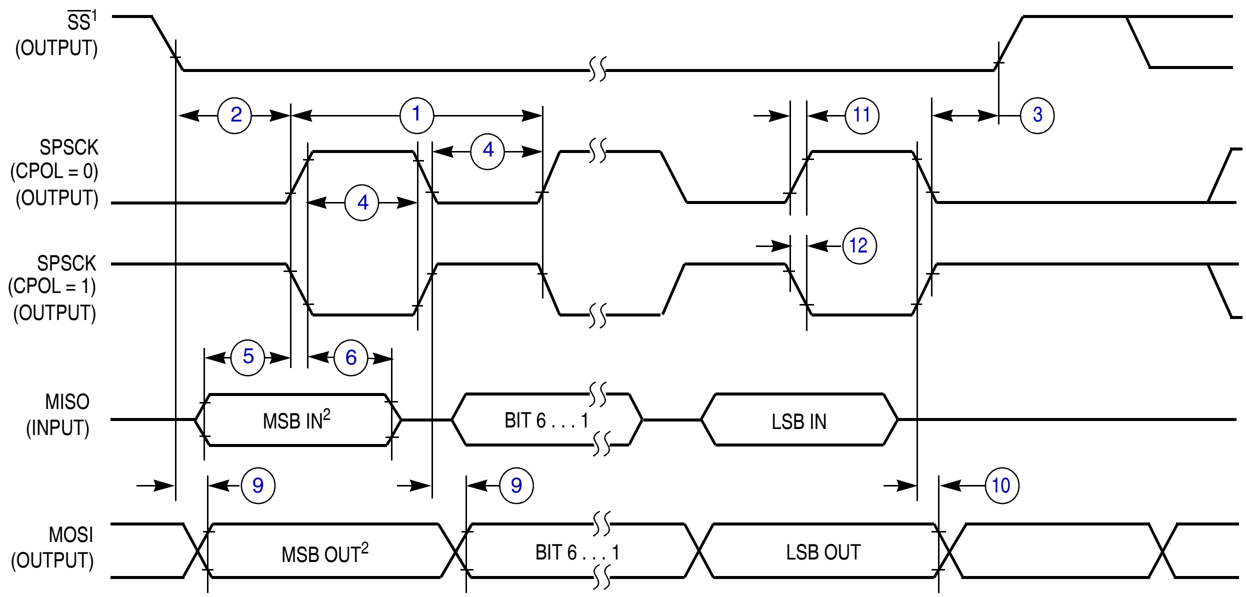
Figure 14. Timer Input Capture Pulse

2.11.3 MSCAN

Table 19. MSCAN Wake-Up Pulse Characteristics

Num	C	Parameter	Symbol	Min	Typical[1]	Max	Unit
1	D	MSCAN wake-up dominant pulse filtered	t_{WUP}	—	—	2	µs
2	D	MSCAN wake-up dominant pulse pass	t_{WUP}	5	—	5	µs

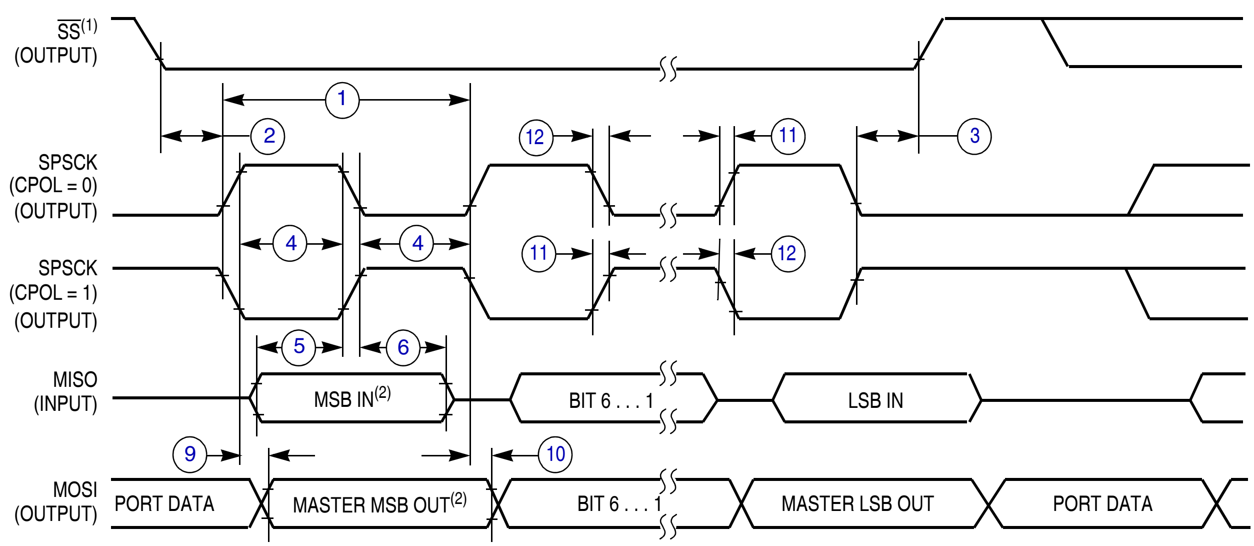
[1] Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.



NOTES:

1. SS output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

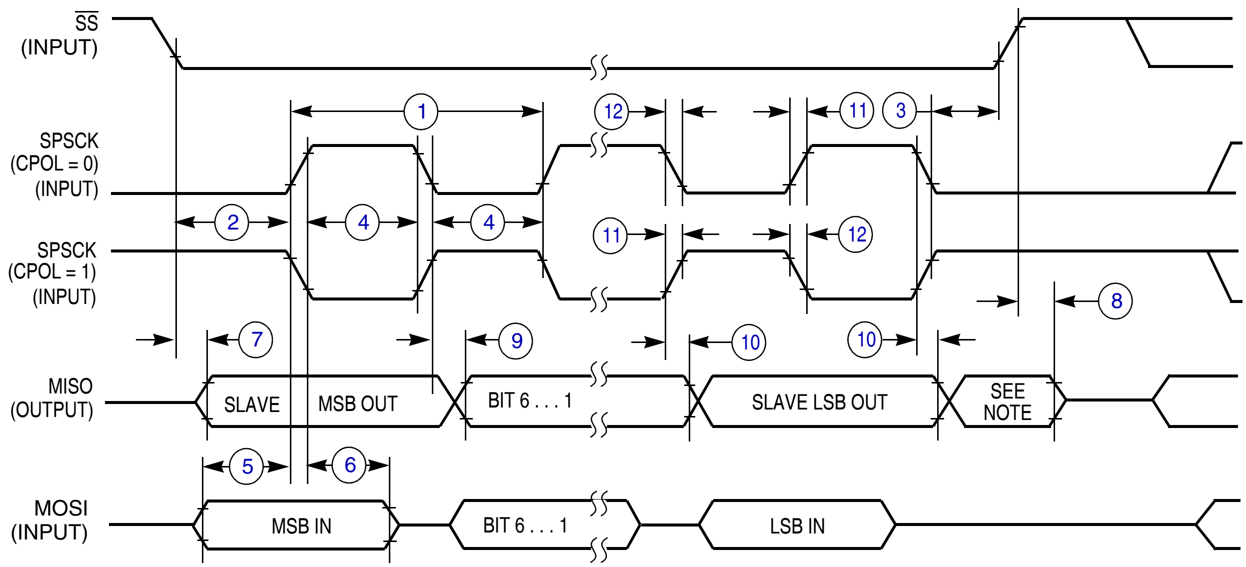
Figure 15. SPI Master Timing (CPHA = 0)



NOTES:

1. SS output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

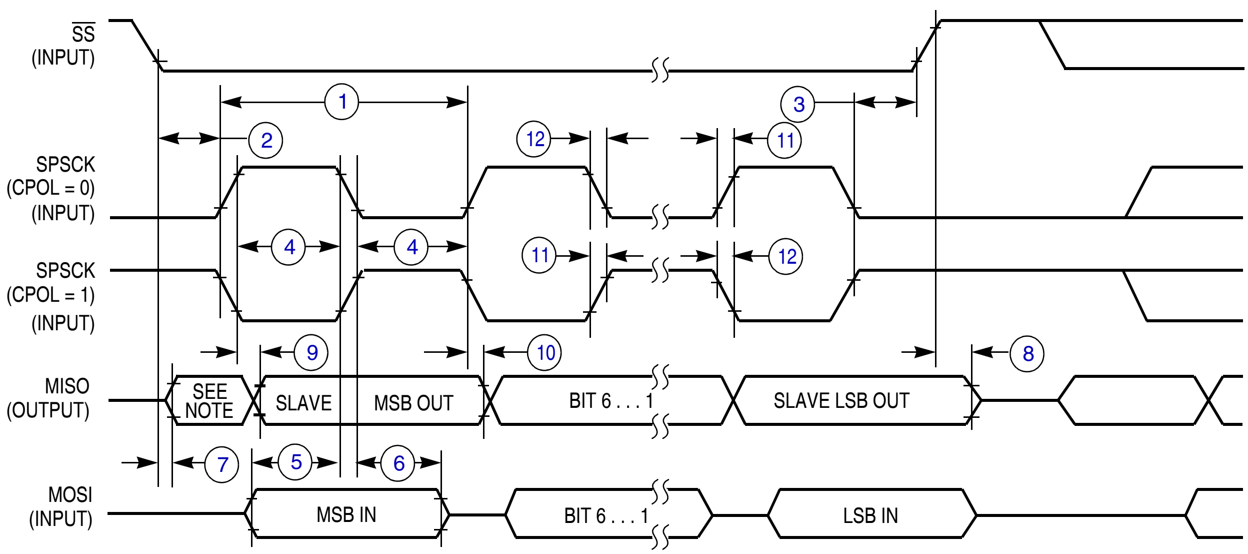
Figure 16. SPI Master Timing (CPHA =1)



NOTE:

1. Not defined but normally MSB of character just received

Figure 17. SPI Slave Timing (CPHA = 0)



NOTE:

1. Not defined but normally LSB of character just received

Figure 18. SPI Slave Timing (CPHA = 1)

2.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the Flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see Chapter 4, “Memory.”

Table 21. Flash Characteristics

Num	C	Characteristic	Symbol	Min	Typical[1]	Max	Unit
1	—	Supply voltage for program/erase	$V_{prog/erase}$	2.7	—	5.5	V
2	—	Supply voltage for read operation	V_{Read}	2.7	—	5.5	V
3	—	Internal FCLK frequency[2]	f_{FCLK}	150	—	200	kHz
4	—	Internal FCLK period (1/FCLK)	t_{Fcyc}	5	—	6.67	μs
5	—	Byte program time (random location)[2]	t_{prog}	9			t_{Fcyc}
6	—	Byte program time (burst mode)[2]	t_{Burst}	4			t_{Fcyc}
7	—	Page erase time[3]	t_{Page}	4000			t_{Fcyc}
8	—	Mass erase time[2]	t_{Mass}	20,000			t_{Fcyc}
9	C	Program/erase endurance[4] T_L to T_H = –40 °C to 105 °C T = 25 °C	—	 10,000 —	 — 100,000	 — —	cycles
10	C	Data retention[5]	t_{D_ret}	15	100	—	years

1 Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.
2 The frequency of this clock is controlled by a software setting.
3 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.
4 **Typical endurance for flash** was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale Semiconductor defines typical endurance, please refer to Engineering Bulletin EB619/D, *Typical Endurance for Nonvolatile Memory*.
5 **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale Semiconductor defines typical data retention, please refer to Engineering Bulletin EB618/D, *Typical Data Retention for Nonvolatile Memory.*

2.14 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

2.14.1 Radiated Emissions

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM Cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (North and East). For more detailed information concerning the evaluation results, conditions and setup, please refer to the EMC Evaluation Report for this device.

4 Revision History

Table 23. Revision History

Revision	Description
1	Initial published
2	Updated ADC channels, Item 1, 4-5 on Table 2.10
3	Completed all theTBDs. Changed RTC to RTI in Figure 1. Corrected the block diagram. Changed V_{DDAD} to V_{DDA}, V_{SSAD} to V_{SSA}. Added charge device model data and removed machine data in Table 8. Updated the specifications of V_{LVDH}, V_{LVDL}, V_{LVWH} and V_{LVWL} in Table 10. Updated $S2I_{DD}$, $S3I_{DD}$ in Table 11. Added C column in Table 14. Updated f_{dco_DMX32} in Table 16.
4	Corrected the expansion of SPI to serial peripheral interface.
5	Updated V_{LVDL} in the Table 10. Updated RI_{DD} in the Table 11.
6	Updated V_{LVDH}, V_{LVDL}, V_{LVWH} and V_{LVWL} in the Table 10. Added LPO on the Figure 1 and LPO features in the Section 1.3, “Features.”
7	Added 44-pin LQFP package information for AC256 and AC128.