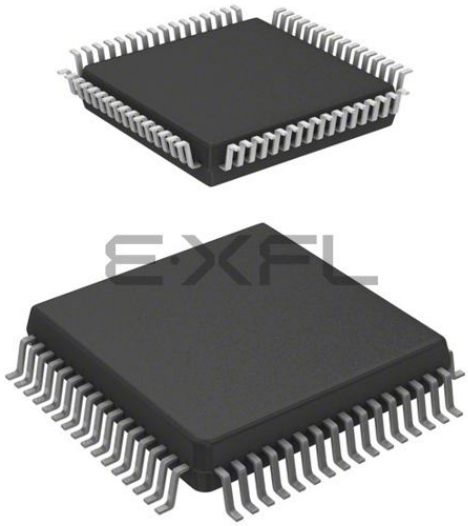

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	LVD, PWM, WDT
Number of I/O	54
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 20x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-QFP
Supplier Device Package	64-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf51ac256avfue

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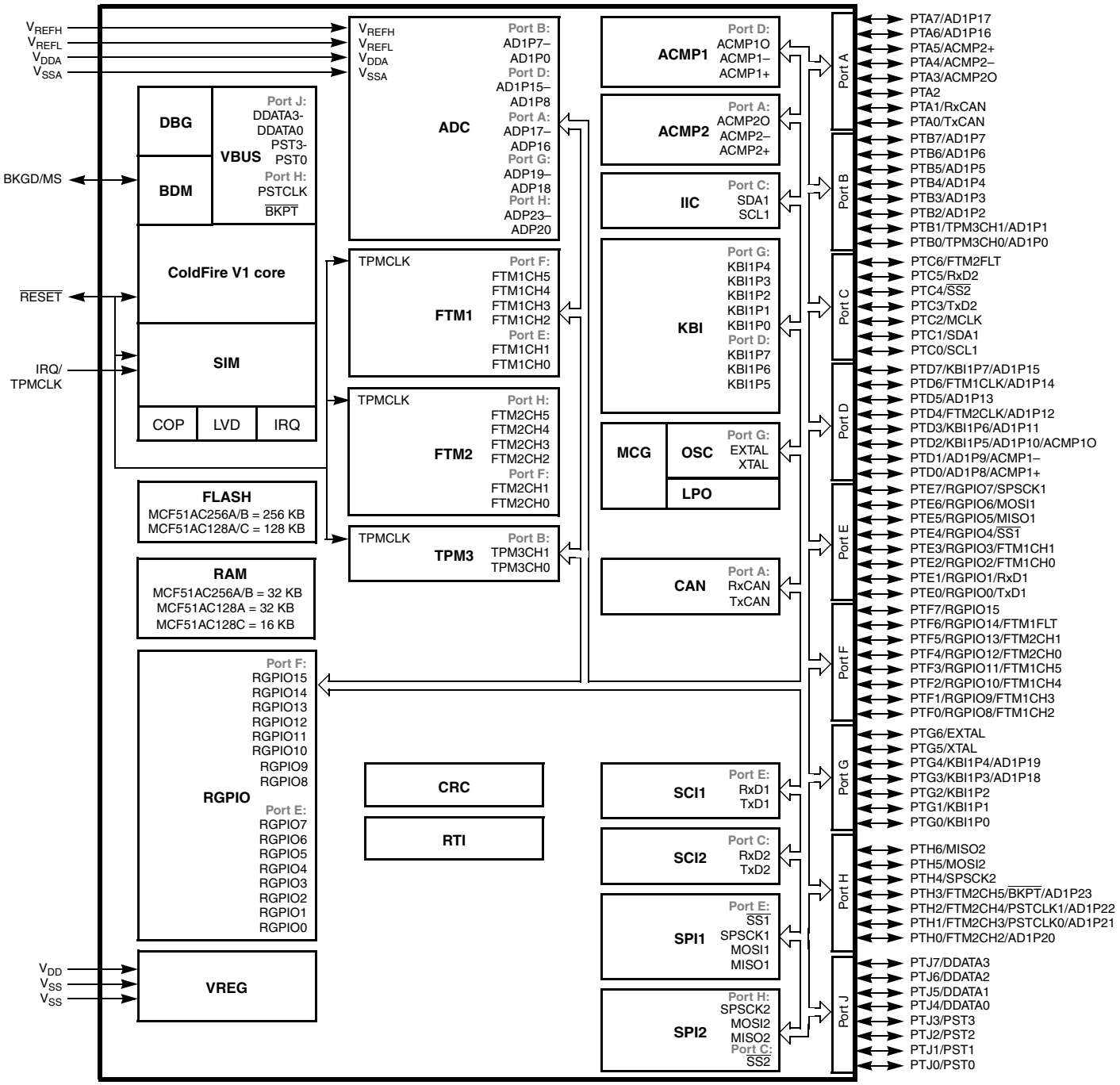


Figure 1. MCF51AC256 Series Block Diagram

1.3 Features

Table 2 describes the functional units of the MCF51AC256 series.

Table 2. MCF51AC256 Series Functional Units

Functional Unit	Function
CF1 Core (V1 ColdFire core)	Executes programs and interrupt handlers
BDM (background debug module)	Provides single pin debugging interface (part of the V1 ColdFire core)
DBG (debug)	Provides debugging and emulation capabilities (part of the V1 ColdFire core)
VBUS (debug visibility bus)	Allows for real-time program traces (part of the V1 ColdFire core)
SIM (system integration module)	Controls resets and chip level interfaces between modules
Flash (flash memory)	Provides storage for program code, constants and variables
RAM (random-access memory)	Provides storage for program variables
RGPIO (rapid general-purpose input/output)	Allows for I/O port access at CPU clock speeds
VREG (voltage regulator)	Controls power management across the device
COP (computer operating properly)	Monitors a countdown timer and generates a reset if the timer is not regularly reset by the software
LVD (low-voltage detect)	Monitors internal and external supply voltage levels, and generates a reset or interrupt when the voltages are too low
CF1_INTC (interrupt controller)	Controls and prioritizes all device interrupts
ADC (analog-to-digital converter)	Measures analog voltages at up to 12 bits of resolution
FTM1, FTM2 (flexible timer/pulse-width modulators)	Provides a variety of timing-based features
TPM3 (timer/pulse-width modulator)	Provides a variety of timing-based features
CRC (cyclic redundancy check)	Accelerates computation of CRC values for ranges of memory
ACMP1, ACMP2 (analog comparators)	Compares two analog inputs
IIC (inter-integrated circuit)	Supports standard IIC communications protocol
KBI (keyboard interrupt)	Provides pin interrupt capabilities
MCG (multipurpose clock generator)	Provides clocking options for the device, including a phase-locked loop (PLL) and frequency-locked loop (FLL) for multiplying slower reference clock sources
OSC (crystal oscillator)	Allows a crystal or ceramic resonator to be used as the system clock source or reference clock for the PLL or FLL
LPO (low-power oscillator)	Provides a second clock source for COP and RTI.
CAN (controller area network)	Supports standard CAN communications protocol
SCI1, SCI2 (serial communications interfaces)	Serial communications UARTs capable of supporting RS-232 and LIN protocols
SPI1 (8-bit serial peripheral interfaces)	Provides 8-bit 4-pin synchronous serial interface
SPI2 (16-bit serial peripheral interfaces)	Provides 16-bit 4-pin synchronous serial interface with FIFO

1.3.1 Feature List

- 32-bit Version 1 ColdFire® central processor unit (CPU)
  - Up to 50.33 MHz at 2.7 V – 5.5 V
  - Provide 0.94 Dhrystone 2.1 DMIPS per MHz performance when running from internal RAM (0.76 DMIPS per MHz when running from flash)
  - Implements instruction set revision C (ISA_C)
- On-chip memory
  - Up to 256 KB flash memory read/program/erase over full operating voltage and temperature
  - Up to 32 KB static random access memory (SRAM)
  - Security circuitry to prevent unauthorized access to SRAM and flash contents
- Power-Saving Modes
  - Three low-power stop plus wait modes
  - Peripheral clock enable register can disable clocks to unused modules, reducing currents; allows clocks to remain enabled to specific peripherals in stop3 mode
- System protection features
  - Watchdog computer operating properly (COP) reset with options to run from independent LPO clock or bus clock
  - Low-voltage detection with reset or interrupt
  - Illegal opcode and illegal address detection with programmable reset or exception response
  - Flash block protection
- Debug support
  - Single-wire background debug interface
  - Real-time debug support, with 6 hardware breakpoints (4 PC, 1 address pair and 1 data) that can be configured into a 1- or 2-level trigger
  - On-chip trace buffer provides programmable start/stop recording conditions plus support for continuous or PC-profiling modes
  - Support for real-time program (and optional partial data) trace using the debug visibility bus
- V1 ColdFire interrupt controller (CF1_INTC)
  - Support of 40 peripheral I/O interrupt requests plus seven software (one per level) interrupt requests
  - Fixed association between interrupt request source and level plus priority, up to two requests can be remapped to the highest maskable level + priority
  - Unique vector number for each interrupt source
  - Support for service routine interrupt acknowledge (software IACK) read cycles for improved system performance
- Multipurpose clock generator (MCG)
  - Oscillator (XOSC); loop-control Pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
  - LPO clock as an optional independent clock source for COP and RTI
  - FLL/PLL controlled by internal or external reference

- Inter-integrated circuit (IIC)
  - Compatible with IIC bus standard
  - Multi-master operation
  - Software programmable for one of 64 different serial clock frequencies
  - Interrupt driven byte-by-byte data transfer
  - Arbitration lost interrupt with automatic mode switching from master to slave
  - Calling address identification interrupt
  - Bus busy detection
  - 10-bit address extension
- Controller area network (CAN)
  - Implementation of the CAN protocol — Version 2.0A/B
    - Standard and extended data frames
    - Zero to eight bytes data length
    - Programmable bit rate up to 1 Mbps
    - Support for remote frames
  - Five receive buffers with FIFO storage scheme
  - Three transmit buffers with internal prioritization using a “local priority” concept
  - Flexible maskable identifier filter supports two full-size (32-bit) extended identifier filters, four 16-bit filters, or eight 8-bit filters
  - Programmable wakeup functionality with integrated low-pass filter
  - Programmable loopback mode supports self-test operation
  - Programmable listen-only mode for monitoring of CAN bus
  - Programmable bus-off recovery functionality
  - Separate signalling and interrupt capabilities for all CAN receiver and transmitter error states (warning, error passive, bus-off)
  - Internal timer for time-stamping of received and transmitted messages
- Serial communications interfaces (SCI)
  - Full-duplex, standard non-return-to-zero (NRZ) format
  - Double-buffered transmitter and receiver with separate enables
  - Programmable baud rates (13-bit modulo divider)
  - Interrupt-driven or polled operation
  - Hardware parity generation and checking
  - Programmable 8-bit or 9-bit character length
  - Receiver wakeup by idle-line or address-mark
  - Optional 13-bit break character generation / 11-bit break character detection
  - Selectable transmitter output polarity
- Serial peripheral interfaces (SPI)
  - Master or slave mode operation
  - Full-duplex or single-wire bidirectional option
  - Programmable transmit bit rate

— Double-buffered transmit and receive
— Serial clock phase and polarity options
— Slave select output
— Selectable MSB-first or LSB-first shifting
— 16-bit and FIFO operations in SPI2

- Input/Output
  — 69 GPIOs
  — 8 keyboard interrupt pins with selectable polarity
  — Hysteresis and configurable pull-up device on all input pins; Configurable slew rate and drive strength on all output pins
  — 16-bits Rapid GPIO pins connected to the processor's local 32-bit platform bus with set, clear, and faster toggle functionality

1.4 Part Numbers

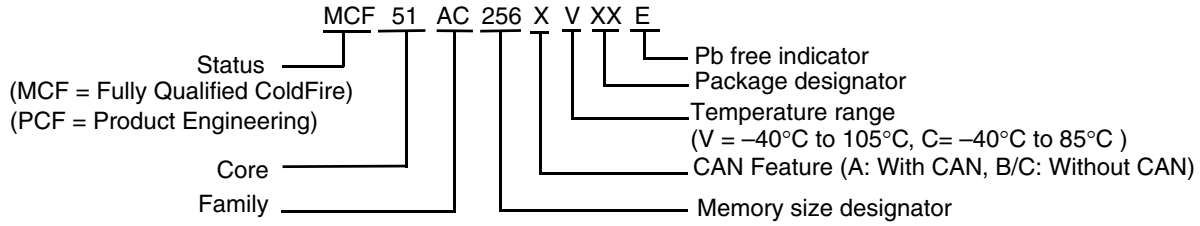


Table 3. Orderable Part Number Summary

Freescale Part Number	Description	Flash / SRAM (Kbytes)	Package	Temperature
MCF51AC256AVFUE	MCF51AC256 ColdFire Microcontroller with CAN	256 / 32	64 QFP	–40°C to 105°C
MCF51AC256BVFUE	MCF51AC256 ColdFire Microcontroller without CAN	256 / 32	64 QFP	–40°C to 105°C
MCF51AC256AVLKE	MCF51AC256 ColdFire Microcontroller with CAN	256 / 32	80 LQFP	–40°C to 105°C
MCF51AC256BVLKE	MCF51AC256 ColdFire Microcontroller without CAN	256 / 32	80 LQFP	–40°C to 105°C
MCF51AC256AVPUE	MCF51AC256 ColdFire Microcontroller with CAN	256 / 32	64 LQFP	–40°C to 105°C
MCF51AC256BVPUE	MCF51AC256 ColdFire Microcontroller without CAN	256 / 32	64 LQFP	–40°C to 105°C
MCF51AC128AVFUE	MCF51AC128 ColdFire Microcontroller with CAN	128 / 32	64 QFP	–40°C to 105°C
MCF51AC128CVFUE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	64 QFP	–40°C to 105°C
MCF51AC128AVLKE	MCF51AC128 ColdFire Microcontroller with CAN	128 / 32	80 LQFP	–40°C to 105°C
MCF51AC128CVLKE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	80 LQFP	–40°C to 105°C
MCF51AC128AVPUE	MCF51AC128 ColdFire Microcontroller with CAN	128 / 32	64 LQFP	–40°C to 105°C
MCF51AC128CVPUE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	64 LQFP	–40°C to 105°C
MCF51AC256ACFUE	MCF51AC256 ColdFire Microcontroller with CAN	256 / 32	64 QFP	–40°C to 85°C
MCF51AC256BCFUE	MCF51AC256 ColdFire Microcontroller without CAN	256 / 32	64 QFP	–40°C to 85°C
MCF51AC256ACLKE	MCF51AC256 ColdFire Microcontroller with CAN	256 / 32	80 LQFP	–40°C to 85°C
MCF51AC256BCLKE	MCF51AC256 ColdFire Microcontroller without CAN	256 / 32	80 LQFP	–40°C to 85°C

1.5 Pinouts and Packaging

Figure 2 shows the pinout of the 80-pin LQFP.

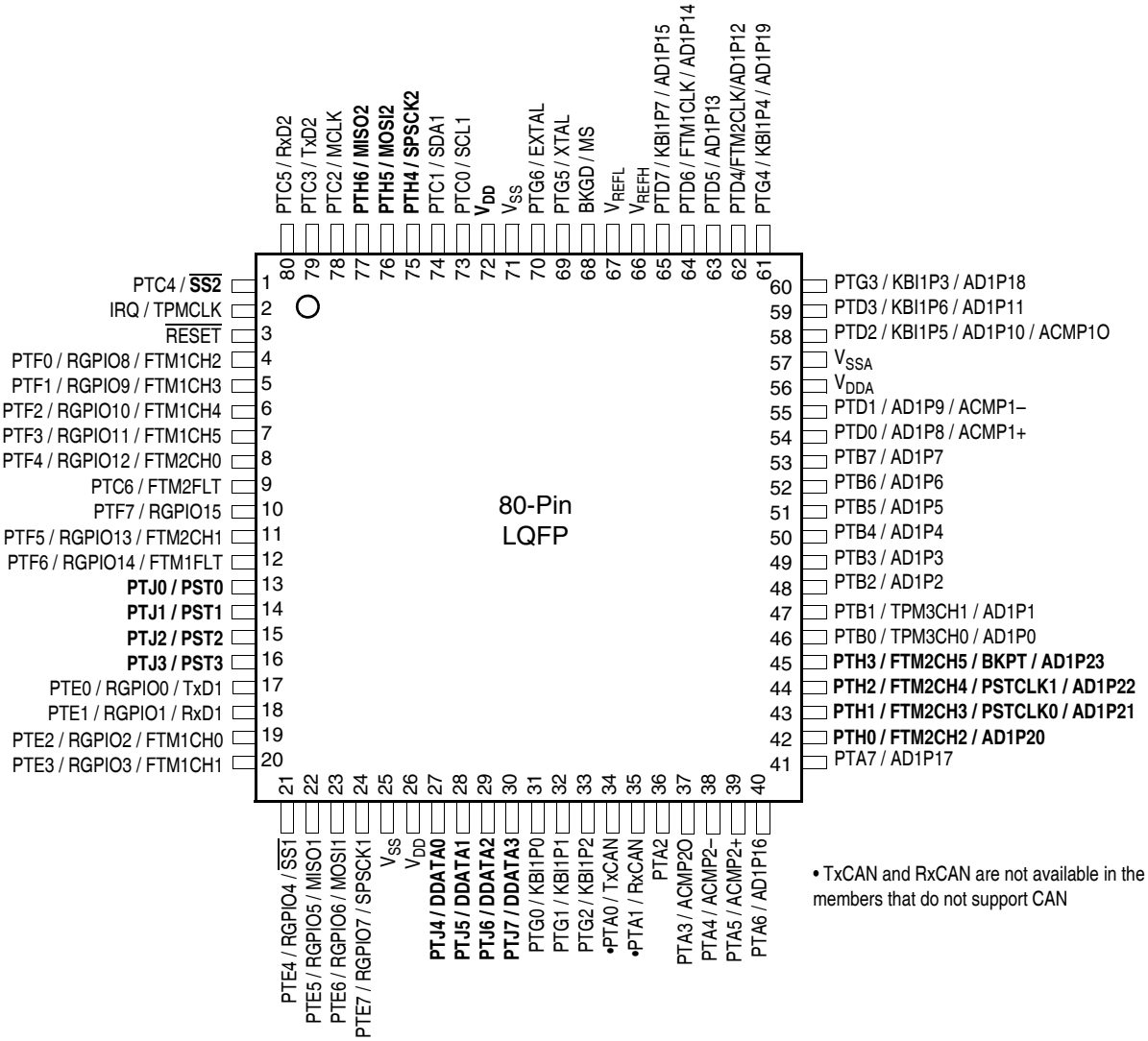


Figure 2. MCF51AC256 Series ColdFire Microcontroller 80-Pin LQFP

Figure 3 shows the pinout of the 64-pin LQFP and QFP.

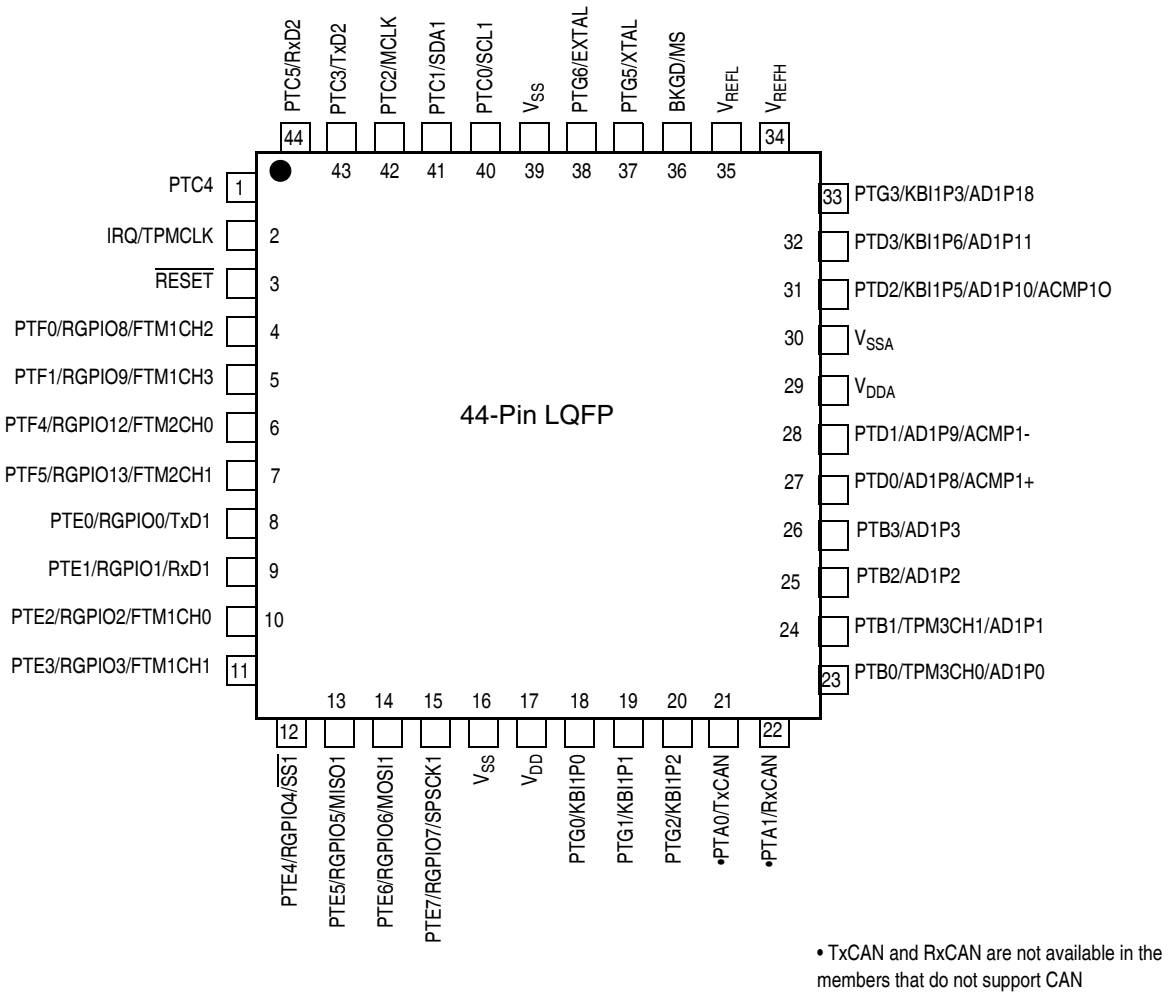


Figure 4. MCF51AC256 Series ColdFire Microcontroller 44-Pin LQFP

Table 4 shows the package pin assignments.

Table 4. Pin Availability by Package Pin-Count

Pin Number			Lowest <-- Priority --> Highest			
80	64	44	Port Pin	Alt 1	Alt 2	Alt 3
1	1	1	PTC4	$\overline{SS2}$		
2	2	2	IRQ	TPMCLK[1]		
3	3	3	$\overline{RESET}$			
4	4	4	PTF0	RGPIO8	FTM1CH2	
5	5	5	PTF1	RGPIO9	FTM1CH3	
6	6	—	PTF2	RGPIO10	FTM1CH4	
7	7	—	PTF3	RGPIO11	FTM1CH5	

Table 4. Pin Availability by Package Pin-Count (continued)

Pin Number			Lowest <-- Priority --> Highest			
80	64	44	Port Pin	Alt 1	Alt 2	Alt 3
8	8	6	PTF4	RGPIO12	FTM2CH0	
9	9	—	PTC6	FTM2FLT		
10	10	—	PTF7	RGPIO15		
11	11	7	PTF5	RGPIO13	FTM2CH1	
12	12	—	PTF6	RGPIO14	FTM1FLT	
13	—	—	PTJ0	PST0		
14	—	—	PTJ1	PST1		
15	—	—	PTJ2	PST2		
16	—	—	PTJ3	PST3		
17	13	8	PTE0	RGPIO0	TxD1	
18	14	9	PTE1	RGPIO1	RxD1	
19	15	10	PTE2	RGPIO2	FTM1CH0	
20	16	11	PTE3	RGPIO3	FTM1CH1	
21	17	12	PTE4	RGPIO4	$\overline{SS1}$	
22	18	13	PTE5	RGPIO5	MISO1	
23	19	14	PTE6	RGPIO6	MOSI1	
24	20	15	PTE7	RGPIO7	SPSCK1	
25	21	16	V_{SS}			
26	22	17	V_{DD}			
27	—	—	PTJ4	DDATA0		
28	—	—	PTJ5	DDATA1		
29	—	—	PTJ6	DDATA2		
30	—	—	PTJ7	DDATA3		
31	23	18	PTG0	KBI1P0		
32	24	19	PTG1	KBI1P1		
33	25	20	PTG2	KBI1P2		
34	26	21	PTA0	TxCAN[2]		
35	27	22	PTA1	RxCAN[3]		
36	28	—	PTA2			
37	29	—	PTA3	ACMP2O		
38	30	—	PTA4	ACMP2–		
39	31	—	PTA5	ACMP2+		
40	32	—	PTA6	AD1P16		
41	33	—	PTA7	AD1P17		
42	—	—	PTH0	FTM2CH2	AD1P20	
43	—	—	PTH1	FTM2CH3	PSTCLK0	AD1P21
44	—	—	PTH2	FTM2CH4	PSTCLK1	AD1P22
45	—	—	PTH3	FTM2CH5	BKPT	AD1P23
46	34	23	PTB0	TPM3CH0	AD1P0	
47	35	24	PTB1	TPM3CH1	AD1P1	
48	36	25	PTB2	AD1P2		

2 Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the MCF51AC256 microcontroller, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. These specifications will, however, be met for production silicon. Finalized specifications will be published after complete characterization and device qualifications have been completed.

NOTE

The parameters specified in this data sheet supersede any values found in the module specifications.

2.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 5. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

2.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 6 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}).

Table 6. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to 5.8	V
Input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	±25	mA
Maximum current into V_{DD}	I_{DD}	120	mA
Storage temperature	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low which would reduce overall power consumption.

2.3 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and it is user-determined rather than being controlled by the MCU design. In order to take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 7. Thermal Characteristics

Rating		Symbol	Value	Unit
Operating temperature range (packaged)		T_A	–40 to 105	°C
Maximum junction temperature		T_J	150	°C
Thermal resistance [1,2,3,4]				
80-pin LQFP				
	1s		51	
	2s2p		38	
64-pin LQFP				
	1s		59	
	2s2p	θ_{JA}	41	°C/W
64-pin QFP				
			50	
	1s		36	
	2s2p			
44-pin LQFP				
	1s		67	
	2s2p		45	

Table 10. DC Characteristics (continued)

Num	C	Parameter	Symbol	Min	Typical[1]	Max	Unit
22	D	DC injection current[5 6 7 8] (single pin limit) $V_{IN} > V_{DD}$ $V_{IN} < V_{SS}$	I_{IC}	 0 0	—	 2 –0.2	mA
		DC injection current (Total MCU limit, includes sum of all stressed pins) $V_{IN} > V_{DD}$ $V_{IN} < V_{SS}$		 0 0	—	 25 –5	mA

1 Typical values are based on characterization data at 25°C unless otherwise stated.

2 Measured with $V_{In} = V_{DD}$ or V_{SS}.

3 Measured with $V_{In} = V_{SS}$.

4 Measured with $V_{In} = V_{DD}$.

5 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

6 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

7 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

8 The $\overline{\text{RESET}}$ pin does not have a clamp diode to V_{DD}. Do not drive this pin above V_{DD}.

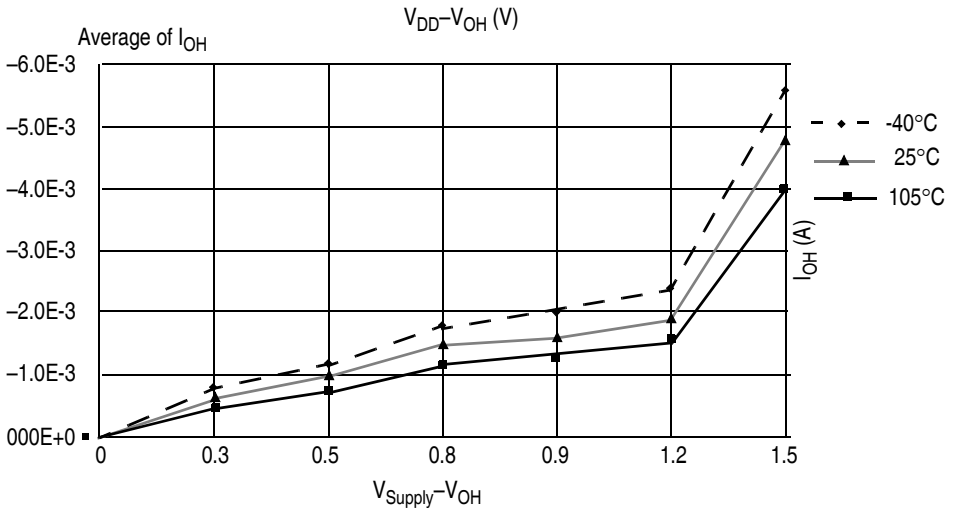


Figure 5. Typical I_{OH} vs. V_{DD}–V_{OH} at V_{DD} = 3 V (Low Drive, PTxDSn = 0)

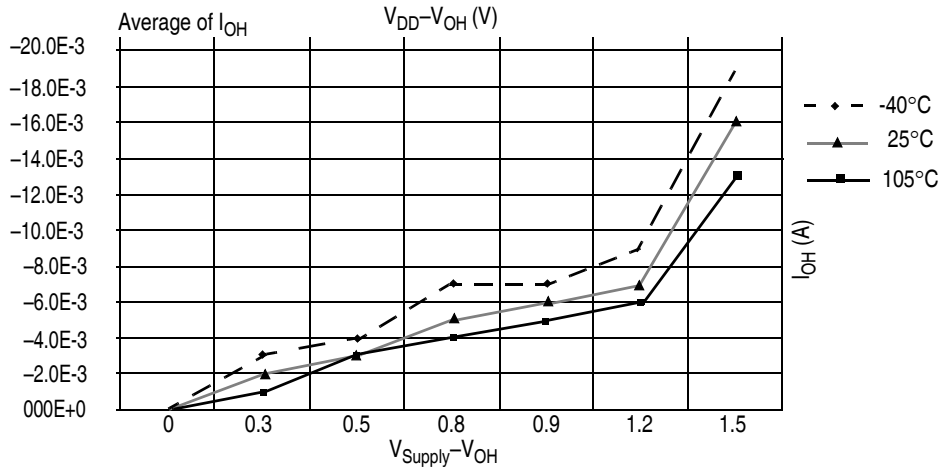


Figure 6. Typical I_{OH} vs. $V_{DD}–V_{OH}$ at V_{DD} = 3 V (High Drive, PTxDSn = 1)

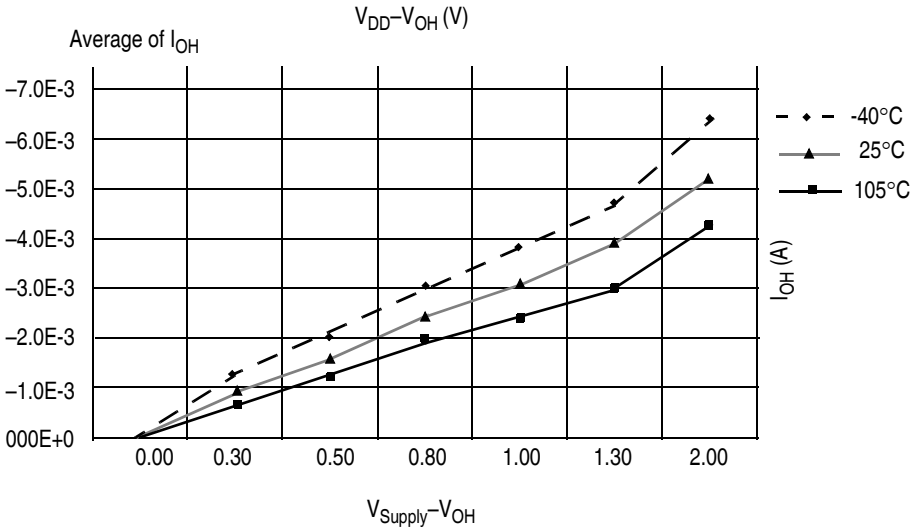


Figure 7. Typical I_{OH} vs. $V_{DD}–V_{OH}$ at V_{DD} = 5 V (Low Drive, PTxDSn = 0)

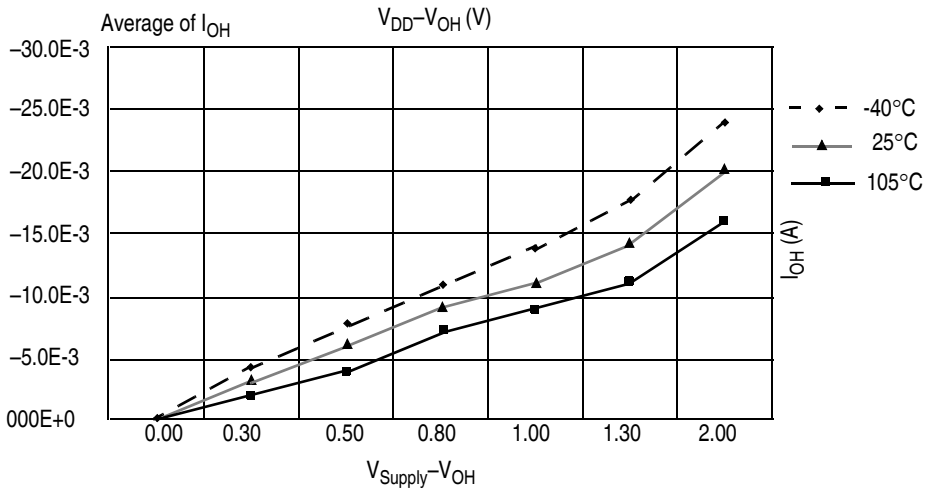


Figure 8. Typical I_{OH} vs. $V_{DD}–V_{OH}$ at V_{DD} = 5 V (High Drive, PTxDSn = 1)

2.6 Supply Current Characteristics

Table 11. Supply Current Characteristics

Num	C	Parameter		Symbol	V_{DD} (V)	Typical[1]	Max[2]	Unit
1	T	Run supply current measured at FEI mode, all modules off, system clock at:	2 MHz	RI_{DD}	5	2.27	—	mA
					3.3	2.24	—	
			4 MHz		5	3.67	—	
					3.3	3.64	—	
			8 MHz		5	6.55	—	
					3.3	6.54	—	
			16 MHz		5	11.90	—	
					3.3	11.85	—	
2	T	Run supply current measured at FEI mode, all modules on, system clock at:	2 MHz		5	3.28	—	
					3.3	3.26	—	
			4 MHz		5	4.33	—	
					3.3	4.32	—	
			8 MHz		5	8.17	—	
					3.3	8.05	—	
			16 MHz		5	14.8	—	
					3.3	14.74	—	
3	T	Run supply current measured at FBE mode, all modules off (RANGE = 1, HGO = 0), system clock at:	2 MHz		5	3.28	—	
					3.3	3.26	—	
			4 MHz		5	4.69	—	
					3.3	4.67	—	
			8 MHz		5	7.48	—	
					3.3	7.46	—	
			16 MHz		5	13.10	—	
					3.3	13.07	—	
4	T	Run supply current measured at FBE mode, all modules on (RANGE = 1, HGO = 0), system clock at:	2 MHz		5	3.64	—	
					3.3	3.63	—	
			4 MHz		5	5.38	—	
					3.3	5.35	—	
			8 MHz		5	8.65	—	
					3.3	8.64	—	
			16 MHz		5	15.55	—	
					3.3	15.40	—	

2.8 ADC Characteristics

Table 13. 5 Volt 12-bit ADC Operating Conditions

Num	C	Characteristic	Conditions	Symb	Min	Typical[1]	Max	Unit	Comment
1	D	Supply voltage	Absolute	V_{DDA}	2.7	—	5.5	V	
	D		Delta to V_{DD} ($V_{DD} - V_{DDA}$)[2]	ΔV_{DDA}	–100	0	100	mV	
2	D	Ground voltage	Delta to V_{SS} ($V_{SS} - V_{SSA}$)[2]	ΔV_{SSA}	–100	0	100	mV	
3	D	Reference voltage high		V_{REFH}	2.7	V_{DDA}	V_{DDA}	V	
4	D	Reference voltage low		V_{REFL}	V_{SSA}	V_{SSA}	V_{SSA}	V	
5	D	Input voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
6	C	Input capacitance		C_{ADIN}	—	4.5	5.5	pF	
7	C	Input resistance		R_{ADIN}	—	3	5	kΩ	
8	C	Analog source resistance	12-bit mode f_{ADCK} > 4MHz f_{ADCK} < 4MHz	R_{AS}	 — —	 — —	 2 5	kΩ	External to MCU
	C		10-bit mode f_{ADCK} > 4MHz f_{ADCK} < 4MHz		 — —	 — —	 5 10		
	C		8-bit mode (all valid f_{ADCK})		—	—	10		
9	D	ADC conversion clock frequency	High speed (ADLPC = 0)	f_{ADCK}	0.4	—	8.0	MHz	
	D		Low power (ADLPC = 1)		0.4	—	4.0		

1 Typical values assume V_{DDA} = 5.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential difference.

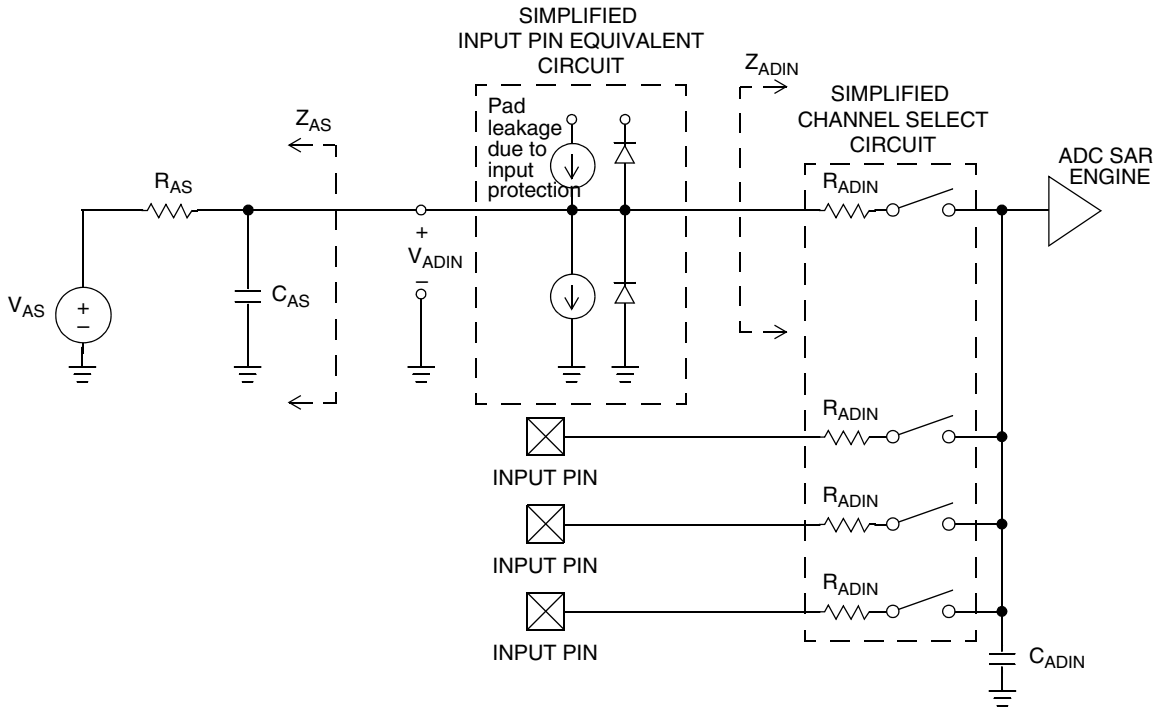


Figure 10. ADC Input Impedance Equivalency Diagram

Table 14. 5 Volt 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Num	C	Characteristic	Conditions	Symb	Min	Typical[1]	Max	Unit	Comment
1	T	Supply current ADLPC = 1 ADLSMP = 1 ADCO = 1		I_{DDA}	—	133	—	µA	
2	T	Supply current ADLPC = 1 ADLSM = 0 ADCO = 1		I_{DDA}	—	218	—	µA	
3	T	Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1		I_{DDA}	—	327	—	µA	
4	D	Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1		I_{DDA}	—	0.582	1	mA	
5	T	Supply current	Stop, reset, module off	I_{DDA}	—	0.011	1	µA	
6	P	ADC asynchronous clock source	High speed (ADLPC = 0)	f_{ADACK}	2	3.3	5	MHz	$t_{ADACK} = 1/f_{ADACK}$
			Low power (ADLPC = 1)		1.25	2	3.3		

3 Monotonicity and No-Missing-Codes guaranteed in 10-bit and 8-bit modes

4 Based on input pad leakage current. Refer to pad electricals.

2.9 External Oscillator (XOSC) Characteristics

Table 15. Oscillator Electrical Specifications (Temperature Range = –40 to 105 °C Ambient)

Num	C	Rating	Symbol	Min	Typical[1]	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1) FEE or FBE mode[2] High range (RANGE = 1) PEE or PBE mode[3] High range (RANGE = 1, HGO = 1) BLPE mode High range (RANGE = 1, HGO = 0) BLPE mode	 f_{lo} f_{hi-fll} f_{hi-pll} f_{hi-hgo} f_{hi-lp}	 32 1 1 1 1	 — — — — —	 38.4 5 16 16 8	 kHz MHz MHz MHz MHz
2	—	Load capacitors	C_1 C_2	See crystal or resonator manufacturer's recommendation.			
3	—	Feedback resistor Low range (32 kHz to 38.4 kHz) High range (1 MHz to 16 MHz)	R_F		 10 1		MΩ
4	—	Series resistor Low range, low gain (RANGE = 0, HGO = 0) Low range, high gain (RANGE = 0, HGO = 1) High range, low gain (RANGE = 1, HGO = 0) High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	 — — — — — —	 0 100 0 0 0 0	 — — — 0 10 20	kΩ
5	T	Crystal start-up time [4] Low range, low gain (RANGE = 0, HGO = 0) Low range, high gain (RANGE = 0, HGO = 1) High range, low gain (RANGE = 1, HGO = 0)[5] High range, high gain (RANGE = 1, HGO = 1)[5]	 $t_{CSTL-LP}$ $t_{CSTL-HGO}$ $t_{CSTH-LP}$ $t_{CSTH-HGO}$	 — — — —	 200 400 5 15	 — — — —	ms
6	T	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE or FBE mode [2] PEE or PBE mode [3] BLPE mode	f_{extal}	0.03125 1 0	—	5 16 40	MHz

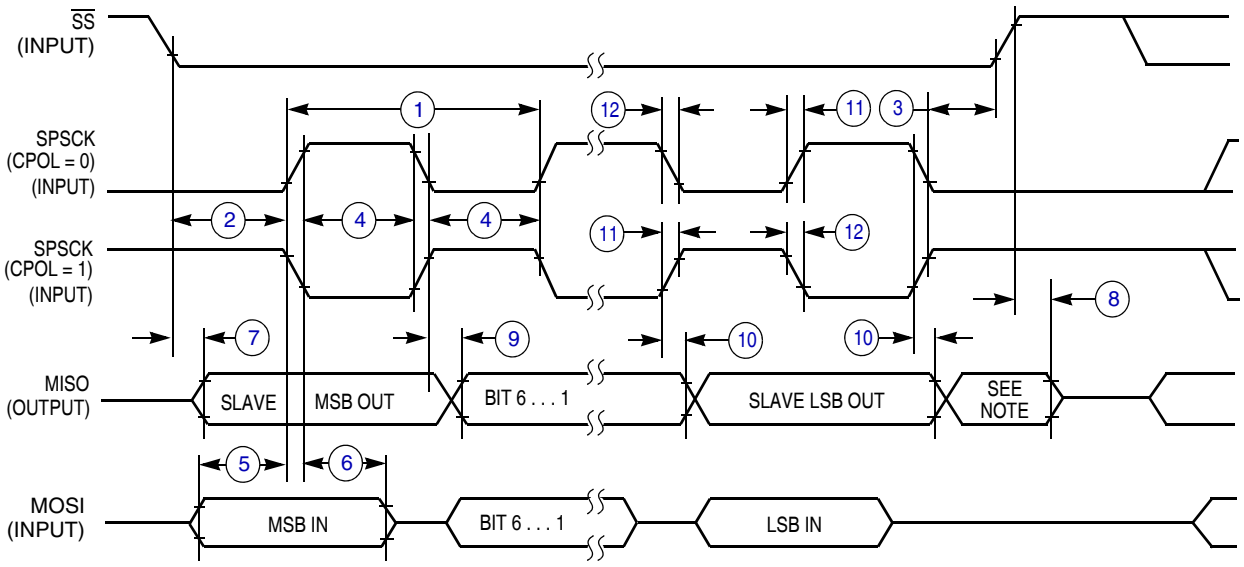
1 Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.

2 When MCG is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.

3 When MCG is configured for PEE or PBE mode, input clock source must be divisible using RDIV to within the range of 1 MHz to 2 MHz.

4 This parameter is characterized and not tested on each device. Proper PC board layout procedures must be followed to achieve specifications.

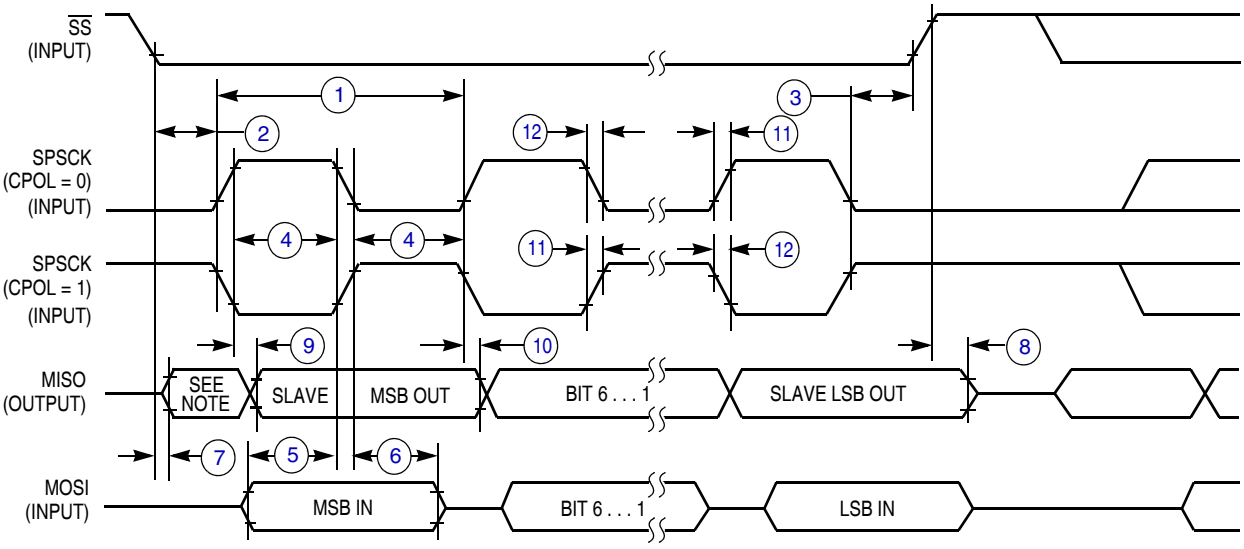
5 4 MHz crystal



NOTE:

1. Not defined but normally MSB of character just received

Figure 17. SPI Slave Timing (CPHA = 0)



NOTE:

1. Not defined but normally LSB of character just received

Figure 18. SPI Slave Timing (CPHA = 1)

2.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the Flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see Chapter 4, “Memory.”

4 Revision History

Table 23. Revision History

Revision	Description
1	Initial published
2	Updated ADC channels, Item 1, 4-5 on Table 2.10
3	Completed all theTBDs. Changed RTC to RTI in Figure 1. Corrected the block diagram. Changed V_{DDAD} to V_{DDA}, V_{SSAD} to V_{SSA}. Added charge device model data and removed machine data in Table 8. Updated the specifications of V_{LVDH}, V_{LVDL}, V_{LVWH} and V_{LVWL} in Table 10. Updated $S2I_{DD}$, $S3I_{DD}$ in Table 11. Added C column in Table 14. Updated f_{dco_DMX32} in Table 16.
4	Corrected the expansion of SPI to serial peripheral interface.
5	Updated V_{LVDL} in the Table 10. Updated RI_{DD} in the Table 11.
6	Updated V_{LVDH}, V_{LVDL}, V_{LVWH} and V_{LVWL} in the Table 10. Added LPO on the Figure 1 and LPO features in the Section 1.3, “Features.”
7	Added 44-pin LQFP package information for AC256 and AC128.