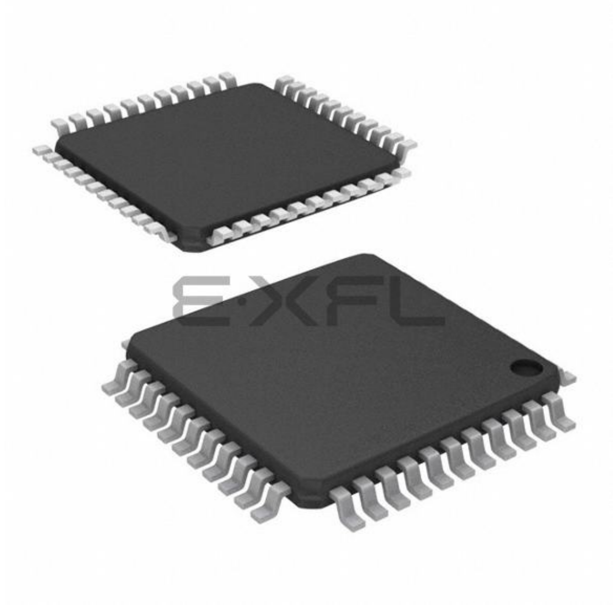
NXP USA Inc. - MCF51AC256BCFGER Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SCI, SPI
Peripherals	LVD, PWM, WDT
Number of I/O	36
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 9x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf51ac256bcfger

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1 MCF51AC256 Family Configurations

1.1 Device Comparison

The MCF51AC256 series is summarized in Table 1.

Table 1. MCF51AC256 Series Device Comparison

Feature	MCF51AC256A		MCF51AC256B			MCF51AC128A		MCF51AC128C		
	80-pin	64-pin	80-pin	64-pin	44-pin	80-pin	64-pin	80-pin	64-pin	44-pin
Flash memory size (Kbytes)	256					128				
RAM size (Kbytes)	32					32 or 16[1]				
V1 ColdFire core with BDM (background debug module)	Yes									
ACMP1 (analog comparator)	Yes									
ACMP2 (analog comparator)	Yes		Yes		No	Yes				No
ADC (analog-to-digital converter) channels (12-bit)	24	20	24	20	9	24	20	24	20	9
CAN (controller area network)	Yes		No			Yes		No		
COP (computer operating properly)	Yes									
CRC (cyclic redundancy check)	Yes									
RTI	Yes									
DBG (debug)	Yes									
IIC1 (inter-integrated circuit)	Yes									
IRQ (interrupt request input)	Yes									
INTC (interrupt controller)	Yes									
KBI (keyboard interrupts)	Yes									
LVD (low-voltage detector)	Yes									
MCG (multipurpose clock generator)	Yes									
OSC (crystal oscillator)	Yes									
Port I/O[2]	69	54	69	54	36	69	54	69	54	36
RGPIO (rapid general-purpose I/O)	16				12	16				12
SCI1, SCI2 (serial communications interfaces)	Yes									
SPI1 (serial peripheral interface)	Yes									
SPI2 (serial peripheral interface)	Yes	No	Yes	No		Yes	No	Yes	No	
FTM1 (flexible timer module) channels	6				4	6				4
FTM2 channels	6	2	6	2	2	6	2	6	2	2

1.3 Features

Table 2 describes the functional units of the MCF51AC256 series.

Table 2. MCF51AC256 Series Functional Units

Functional Unit	Function
CF1 Core (V1 ColdFire core)	Executes programs and interrupt handlers
BDM (background debug module)	Provides single pin debugging interface (part of the V1 ColdFire core)
DBG (debug)	Provides debugging and emulation capabilities (part of the V1 ColdFire core)
VBUS (debug visibility bus)	Allows for real-time program traces (part of the V1 ColdFire core)
SIM (system integration module)	Controls resets and chip level interfaces between modules
Flash (flash memory)	Provides storage for program code, constants and variables
RAM (random-access memory)	Provides storage for program variables
RGPIO (rapid general-purpose input/output)	Allows for I/O port access at CPU clock speeds
VREG (voltage regulator)	Controls power management across the device
COP (computer operating properly)	Monitors a countdown timer and generates a reset if the timer is not regularly reset by the software
LVD (low-voltage detect)	Monitors internal and external supply voltage levels, and generates a reset or interrupt when the voltages are too low
CF1_INTC (interrupt controller)	Controls and prioritizes all device interrupts
ADC (analog-to-digital converter)	Measures analog voltages at up to 12 bits of resolution
FTM1, FTM2 (flexible timer/pulse-width modulators)	Provides a variety of timing-based features
TPM3 (timer/pulse-width modulator)	Provides a variety of timing-based features
CRC (cyclic redundancy check)	Accelerates computation of CRC values for ranges of memory
ACMP1, ACMP2 (analog comparators)	Compares two analog inputs
IIC (inter-integrated circuit)	Supports standard IIC communications protocol
KBI (keyboard interrupt)	Provides pin interrupt capabilities
MCG (multipurpose clock generator)	Provides clocking options for the device, including a phase-locked loop (PLL) and frequency-locked loop (FLL) for multiplying slower reference clock sources
OSC (crystal oscillator)	Allows a crystal or ceramic resonator to be used as the system clock source or reference clock for the PLL or FLL
LPO (low-power oscillator)	Provides a second clock source for COP and RTI.
CAN (controller area network)	Supports standard CAN communications protocol
SCI1, SCI2 (serial communications interfaces)	Serial communications UARTs capable of supporting RS-232 and LIN protocols
SPI1 (8-bit serial peripheral interfaces)	Provides 8-bit 4-pin synchronous serial interface
SPI2 (16-bit serial peripheral interfaces)	Provides 16-bit 4-pin synchronous serial interface with FIFO

  - Trimmable internal reference allows 0.2% resolution and 2% deviation
- Analog-to-digital converter (ADC)
  - 24 analog inputs with 12 bits resolution
  - Output formatted in 12-, 10- or 8-bit right-justified format
  - Single or continuous conversion (automatic return to idle after single conversion)
  - Operation in low-power modes for lower noise operation
  - Asynchronous clock source for lower noise operation
  - Automatic compare with interrupt for less-than, or greater-than or equal-to, programmable value
  - On-chip temperature sensor
- Flexible timer/pulse-width modulators (FTM)
  - 16-bit Free-running counter or a counter with initial and final value. The counting can be up and unsigned, up and signed, or up-down and unsigned
  - Up to 6 channels, and each channel can be configured for input capture, output compare or edge-aligned PWM mode, all channels can be configured for center-aligned PWM mode
    - Channels can operate as pairs with equal outputs, pairs with complimentary outputs or independent channels (with independent outputs)
    - Each pair of channels can be combined to generate a PWM signal (with independent control of both edges of PWM signal)
    - Deadtime insertion is available for each complementary pair
  - The load of the FTM registers which have write buffer can be synchronized; write protection for critical registers
  - Generation of the triggers to ADC (hardware trigger)
  - A fault input for global fault control
  - Backwards compatible with TPM
- Timer/pulse width modulator (TPM)
  - 16-bit free-running or modulo up/down count operation
  - Two channels, each channel may be input capture, output compare, or edge-aligned PWM
  - One interrupt per channel plus terminal count interrupt
- Cyclic redundancy check (CRC) generator
  - High speed hardware CRC generator circuit using 16-bit shift register
  - CRC16-CCITT compliancy with $x^{16} + x^{12} + x^5 + 1$ polynomial
  - Error detection for all single, double, odd, and most multi-bit errors
  - Programmable initial seed value
- Analog comparators (ACMP)
  - Full rail to rail supply operation
  - Selectable interrupt on rising edge, falling edge, or either rising or falling edges of comparator output
  - Option to compare to fixed internal bandgap reference voltage
  - Option to allow comparator output to be visible on a pin, ACMPxO

- Inter-integrated circuit (IIC)
  - Compatible with IIC bus standard
  - Multi-master operation
  - Software programmable for one of 64 different serial clock frequencies
  - Interrupt driven byte-by-byte data transfer
  - Arbitration lost interrupt with automatic mode switching from master to slave
  - Calling address identification interrupt
  - Bus busy detection
  - 10-bit address extension
- Controller area network (CAN)
  - Implementation of the CAN protocol — Version 2.0A/B
    - Standard and extended data frames
    - Zero to eight bytes data length
    - Programmable bit rate up to 1 Mbps
    - Support for remote frames
  - Five receive buffers with FIFO storage scheme
  - Three transmit buffers with internal prioritization using a “local priority” concept
  - Flexible maskable identifier filter supports two full-size (32-bit) extended identifier filters, four 16-bit filters, or eight 8-bit filters
  - Programmable wakeup functionality with integrated low-pass filter
  - Programmable loopback mode supports self-test operation
  - Programmable listen-only mode for monitoring of CAN bus
  - Programmable bus-off recovery functionality
  - Separate signalling and interrupt capabilities for all CAN receiver and transmitter error states (warning, error passive, bus-off)
  - Internal timer for time-stamping of received and transmitted messages
- Serial communications interfaces (SCI)
  - Full-duplex, standard non-return-to-zero (NRZ) format
  - Double-buffered transmitter and receiver with separate enables
  - Programmable baud rates (13-bit modulo divider)
  - Interrupt-driven or polled operation
  - Hardware parity generation and checking
  - Programmable 8-bit or 9-bit character length
  - Receiver wakeup by idle-line or address-mark
  - Optional 13-bit break character generation / 11-bit break character detection
  - Selectable transmitter output polarity
- Serial peripheral interfaces (SPI)
  - Master or slave mode operation
  - Full-duplex or single-wire bidirectional option
  - Programmable transmit bit rate

1.5 Pinouts and Packaging

Figure 2 shows the pinout of the 80-pin LQFP.

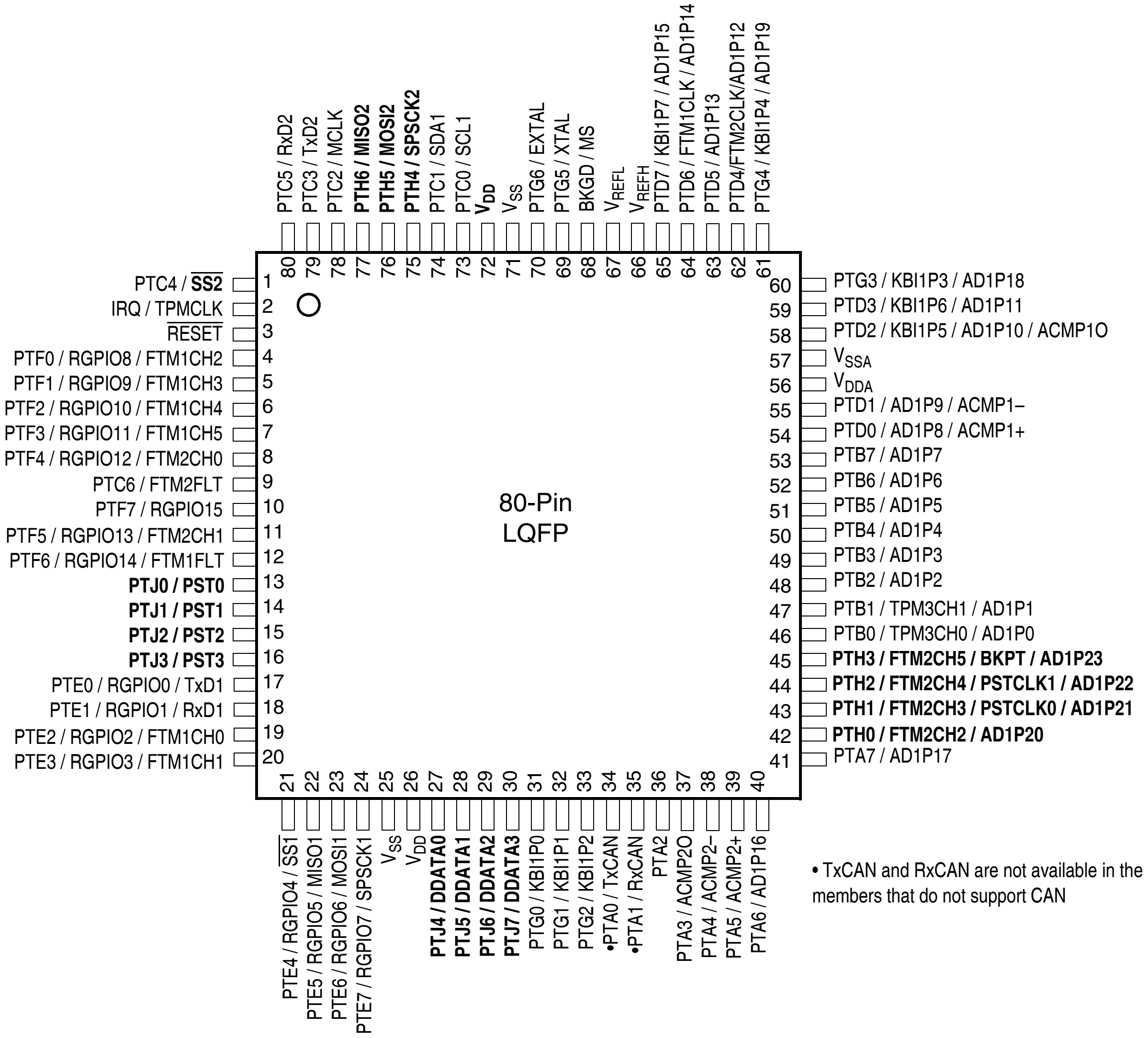
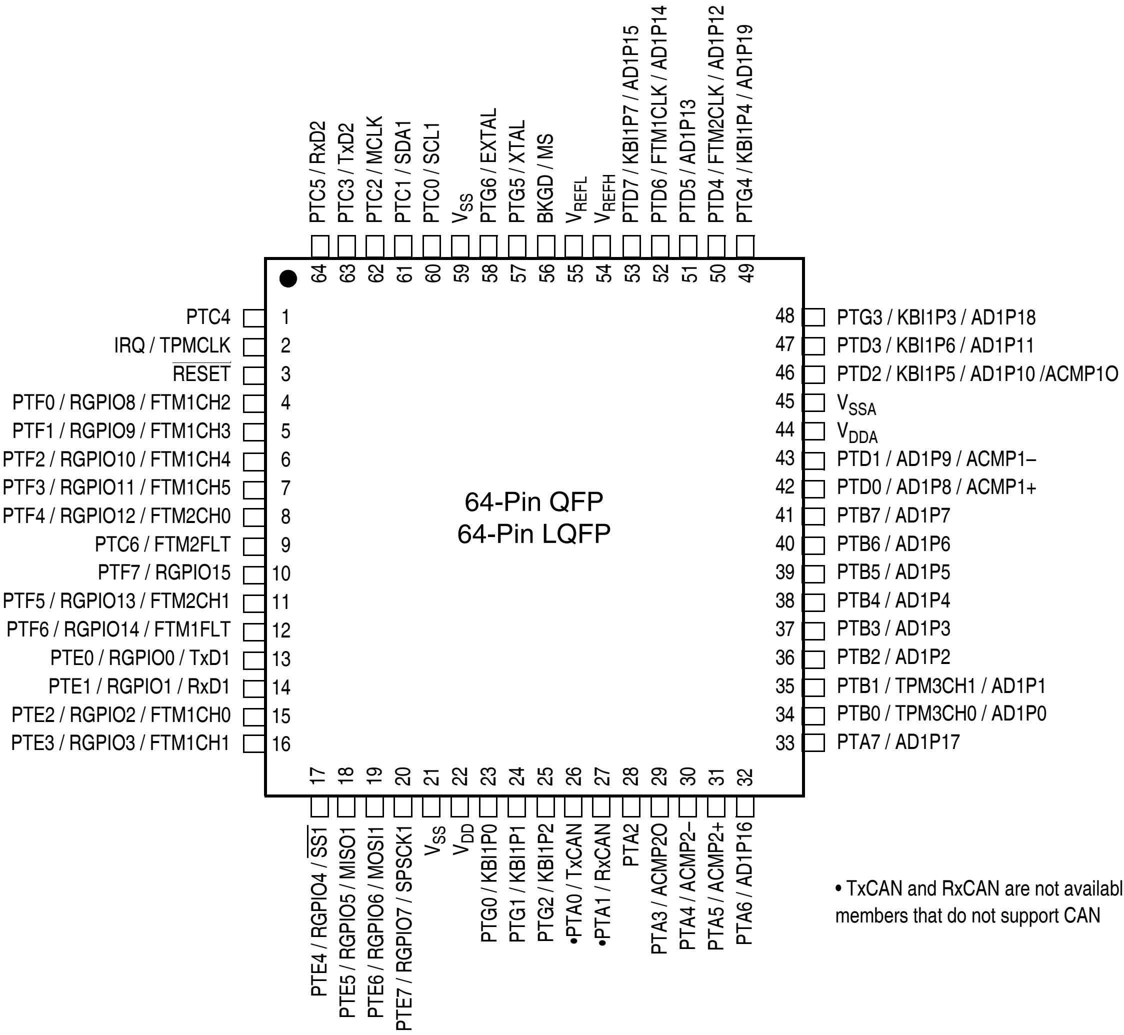


Figure 2. MCF51AC256 Series ColdFire Microcontroller 80-Pin LQFP

Figure 3 shows the pinout of the 64-pin LQFP and QFP.



• TxCAN and RxCAN are not available in the members that do not support CAN

Figure 3. MCF51AC256 Series ColdFire Microcontroller 64-Pin QFP/LQFP

Figure 4 shows the pinout of the 44-pin LQFP.

2 Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the MCF51AC256 microcontroller, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. These specifications will, however, be met for production silicon. Finalized specifications will be published after complete characterization and device qualifications have been completed.

NOTE

The parameters specified in this data sheet supersede any values found in the module specifications.

2.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 5. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

2.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 6 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}).

Table 6. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to 5.8	V
Input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1], [2], [3]	I_D	±25	mA
Maximum current into V_{DD}	I_{DD}	120	mA
Storage temperature	T_{stg}	–55 to 150	°C

[1] Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

[2] All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

[3] Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low which would reduce overall power consumption.

2.3 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and it is user-determined rather than being controlled by the MCU design. In order to take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 7. Thermal Characteristics

Rating		Symbol	Value	Unit
Operating temperature range (packaged)		T_A	–40 to 105	°C
Maximum junction temperature		T_J	150	°C
Thermal resistance [1,2,3,4]		θ_{JA}		°C/W
80-pin LQFP				
	1s		51	
	2s2p		38	
64-pin LQFP				
	1s		59	
	2s2p		41	
64-pin QFP				
	1s		50	
	2s2p		36	
44-pin LQFP				
	1s		67	
	2s2p		45	

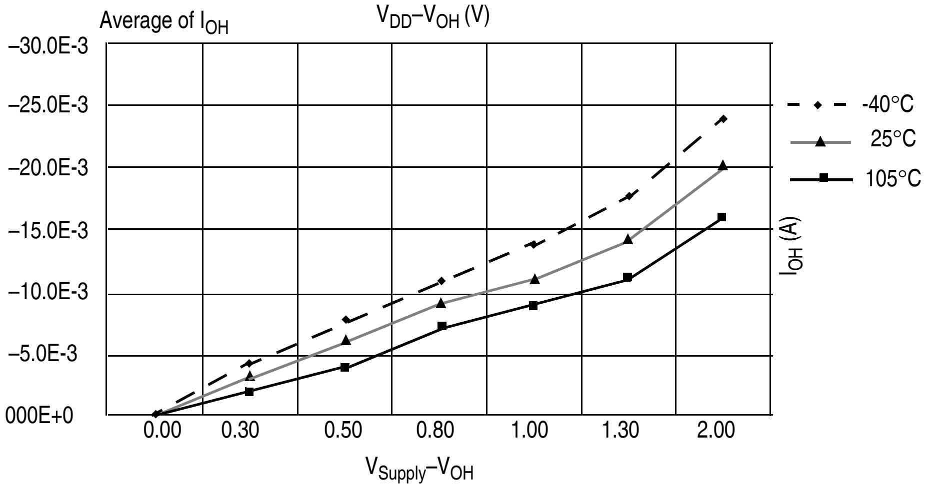


Figure 8. Typical I_{OH} vs. V_{DD}–V_{OH} at V_{DD} = 5 V (High Drive, PTxDSn = 1)

2.6 Supply Current Characteristics

Table 11. Supply Current Characteristics

Num	C	Parameter		Symbol	V_{DD} (V)	Typical[1]	Max[2]	Unit
1	T	Run supply current measured at FEI mode, all modules off, system clock at:	2 MHz	RI_{DD}	5	2.27	—	mA
					3.3	2.24	—	
			4 MHz		5	3.67	—	
					3.3	3.64	—	
			8 MHz		5	6.55	—	
					3.3	6.54	—	
			16 MHz		5	11.90	—	
					3.3	11.85	—	
2	T	Run supply current measured at FEI mode, all modules on, system clock at:	2 MHz		5	3.28	—	
					3.3	3.26	—	
			4 MHz		5	4.33	—	
					3.3	4.32	—	
			8 MHz		5	8.17	—	
					3.3	8.05	—	
			16 MHz		5	14.8	—	
					3.3	14.74	—	
3	T	Run supply current measured at FBE mode, all modules off (RANGE = 1, HGO = 0), system clock at:	2 MHz		5	3.28	—	
					3.3	3.26	—	
			4 MHz		5	4.69	—	
					3.3	4.67	—	
			8 MHz		5	7.48	—	
					3.3	7.46	—	
			16 MHz		5	13.10	—	
					3.3	13.07	—	
4	T	Run supply current measured at FBE mode, all modules on (RANGE = 1, HGO = 0), system clock at:	2 MHz		5	3.64	—	
					3.3	3.63	—	
			4 MHz		5	5.38	—	
					3.3	5.35	—	
			8 MHz		5	8.65	—	
					3.3	8.64	—	
			16 MHz		5	15.55	—	
					3.3	15.40	—	

Table 11. Supply Current Characteristics (continued)

Num	C	Parameter	Symbol	V_{DD} (V)	Typical[1]	Max[2]	Unit
5	C	Wait mode supply[3] current measured at (CPU clock = 2 MHz, f_{Bus} = 1 MHz)	WI_{DD}	5	1.3	2	mA
				3	1.29	2	
6	C	Wait mode supply[3] current measured at (CPU clock = 16 MHz, f_{Bus} = 8 MHz)		5	5.11	8	mA
				3	5.1	8	
7	C	Wait mode supply[3] current measured at (CPU clock = 50 MHz, f_{Bus} = 25 MHz)		5	15.24	25	mA
				3	15.2	25	
8	C	Stop2 mode supply current –40 °C 25 °C 120 °C	$S2I_{DD}$	5	1.40	2.5 2.5 200	µA
		–40 °C 25 °C 120 °C		3	1.16	2.5 2.5 200	µA
9	C	Stop3 mode supply current –40 °C 25 °C 120 °C	$S3I_{DD}$	5	1.60	2.5 2.5 220	µA
		–40 °C 25 °C 120 °C		3	1.35	2.5 2.5 220	µA
10	C	RTI adder to stop2 or stop3[3], 25 °C	$S23I_{DDRTI}$	5	300		nA
				3	300		nA
11	C	Adder to stop3 for oscillator enabled[4] (ERCLKEN =1 and EREFSTEN = 1)	$S3I_{DDOSC}$	5, 3	5		µA

[1] Typicals are measured at 25 °C.

[2] Values given here are preliminary estimates prior to completing characterization.

[3] Most customers are expected to find that auto-wakeup from stop2 or stop3 can be used instead of the higher current wait mode.

[4] Values given under the following conditions: low range operation (RANGE = 0), low power mode (HGO = 0).

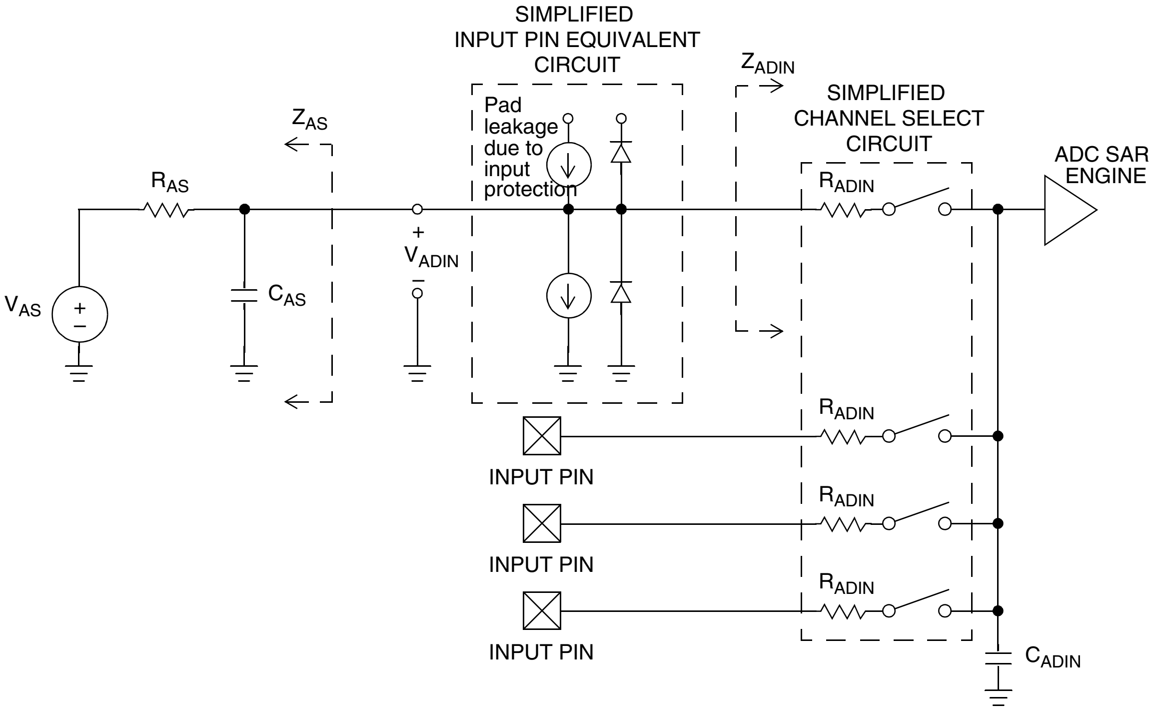


Figure 10. ADC Input Impedance Equivalency Diagram

Table 14. 5 Volt 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

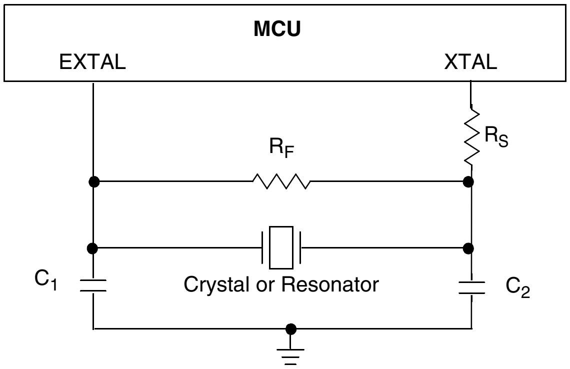
Num	C	Characteristic	Conditions	Symb	Min	Typical[1]	Max	Unit	Comment
1	T	Supply current ADLPC = 1 ADLSMP = 1 ADCO = 1		I_{DDA}	—	133	—	µA	
2	T	Supply current ADLPC = 1 ADLSM = 0 ADCO = 1		I_{DDA}	—	218	—	µA	
3	T	Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1		I_{DDA}	—	327	—	µA	
4	D	Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1		I_{DDA}	—	0.582	1	mA	
5	T	Supply current	Stop, reset, module off	I_{DDA}	—	0.011	1	µA	
6	P	ADC asynchronous clock source	High speed (ADLPC = 0)	f_{ADACK}	2	3.3	5	MHz	t_{ADACK} = $1/f_{ADACK}$
			Low power (ADLPC = 1)		1.25	2	3.3		

Table 14. 5 Volt 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Num	C	Characteristic	Conditions	Symb	Min	Typical[1]	Max	Unit	Comment
7	P	Conversion time (including sample time)	Short sample (ADLSMP = 0)	t_{ADC}	—	20	—	ADCK cycles	See Table 10 for conversion time variances
			Long sample (ADLSMP = 1)		—	40	—		
8	T	Sample time	Short sample (ADLSMP = 0)	t_{ADS}	—	3.5	—	ADCK cycles	
			Long sample (ADLSMP = 1)		—	23.5	—		
9	T	Total unadjusted error	12-bit mode	E_{TUE}	—	±3.0	—	LSB[2]	Includes quantization
	P		10-bit mode		—	±1	±2.5		
	T		8-bit mode		—	±0.5	±1.0		
10	T	Differential non-linearity	12-bit mode	DNL	—	±1.75	—	LSB[2]	
	P		10-bit mode[3]		—	±0.5	±1.0		
	T		8-bit mode[3]		—	±0.3	±0.5		
11	T	Integral non-linearity	12-bit mode	INL	—	±1.5	—	LSB[2]	
	T		10-bit mode		—	±0.5	±1.0		
	T		8-bit mode		—	±0.3	±0.5		
12	T	Zero-scale error	12-bit mode	E_{ZS}	—	±1.5	—	LSB[2]	$V_{ADIN} = V_{SSA}$
	P		10-bit mode		—	±0.5	±1.5		
	T		8-bit mode		—	±0.5	±0.5		
13	T	Full-scale error	12-bit mode	E_{FS}	—	±1	—	LSB[2]	$V_{ADIN} = V_{DDA}$
	P		10-bit mode		—	±0.5	±1		
	T		8-bit mode		—	±0.5	±0.5		
14	D	Quantization error	12-bit mode	E_Q	—	–1 to 0	—	LSB[2]	
			10-bit mode		—	—	±0.5		
			8-bit mode		—	—	±0.5		
15	D	Input leakage error	12-bit mode	E_{IL}	—	±1	—	LSB[2]	Pad leakage[4] * R_{AS}
			10-bit mode		—	±0.2	±2.5		
			8-bit mode		—	±0.1	±1		
16	D	Temp sensor voltage	25°C	V_{TEMP25}	—	1.396	—	V	
17	D	Temp sensor slope	–40 °C–25 °C	m	—	3.266	—	mV/°C	
			25 °C–85 °C		—	3.638	—		

[1] Typical values assume $V_{DDA} = 5.0$ V, Temp = 25 °C, $f_{ADCK} = 1.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

[2] 1 LSB = $(V_{REFH} - V_{REFL})/2^N$.



2.10 MCG Specifications

Table 16. MCG Frequency Specifications (Temperature Range = –40 to 105 °C Ambient)

Num	C	Rating		Symbol	Min	Typical[1]	Max	Unit
1	C	Internal reference frequency — factory trimmed at V_{DD} = 5 V and temperature = 25 °C		f_{int_ft}	—	32.768	—	kHz
2	C	Average internal reference frequency — untrimmed		f_{int_ut}	31.25	—	39.0625	kHz
3	T	Internal reference startup time		t_{irefst}	—	60	100	µs
4	C	DCO output frequency range — untrimmed [2]	Low range (DRS=00)	f_{dco_ut}	16	—	20	MHz
	C		Mid range (DRS=01)		32	—	40	
	C		High range (DRS=10)		48	—	60	
5	P	DCO output frequency[2] reference =32768Hz and DMX32 = 1	Low range (DRS=00)	f_{dco_DMX32}	—	16.82	—	MHz
	P		Mid range (DRS=01)		—	33.69	—	
	P		High range (DRS=10)		—	50.48	—	
6	D	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)		$\Delta f_{dco\_res\_t}$	—	±0.1	±0.2	%f_{dco}
7	D	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)		$\Delta f_{dco\_res\_t}$	—	±0.2	±0.4	%f_{dco}
8	D	Total deviation of trimmed DCO output frequency over voltage and temperature		Δf_{dco_t}	—	0.5 –1.0	±2	%f_{dco}
9	D	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0–70 °C		Δf_{dco_t}	—	±0.5	±1	%f_{dco}
10	D	FLL acquisition time[3]		$t_{fll\_acquire}$	—	—	1	ms
11	D	PLL acquisition time[4]		$t_{pll\_acquire}$	—	—	1	ms
12	D	Long term jitter of DCO output clock (averaged over 2ms interval) [5]		C_{Jitter}	—	0.02	0.2	%f_{dco}
13	D	VCO operating frequency		f_{vco}	7.0	—	55.0	MHz
16	D	Jitter of PLL output clock measured over 625 ns[6]		$f_{pll\_jitter\_625ns}$	—	0.566[6]	—	%f_{pll}
17	D	Lock entry frequency tolerance [7]		D_{lock}	±1.49	—	±2.98	%

2.11.1 Control Timing

Table 17. Control Timing

Num	C	Parameter	Symbol	Min	Typical[1]	Max	Unit
1	D	Bus frequency ($t_{cyc} = 1/f_{Bus}$)	f_{Bus}	dc	—	24	MHz
2	D	Internal low-power oscillator period	t_{LPO}	800	—	1500	μs
3	D	External reset pulse width[2] ($t_{cyc} = 1/f_{Self\_reset}$)	t_{extrst}	100	—	—	ns
4	D	Reset low drive	t_{rstdrv}	$66 \times t_{cyc}$	—	—	ns
5	D	Active background debug mode latch setup time	t_{MSSU}	500	—	—	ns
6	D	Active background debug mode latch hold time	t_{MSH}	100	—	—	ns
7	D	IRQ pulse width Asynchronous path[2] Synchronous path[3]	t_{ILIH}, t_{IHIL}	 100 $1.5 \times t_{cyc}$	—	—	ns
8	D	KBIPx pulse width Asynchronous path[2] Synchronous path[3]	t_{ILIH}, t_{IHIL}	 100 $1.5 \times t_{cyc}$	—	—	ns
9	D	Port rise and fall time (load = 50 pF)[4] Slew rate control disabled (PTxSE = 0), Low Drive Slew rate control enabled (PTxSE = 1), Low Drive Slew rate control disabled (PTxSE = 0), Low Drive Slew rate control enabled (PTxSE = 1), Low Drive	t_{Rise}, t_{Fall}	 — — — —	 11 35 40 75	—	ns

[1] Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.

[2] This is the shortest pulse that is guaranteed to be recognized as a reset pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

[3] This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

[4] Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40 °C to 105 °C.

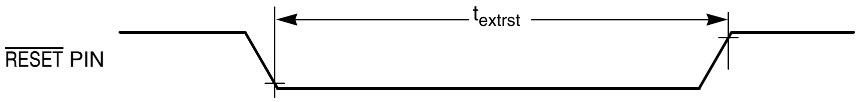


Figure 11. Reset Timing

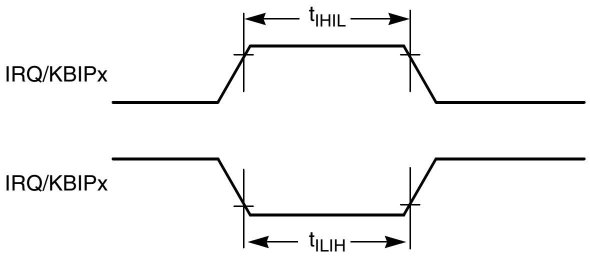


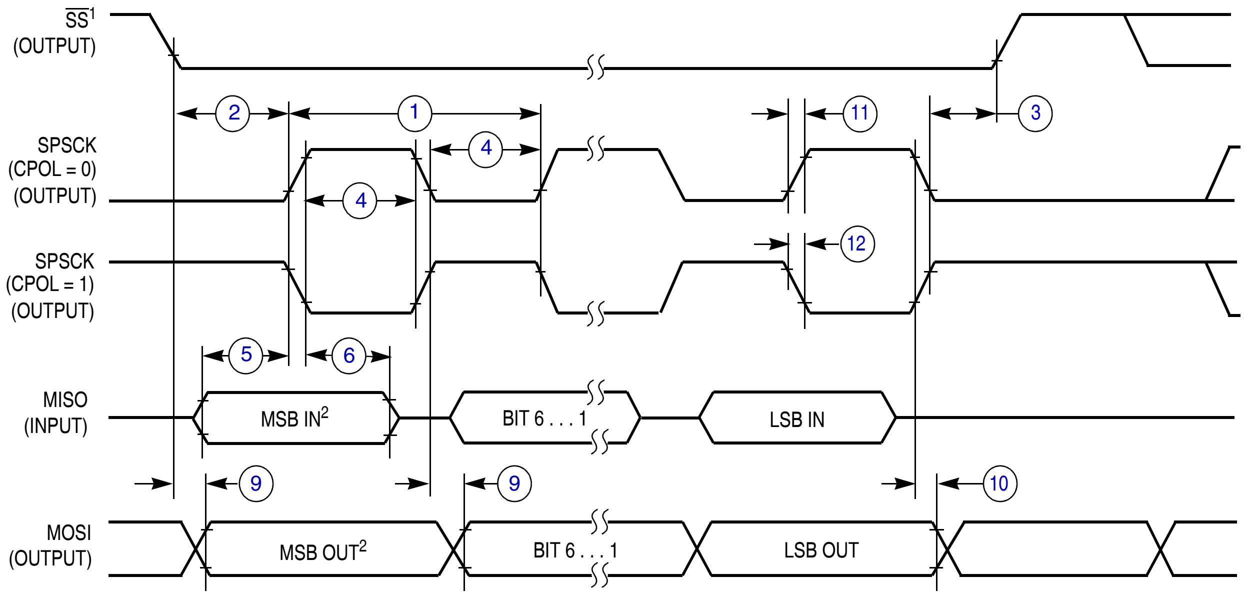
Figure 12. IRQ/KBIPx Timing

2.12 SPI Characteristics

Table 20 and Figure 15 through Figure 18 describe the timing requirements for the SPI system.

Table 20. SPI Timing

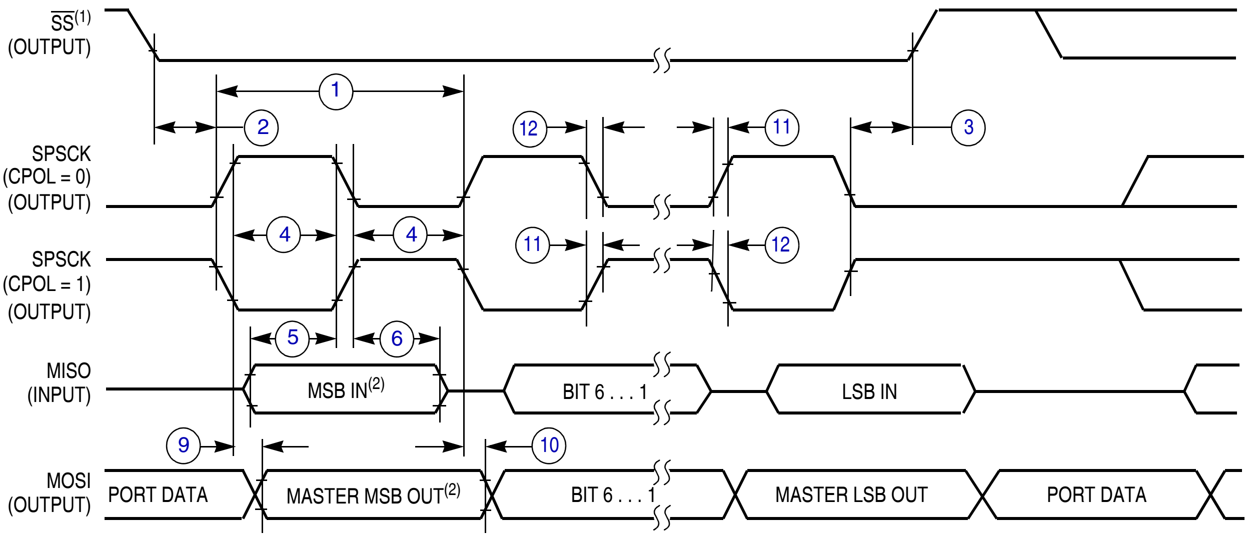
No.	C	Function	Symbol	Min	Max	Unit
—	D	Operating frequency Master Slave	f_{op}	$f_{Bus}/2048$ 0	$f_{Bus}/2$ $f_{Bus}/4$	Hz
1	D	SPSCK period Master Slave	t_{SPSCK}	2 4	2048 —	t_{cyc} t_{cyc}
2	D	Enable lead time Master Slave	t_{Lead}	1/2 1	— —	t_{SPSCK} t_{cyc}
3	D	Enable lag time Master Slave	t_{Lag}	1/2 1	— —	t_{SPSCK} t_{cyc}
4	D	Clock (SPSCK) high or low time Master Slave	t_{WSPSCK}	$t_{cyc} - 30$ $t_{cyc} - 30$	1024 t_{cyc} —	ns ns
5	D	Data setup time (inputs) Master Slave	t_{SU}	15 15	— —	ns ns
6	D	Data hold time (inputs) Master Slave	t_{HI}	0 25	— —	ns ns
7	D	Slave access time	t_a	—	1	t_{cyc}
8	D	Slave MISO disable time	t_{dis}	—	1	t_{cyc}
9	D	Data valid (after SPSCK edge) Master Slave	t_v	— —	25 25	ns ns
10	D	Data hold time (outputs) Master Slave	t_{HO}	0 0	— —	ns ns
11	D	Rise time Input Output	t_{RI} t_{RO}	— —	$t_{cyc} - 25$ 25	ns ns
12	D	Fall time Input Output	t_{FI} t_{FO}	— —	$t_{cyc} - 25$ 25	ns ns



NOTES:

1. $\overline{\text{SS}}$ output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 15. SPI Master Timing (CPHA = 0)



NOTES:

1. $\overline{\text{SS}}$ output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 16. SPI Master Timing (CPHA =1)

Table 21. Flash Characteristics

Num	C	Characteristic	Symbol	Min	Typical[1]	Max	Unit
1	—	Supply voltage for program/erase	$V_{prog/erase}$	2.7	—	5.5	V
2	—	Supply voltage for read operation	V_{Read}	2.7	—	5.5	V
3	—	Internal FCLK frequency[2]	f_{FCLK}	150	—	200	kHz
4	—	Internal FCLK period (1/FCLK)	t_{Fcyc}	5	—	6.67	μs
5	—	Byte program time (random location)[2]	t_{prog}	9			t_{Fcyc}
6	—	Byte program time (burst mode)[2]	t_{Burst}	4			t_{Fcyc}
7	—	Page erase time[3]	t_{Page}	4000			t_{Fcyc}
8	—	Mass erase time[2]	t_{Mass}	20,000			t_{Fcyc}
9	C	Program/erase endurance[4] T_L to T_H = –40 °C to 105 °C T = 25 °C	—	10,000 —	— 100,000	— —	cycles
10	C	Data retention[5]	t_{D_ret}	15	100	—	years

[1] Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.

[2] The frequency of this clock is controlled by a software setting.

[3] These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

[4] **Typical endurance for flash** was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale Semiconductor defines typical endurance, please refer to Engineering Bulletin EB619/D, *Typical Endurance for Nonvolatile Memory*.

[5] **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale Semiconductor defines typical data retention, please refer to Engineering Bulletin EB618/D, *Typical Data Retention for Nonvolatile Memory.*

2.14 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

2.14.1 Radiated Emissions

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM Cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (North and East). For more detailed information concerning the evaluation results, conditions and setup, please refer to the EMC Evaluation Report for this device.

3 Mechanical Outline Drawings

Table 22 provides the available package types and their document numbers. The latest package outline/mechanical drawings are available on the MCF51AC256 Series Product Summary pages at http://www.freescale.com.

To view the latest drawing, either:

- Click on the appropriate link in Table 22, or
- Open a browser to the FreescaleÆ website (http://www.freescale.com), and enter the appropriate document number (from Table 22) in the “Enter Keyword” search box at the top of the page.

Table 22. Package Information

Pin Count	Type	Document No.
80	LQFP	98ARL10530D
64	LQFP	98ASS23234W
64	QFP	98ASB42844B
44	LQFP	98ASS23225W