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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I ² C, SCI, SPI
Peripherals	LVD, PWM, WDT
Number of I/O	69
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf51ac256bclke

1.3.1 Feature List

- 32-bit Version 1 ColdFire® central processor unit (CPU)
 - Up to 50.33 MHz at 2.7 V – 5.5 V
 - Provide 0.94 Dhrystone 2.1 DMIPS per MHz performance when running from internal RAM (0.76 DMIPS per MHz when running from flash)
 - Implements instruction set revision C (ISA_C)
- On-chip memory
 - Up to 256 KB flash memory read/program/erase over full operating voltage and temperature
 - Up to 32 KB static random access memory (SRAM)
 - Security circuitry to prevent unauthorized access to SRAM and flash contents
- Power-Saving Modes
 - Three low-power stop plus wait modes
 - Peripheral clock enable register can disable clocks to unused modules, reducing currents; allows clocks to remain enabled to specific peripherals in stop3 mode
- System protection features
 - Watchdog computer operating properly (COP) reset with options to run from independent LPO clock or bus clock
 - Low-voltage detection with reset or interrupt
 - Illegal opcode and illegal address detection with programmable reset or exception response
 - Flash block protection
- Debug support
 - Single-wire background debug interface
 - Real-time debug support, with 6 hardware breakpoints (4 PC, 1 address pair and 1 data) that can be configured into a 1- or 2-level trigger
 - On-chip trace buffer provides programmable start/stop recording conditions plus support for continuous or PC-profiling modes
 - Support for real-time program (and optional partial data) trace using the debug visibility bus
- V1 ColdFire interrupt controller (CF1_INTC)
 - Support of 40 peripheral I/O interrupt requests plus seven software (one per level) interrupt requests
 - Fixed association between interrupt request source and level plus priority, up to two requests can be remapped to the highest maskable level + priority
 - Unique vector number for each interrupt source
 - Support for service routine interrupt acknowledge (software IACK) read cycles for improved system performance
- Multipurpose clock generator (MCG)
 - Oscillator (XOSC); loop-control Pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
 - LPO clock as an optional independent clock source for COP and RTI
 - FLL/PLL controlled by internal or external reference

- Trimmable internal reference allows 0.2% resolution and 2% deviation
- Analog-to-digital converter (ADC)
 - 24 analog inputs with 12 bits resolution
 - Output formatted in 12-, 10- or 8-bit right-justified format
 - Single or continuous conversion (automatic return to idle after single conversion)
 - Operation in low-power modes for lower noise operation
 - Asynchronous clock source for lower noise operation
 - Automatic compare with interrupt for less-than, or greater-than or equal-to, programmable value
 - On-chip temperature sensor
- Flexible timer/pulse-width modulators (FTM)
 - 16-bit Free-running counter or a counter with initial and final value. The counting can be up and unsigned, up and signed, or up-down and unsigned
 - Up to 6 channels, and each channel can be configured for input capture, output compare or edge-aligned PWM mode, all channels can be configured for center-aligned PWM mode
 - Channels can operate as pairs with equal outputs, pairs with complimentary outputs or independent channels (with independent outputs)
 - Each pair of channels can be combined to generate a PWM signal (with independent control of both edges of PWM signal)
 - Deadtime insertion is available for each complementary pair
 - The load of the FTM registers which have write buffer can be synchronized; write protection for critical registers
 - Generation of the triggers to ADC (hardware trigger)
 - A fault input for global fault control
 - Backwards compatible with TPM
- Timer/pulse width modulator (TPM)
 - 16-bit free-running or modulo up/down count operation
 - Two channels, each channel may be input capture, output compare, or edge-aligned PWM
 - One interrupt per channel plus terminal count interrupt
- Cyclic redundancy check (CRC) generator
 - High speed hardware CRC generator circuit using 16-bit shift register
 - CRC16-CCITT compliancy with $x^{16} + x^{12} + x^5 + 1$ polynomial
 - Error detection for all single, double, odd, and most multi-bit errors
 - Programmable initial seed value
- Analog comparators (ACMP)
 - Full rail to rail supply operation
 - Selectable interrupt on rising edge, falling edge, or either rising or falling edges of comparator output
 - Option to compare to fixed internal bandgap reference voltage
 - Option to allow comparator output to be visible on a pin, ACMPxO

- Inter-integrated circuit (IIC)
 - Compatible with IIC bus standard
 - Multi-master operation
 - Software programmable for one of 64 different serial clock frequencies
 - Interrupt driven byte-by-byte data transfer
 - Arbitration lost interrupt with automatic mode switching from master to slave
 - Calling address identification interrupt
 - Bus busy detection
 - 10-bit address extension
- Controller area network (CAN)
 - Implementation of the CAN protocol — Version 2.0A/B
 - Standard and extended data frames
 - Zero to eight bytes data length
 - Programmable bit rate up to 1 Mbps
 - Support for remote frames
 - Five receive buffers with FIFO storage scheme
 - Three transmit buffers with internal prioritization using a “local priority” concept
 - Flexible maskable identifier filter supports two full-size (32-bit) extended identifier filters, four 16-bit filters, or eight 8-bit filters
 - Programmable wakeup functionality with integrated low-pass filter
 - Programmable loopback mode supports self-test operation
 - Programmable listen-only mode for monitoring of CAN bus
 - Programmable bus-off recovery functionality
 - Separate signalling and interrupt capabilities for all CAN receiver and transmitter error states (warning, error passive, bus-off)
 - Internal timer for time-stamping of received and transmitted messages
- Serial communications interfaces (SCI)
 - Full-duplex, standard non-return-to-zero (NRZ) format
 - Double-buffered transmitter and receiver with separate enables
 - Programmable baud rates (13-bit modulo divider)
 - Interrupt-driven or polled operation
 - Hardware parity generation and checking
 - Programmable 8-bit or 9-bit character length
 - Receiver wakeup by idle-line or address-mark
 - Optional 13-bit break character generation / 11-bit break character detection
 - Selectable transmitter output polarity
- Serial peripheral interfaces (SPI)
 - Master or slave mode operation
 - Full-duplex or single-wire bidirectional option
 - Programmable transmit bit rate

MCF51AC256 Family Configurations

- Double-buffered transmit and receive
- Serial clock phase and polarity options
- Slave select output
- Selectable MSB-first or LSB-first shifting
- 16-bit and FIFO operations in SPI2
- Input/Output
 - 69 GPIOs
 - 8 keyboard interrupt pins with selectable polarity
 - Hysteresis and configurable pull-up device on all input pins; Configurable slew rate and drive strength on all output pins
 - 16-bits Rapid GPIO pins connected to the processor's local 32-bit platform bus with set, clear, and faster toggle functionality

1.4 Part Numbers

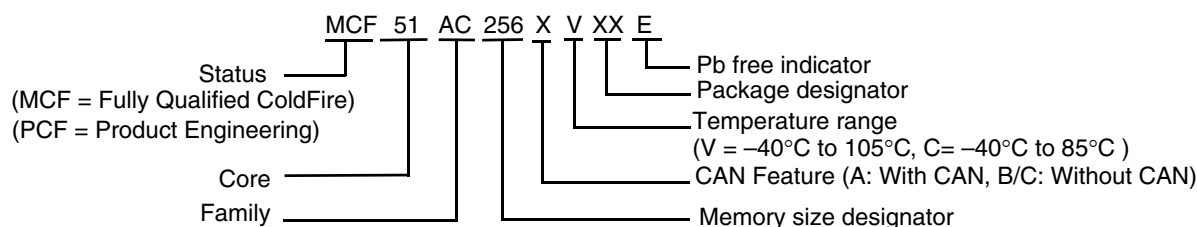
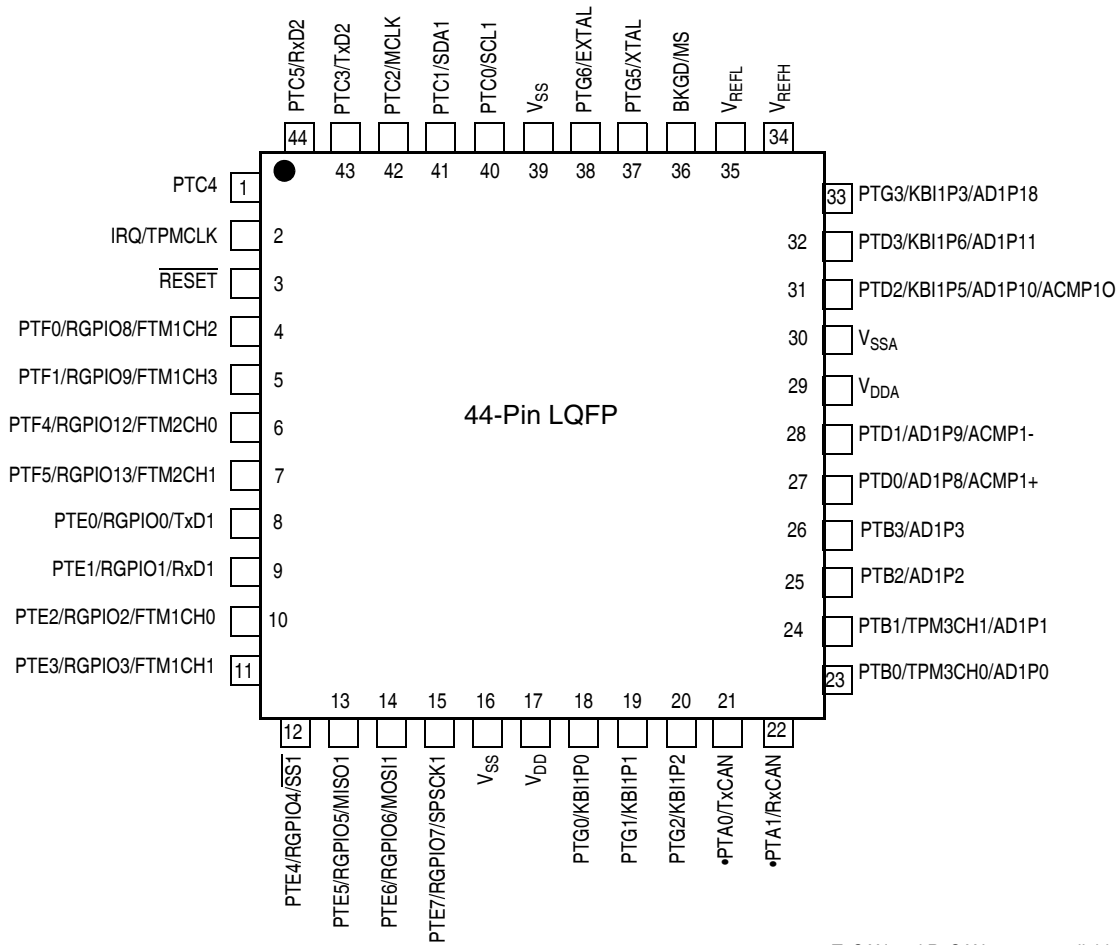


Table 3. Orderable Part Number Summary

Freescall Part Number	Description	Flash / SRAM (Kbytes)	Package	Temperature
MCF51AC256AVFUE	MCF51AC256 ColdFire Microcontroller with CAN	256 / 32	64 QFP	-40°C to 105°C
MCF51AC256BVFUE	MCF51AC256 ColdFire Microcontroller without CAN	256 / 32	64 QFP	-40°C to 105°C
MCF51AC256AVLKE	MCF51AC256 ColdFire Microcontroller with CAN	256 / 32	80 LQFP	-40°C to 105°C
MCF51AC256BVLKE	MCF51AC256 ColdFire Microcontroller without CAN	256 / 32	80 LQFP	-40°C to 105°C
MCF51AC256AVPUE	MCF51AC256 ColdFire Microcontroller with CAN	256 / 32	64 LQFP	-40°C to 105°C
MCF51AC256BVPUE	MCF51AC256 ColdFire Microcontroller without CAN	256 / 32	64 LQFP	-40°C to 105°C
MCF51AC128AVFUE	MCF51AC128 ColdFire Microcontroller with CAN	128 / 32	64 QFP	-40°C to 105°C
MCF51AC128CVFUE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	64 QFP	-40°C to 105°C
MCF51AC128AVLKE	MCF51AC128 ColdFire Microcontroller with CAN	128 / 32	80 LQFP	-40°C to 105°C
MCF51AC128CVLKE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	80 LQFP	-40°C to 105°C
MCF51AC128AVPUE	MCF51AC128 ColdFire Microcontroller with CAN	128 / 32	64 LQFP	-40°C to 105°C
MCF51AC128CVPUE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	64 LQFP	-40°C to 105°C
MCF51AC256ACFUE	MCF51AC256 ColdFire Microcontroller with CAN	256 / 32	64 QFP	-40°C to 85°C
MCF51AC256BCFUE	MCF51AC256 ColdFire Microcontroller without CAN	256 / 32	64 QFP	-40°C to 85°C
MCF51AC256ACLKE	MCF51AC256 ColdFire Microcontroller with CAN	256 / 32	80 LQFP	-40°C to 85°C
MCF51AC256BCLKE	MCF51AC256 ColdFire Microcontroller without CAN	256 / 32	80 LQFP	-40°C to 85°C

Table 3. Orderable Part Number Summary

MCF51AC256ACPUE	MCF51AC256 ColdFire Microcontroller with CAN	256 / 32	64 LQFP	–40°C to 85°C
MCF51AC256BCPUE	MCF51AC256 ColdFire Microcontroller without CAN	256 / 32	64 LQFP	–40°C to 85°C
MCF51AC256BCFGE	MCF51AC256 ColdFire Microcontroller without CAN	256/32	44 LQFP	–40°C to 85°C
MCF51AC128ACFUE	MCF51AC128 ColdFire Microcontroller with CAN	128 / 32	64 QFP	–40°C to 85°C
MCF51AC128CCFUE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	64 QFP	–40°C to 85°C
MCF51AC128ACLKE	MCF51AC128 ColdFire Microcontroller with CAN	128 / 32	80 LQFP	–40°C to 85°C
MCF51AC128CCLKE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	80 LQFP	–40°C to 85°C
MCF51AC128ACPUE	MCF51AC128 ColdFire Microcontroller with CAN	128 / 32	64 LQFP	–40°C to 85°C
MCF51AC128CCPUE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	64 LQFP	–40°C to 85°C
MCF51AC128CCFGE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	44 LQFP	–40°C to 85°C



• TxCAN and RxCAN are not available in the members that do not support CAN

Figure 4. MCF51AC256 Series ColdFire Microcontroller 44-Pin LQFP

Table 4 shows the package pin assignments.

Table 4. Pin Availability by Package Pin-Count

Pin Number			Lowest <-- Priority --> Highest			
80	64	44	Port Pin	Alt 1	Alt 2	Alt 3
1	1	1	PTC4	SS2		
2	2	2	IRQ	TPMCLK ¹		
3	3	3	RESET			
4	4	4	PTF0	RGPIO8	FTM1CH2	
5	5	5	PTF1	RGPIO9	FTM1CH3	
6	6	—	PTF2	RGPIO10	FTM1CH4	
7	7	—	PTF3	RGPIO11	FTM1CH5	

2 Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the MCF51AC256 microcontroller, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. These specifications will, however, be met for production silicon. Finalized specifications will be published after complete characterization and device qualifications have been completed.

NOTE

The parameters specified in this data sheet supersede any values found in the module specifications.

2.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 5. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

2.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 6 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}).

Table 6. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	−0.3 to 5.8	V
Input voltage	V_{In}	−0.3 to $V_{DD} + 0.3$	V
Instantaneous maximum current Single pin limit (applies to all port pins) ^{1, 2, 3}	I_D	±25	mA
Maximum current into V_{DD}	I_{DD}	120	mA
Storage temperature	T_{stg}	−55 to 150	°C

¹ Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

² All functional non-supply pins are internally clamped to V_{SS} and V_{DD} .

³ Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD} , the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low which would reduce overall power consumption.

2.3 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and it is user-determined rather than being controlled by the MCU design. In order to take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 7. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	−40 to 105	°C
Maximum junction temperature	T_J	150	°C
Thermal resistance ^{1,2,3,4}			
80-pin LQFP			
1s		51	
2s2p		38	
64-pin LQFP			
1s		59	
2s2p	θ_{JA}	41	°C/W
64-pin QFP			
1s		50	
2s2p		36	
44-pin LQFP			
1s		67	
2s2p		45	

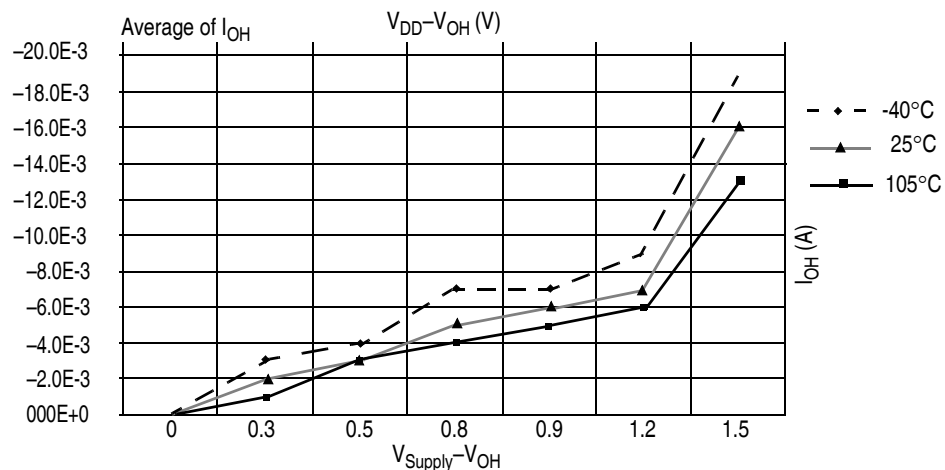


Figure 6. Typical I_{OH} vs. $V_{DD} - V_{OH}$ at $V_{DD} = 3$ V (High Drive, PTxDSn = 1)

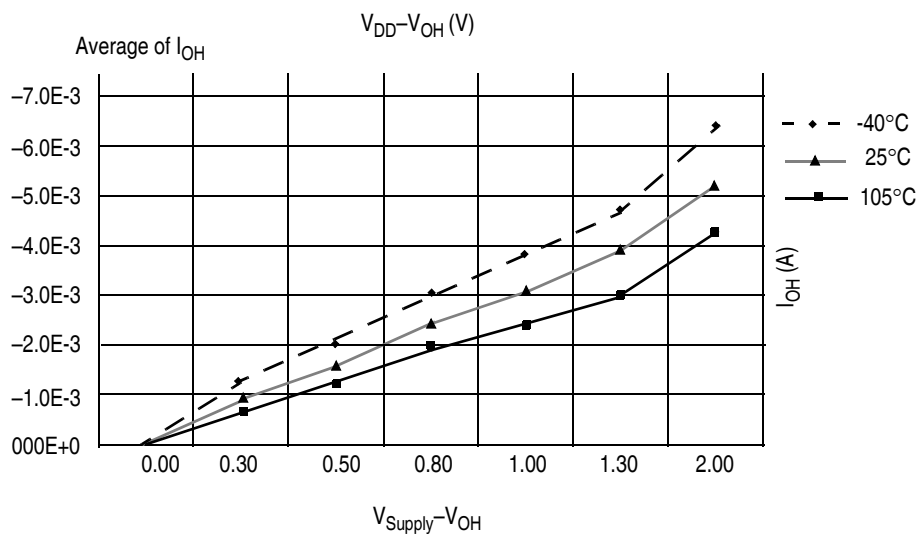


Figure 7. Typical I_{OH} vs. $V_{DD} - V_{OH}$ at $V_{DD} = 5$ V (Low Drive, PTxDSn = 0)

Figure 9. Typical Run I_{DD} vs. System Clock Freq. for FEI and FBE Modes

2.7 Analog Comparator (ACMP) Electricals

Table 12. Analog Comparator Electrical Specifications

Num	C	Rating	Symbol	Min	Typical	Max	Unit
1	—	Supply voltage	V_{DD}	2.7	—	5.5	V
2	T	Supply current (active)	I_{DDAC}	—	20	35	μA
3	D	Analog input voltage	V_{AIN}	$V_{SS} - 0.3$	—	V_{DD}	V
4	D	Analog input offset voltage	V_{AIO}	—	20	40	mV
5	D	Analog comparator hysteresis	V_H	3.0	6.0	20.0	mV
6	D	Analog input leakage current	I_{ALKG}	—	—	1.0	μA
7	D	Analog comparator initialization delay	t_{AINIT}	—	—	1.0	μs
8	P	Bandgap voltage reference factory trimmed at $V_{DD} = 5.3248$ V, Temp = 25 °C	V_{BG}	1.18	1.20	1.21	V

2.8 ADC Characteristics

Table 13. 5 Volt 12-bit ADC Operating Conditions

Num	C	Characteristic	Conditions	Symb	Min	Typical ¹	Max	Unit	Comment
1	D	Supply voltage	Absolute	V_{DDA}	2.7	—	5.5	V	
	D		Delta to V_{DD} ($V_{DD} - V_{DDA}$) ²	ΔV_{DDA}	−100	0	100	mV	
2	D	Ground voltage	Delta to V_{SS} ($V_{SS} - V_{SSA}$) ²	ΔV_{SSA}	−100	0	100	mV	
3	D	Reference voltage high		V_{REFH}	2.7	V_{DDA}	V_{DDA}	V	
4	D	Reference voltage low		V_{REFL}	V_{SSA}	V_{SSA}	V_{SSA}	V	
5	D	Input voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
6	C	Input capacitance		C_{ADIN}	—	4.5	5.5	pF	
7	C	Input resistance		R_{ADIN}	—	3	5	k Ω	
8	C	Analog source resistance	12-bit mode $f_{ADCK} > 4\text{MHz}$ $f_{ADCK} < 4\text{MHz}$	R_{AS}	— —	— —	2 5	k Ω	External to MCU
	C		10-bit mode $f_{ADCK} > 4\text{MHz}$ $f_{ADCK} < 4\text{MHz}$		— —	— —	5 10		
	C		8-bit mode (all valid f_{ADCK})		—	—	10		
9	D	ADC conversion clock frequency	High speed (ADLPC = 0)	f_{ADCK}	0.4	—	8.0	MHz	
	D		Low power (ADLPC = 1)		0.4	—	4.0		

¹ Typical values assume $V_{DDA} = 5.0\text{ V}$, Temp = 25 °C, $f_{ADCK} = 1.0\text{ MHz}$ unless otherwise stated. Typical values are for reference only and are not tested in production.

² DC potential difference.

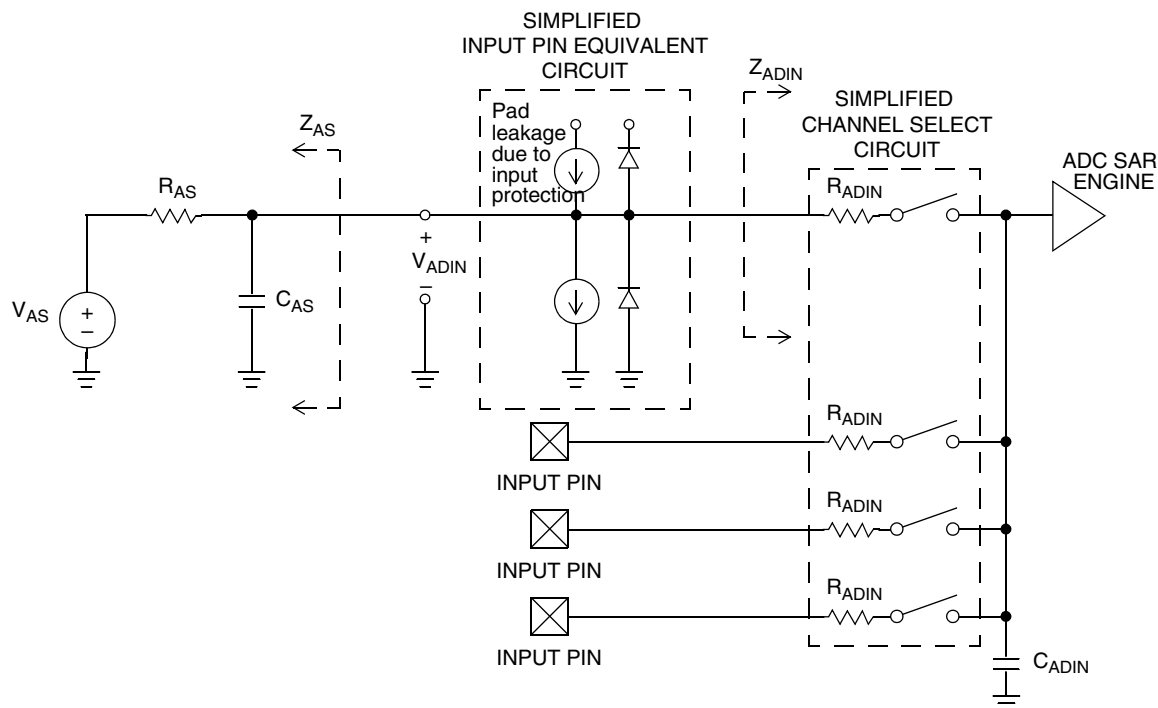


Figure 10. ADC Input Impedance Equivalency Diagram

Table 14. 5 Volt 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Num	C	Characteristic	Conditions	Symb	Min	Typical ¹	Max	Unit	Comment
1	T	Supply current ADLPC = 1 ADLSMP = 1 ADCO = 1		I_{DDA}	—	133	—	μA	
2	T	Supply current ADLPC = 1 ADLSM = 0 ADCO = 1		I_{DDA}	—	218	—	μA	
3	T	Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1		I_{DDA}	—	327	—	μA	
4	D	Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1		I_{DDA}	—	0.582	1	mA	
5	T	Supply current	Stop, reset, module off	I_{DDA}	—	0.011	1	μA	
6	P	ADC asynchronous clock source	High speed (ADLPC = 0)	f_{ADACK}	2	3.3	5	MHz	$t_{ADACK} = 1/f_{ADACK}$
			Low power (ADLPC = 1)		1.25	2	3.3		

Table 14. 5 Volt 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Num	C	Characteristic	Conditions	Symb	Min	Typical ¹	Max	Unit	Comment
7	P	Conversion time (including sample time)	Short sample (ADLSMP = 0)	t_{ADC}	—	20	—	ADCK cycles	See Table 10 for conversion time variances
			Long sample (ADLSMP = 1)		—	40	—		
8	T	Sample time	Short sample (ADLSMP = 0)	t_{ADS}	—	3.5	—	ADCK cycles	
			Long sample (ADLSMP = 1)		—	23.5	—		
9	T	Total unadjusted error	12-bit mode	E_{TUE}	—	±3.0	—	LSB ²	Includes quantization
	P		10-bit mode		—	±1	±2.5		
	T		8-bit mode		—	±0.5	±1.0		
10	T	Differential non-linearity	12-bit mode	DNL	—	±1.75	—	LSB ²	
	P		10-bit mode ³		—	±0.5	±1.0		
	T		8-bit mode ³		—	±0.3	±0.5		
11	T	Integral non-linearity	12-bit mode	INL	—	±1.5	—	LSB ²	
	T		10-bit mode		—	±0.5	±1.0		
	T		8-bit mode		—	±0.3	±0.5		
12	T	Zero-scale error	12-bit mode	E_{ZS}	—	±1.5	—	LSB ²	$V_{ADIN} = V_{SSA}$
	P		10-bit mode		—	±0.5	±1.5		
	T		8-bit mode		—	±0.5	±0.5		
13	T	Full-scale error	12-bit mode	E_{FS}	—	±1	—	LSB ²	$V_{ADIN} = V_{DDA}$
	P		10-bit mode		—	±0.5	±1		
	T		8-bit mode		—	±0.5	±0.5		
14	D	Quantization error	12-bit mode	E_Q	—	−1 to 0	—	LSB ²	
			10-bit mode		—	—	±0.5		
			8-bit mode		—	—	±0.5		
15	D	Input leakage error	12-bit mode	E_{IL}	—	±1	—	LSB ²	Pad leakage ^{4*} R_{AS}
			10-bit mode		—	±0.2	±2.5		
			8-bit mode		—	±0.1	±1		
16	D	Temp sensor voltage	25°C	V_{TEMP25}	—	1.396	—	V	
17	D	Temp sensor slope	−40 °C–25 °C	m	—	3.266	—	mV/°C	
			25 °C–85 °C		—	3.638	—		

¹ Typical values assume $V_{DDA} = 5.0$ V, Temp = 25 °C, $f_{ADCK} = 1.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

² 1 LSB = $(V_{REFH} - V_{REFL})/2^N$.

³ Monotonicity and No-Missing-Codes guaranteed in 10-bit and 8-bit modes

⁴ Based on input pad leakage current. Refer to pad electricals.

2.9 External Oscillator (XOSC) Characteristics

Table 15. Oscillator Electrical Specifications (Temperature Range = –40 to 105 °C Ambient)

Num	C	Rating	Symbol	Min	Typical ¹	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1)					
		Low range (RANGE = 0)	f_{lo}	32	—	38.4	kHz
		High range (RANGE = 1) FEE or FBE mode ²	f_{hi-ll}	1	—	5	MHz
		High range (RANGE = 1) PEE or PBE mode ³	f_{hi-pll}	1	—	16	MHz
		High range (RANGE = 1, HGO = 1) BLPE mode	f_{hi-hgo}	1	—	16	MHz
		High range (RANGE = 1, HGO = 0) BLPE mode	f_{hi-lp}	1	—	8	MHz
2	—	Load capacitors	C_1 C_2	See crystal or resonator manufacturer's recommendation.			
3	—	Feedback resistor	R_F		10		MΩ
		Low range (32 kHz to 38.4 kHz) High range (1 MHz to 16 MHz)			1		
4	—	Series resistor	R_S				kΩ
		Low range, low gain (RANGE = 0, HGO = 0)		—	0	—	
		Low range, high gain (RANGE = 0, HGO = 1)		—	100	—	
		High range, low gain (RANGE = 1, HGO = 0)		—	0	—	
		High range, high gain (RANGE = 1, HGO = 1)		—	0	0	
		≥ 8 MHz		—	0	0	
5	T	Crystal start-up time ⁴					ms
		Low range, low gain (RANGE = 0, HGO = 0)	$t_{CSTL-LP}$	—	200	—	
		Low range, high gain (RANGE = 0, HGO = 1)	$t_{CSTL-HGO}$	—	400	—	
		High range, low gain (RANGE = 1, HGO = 0) ⁵	$t_{CSTH-LP}$	—	5	—	
		High range, high gain (RANGE = 1, HGO = 1) ⁵	$t_{CSTH-HGO}$	—	15	—	
6	T	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1)					MHz
		FEE or FBE mode ²	f_{extal}	0.03125	—	5	
		PEE or PBE mode ³		1	—	16	
		BLPE mode		0	—	40	

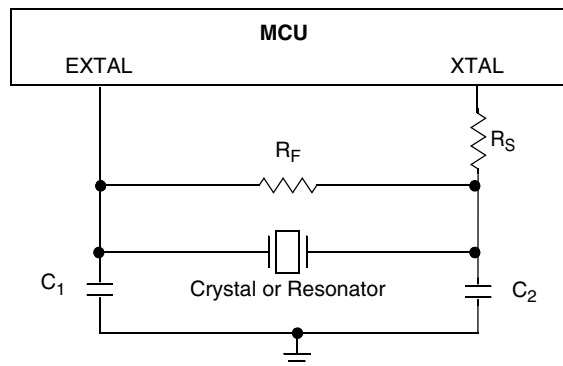
¹ Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.

² When MCG is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.

³ When MCG is configured for PEE or PBE mode, input clock source must be divisible using RDIV to within the range of 1 MHz to 2 MHz.

⁴ This parameter is characterized and not tested on each device. Proper PC board layout procedures must be followed to achieve specifications.

⁵ 4 MHz crystal



2.10 MCG Specifications

Table 16. MCG Frequency Specifications (Temperature Range = -40 to 105 °C Ambient)

Num	C	Rating	Symbol	Min	Typical ¹	Max	Unit
1	C	Internal reference frequency — factory trimmed at $V_{DD} = 5\text{ V}$ and temperature = 25 °C	f_{int_ft}	—	32.768	—	kHz
2	C	Average internal reference frequency — untrimmed	f_{int_ut}	31.25	—	39.0625	kHz
3	T	Internal reference startup time	t_{irefst}	—	60	100	μs
4	C	DCO output frequency range — untrimmed ²	f_{dco_ut}	16	—	20	MHz
	C			32	—	40	
	C			48	—	60	
5	P	DCO output frequency ² reference = 32768Hz and DMX32 = 1	f_{dco_DMX32}	—	16.82	—	MHz
	P			—	33.69	—	
	P			—	50.48	—	
6	D	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)	$\Delta f_{dco_res_t}$	—	±0.1	±0.2	% f_{dco}
7	D	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)	$\Delta f_{dco_res_t}$	—	±0.2	±0.4	% f_{dco}
8	D	Total deviation of trimmed DCO output frequency over voltage and temperature	Δf_{dco_t}	—	0.5 -1.0	±2	% f_{dco}
9	D	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0–70 °C	Δf_{dco_t}	—	±0.5	±1	% f_{dco}
10	D	FLL acquisition time ³	$t_{fll_acquire}$	—	—	1	ms
11	D	PLL acquisition time ⁴	$t_{pll_acquire}$	—	—	1	ms
12	D	Long term jitter of DCO output clock (averaged over 2ms interval) ⁵	C_{jitter}	—	0.02	0.2	% f_{dco}
13	D	VCO operating frequency	f_{vco}	7.0	—	55.0	MHz
16	D	Jitter of PLL output clock measured over 625 ns ⁶	$f_{pll_jitter_625ns}$	—	0.566 ⁶	—	% f_{pll}
17	D	Lock entry frequency tolerance ⁷	D_{lock}	±1.49	—	±2.98	%

Table 16. MCG Frequency Specifications (continued)(Temperature Range = –40 to 105 °C Ambient)

Num	C	Rating	Symbol	Min	Typical ¹	Max	Unit
18	D	Lock exit frequency tolerance ⁸	D _{unl}	±4.47	—	±5.97	%
19	D	Lock time — FLL	t _{fil_lock}	—	—	t _{fil_acquire} + 1075(1/f _{int_t})	s
20	D	Lock time — PLL	t _{pll_lock}	—	—	t _{pll_acquire} + 1075(1/f _{pll_ref})	s
21	D	Loss of external clock minimum frequency — RANGE = 0	f _{loc_low}	(3/5) × f _{int}	—	—	kHz

¹ Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.

² The resulting bus clock frequency must not exceed the maximum specified bus clock frequency of the device.

³ This specification applies when the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

⁴ This specification applies when the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

⁵ Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

⁶ 625 ns represents 5 time quanta for CAN applications, under worst case conditions of 8 MHz CAN bus clock, 1 Mbps CAN bus speed, and 8 time quanta per bit for bit time settings. 5 time quanta is the minimum time between a synchronization edge and the sample point of a bit using 8 time quanta per bit.

⁷ Below D_{lock} minimum, the MCG enters lock. Above D_{lock} maximum, the MCG will not enter lock. But if the MCG is already in lock, then the MCG may stay in lock.

⁸ Below D_{unl} minimum, the MCG will not exit lock if already in lock. Above D_{unl} maximum, the MCG is guaranteed to exit lock.

2.11 AC Characteristics

This section describes ac timing characteristics for each peripheral system.

2.11.1 Control Timing

Table 17. Control Timing

Num	C	Parameter	Symbol	Min	Typical ¹	Max	Unit
1	D	Bus frequency ($t_{cyc} = 1/f_{Bus}$)	f_{Bus}	dc	—	24	MHz
2	D	Internal low-power oscillator period	t_{LPO}	800	—	1500	μs
3	D	External reset pulse width ² ($t_{cyc} = 1/f_{Self_reset}$)	t_{extrst}	100	—	—	ns
4	D	Reset low drive	t_{rstdrv}	$66 \times t_{cyc}$	—	—	ns
5	D	Active background debug mode latch setup time	t_{MSSU}	500	—	—	ns
6	D	Active background debug mode latch hold time	t_{MSH}	100	—	—	ns
7	D	IRQ pulse width Asynchronous path ² Synchronous path ³	t_{ILIH}, t_{IHIL}	100 $1.5 \times t_{cyc}$	—	—	ns
8	D	KBIPx pulse width Asynchronous path ² Synchronous path ³	t_{ILIH}, t_{IHIL}	100 $1.5 \times t_{cyc}$	—	—	ns
9	D	Port rise and fall time (load = 50 pF) ⁴ Slew rate control disabled (PTxSE = 0), Low Drive Slew rate control enabled (PTxSE = 1), Low Drive Slew rate control disabled (PTxSE = 0), Low Drive Slew rate control enabled (PTxSE = 1), Low Drive	t_{Rise}, t_{Fall}	— — — —	11 35 40 75	—	ns

¹ Typical values are based on characterization data at $V_{DD} = 5.0 V$, 25 °C unless otherwise stated.

² This is the shortest pulse that is guaranteed to be recognized as a reset pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

³ This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

⁴ Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40 °C to 105 °C.

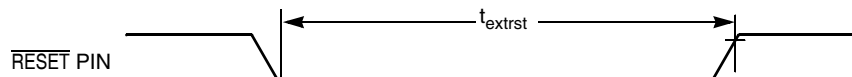


Figure 11. Reset Timing

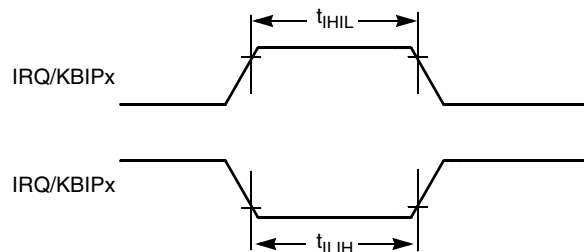
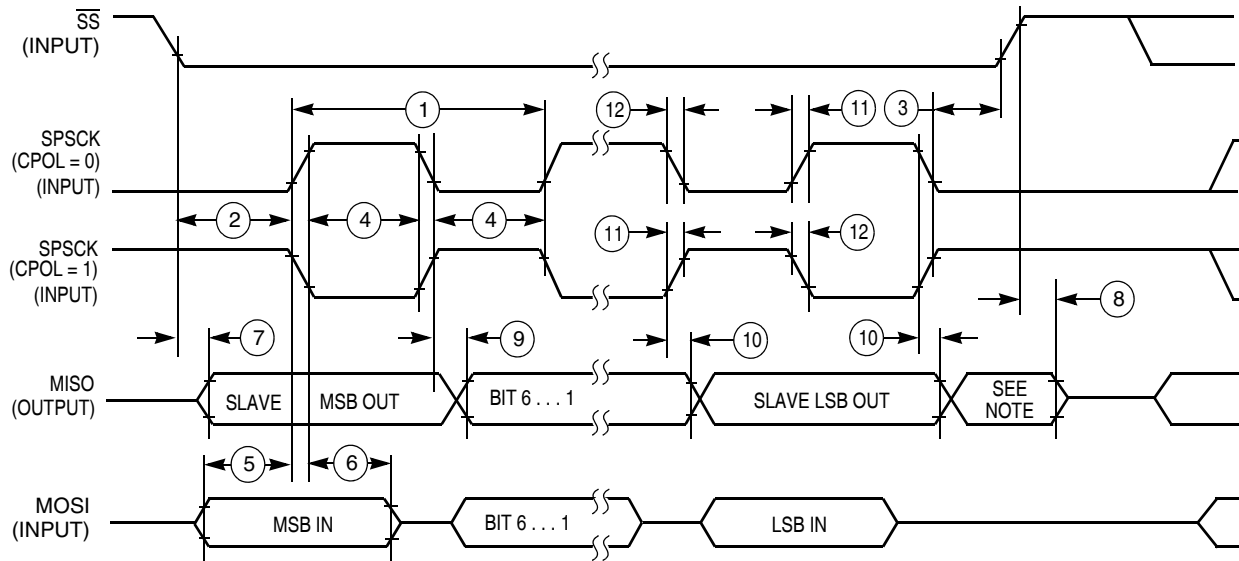


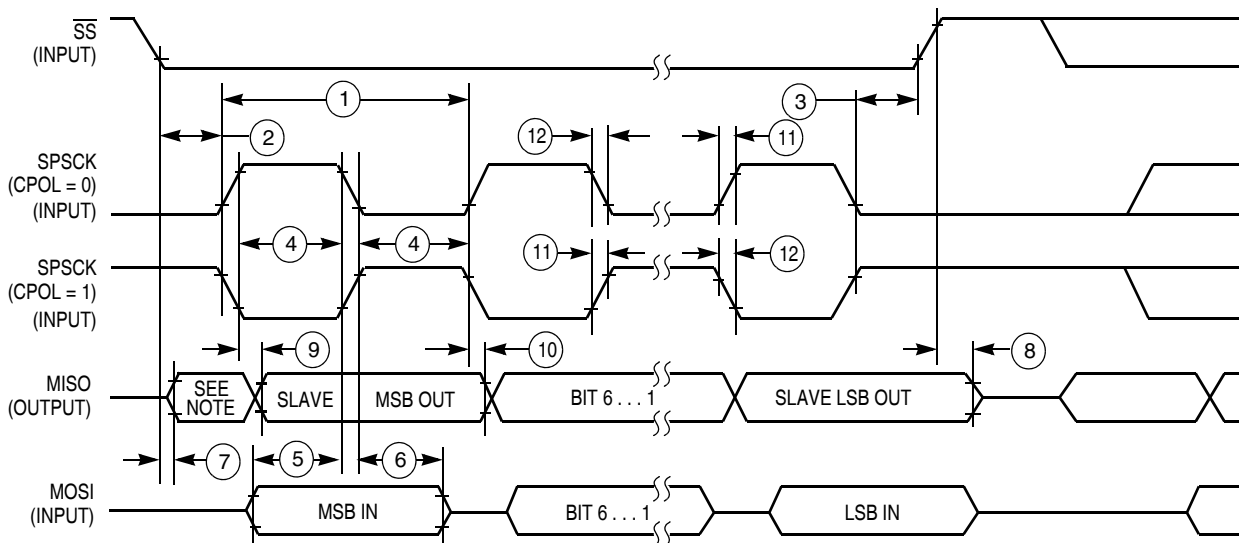
Figure 12. IRQ/KBIPx Timing



NOTE:

1. Not defined but normally MSB of character just received

Figure 17. SPI Slave Timing (CPHA = 0)



NOTE:

1. Not defined but normally LSB of character just received

Figure 18. SPI Slave Timing (CPHA = 1)

2.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the Flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see Chapter 4, “Memory.”

3 Mechanical Outline Drawings

Table 22 provides the available package types and their document numbers. The latest package outline/mechanical drawings are available on the MCF51AC256 Series Product Summary pages at <http://www.freescale.com>.

To view the latest drawing, either:

- Click on the appropriate link in Table 22, or
- Open a browser to the Freescale website (<http://www.freescale.com>), and enter the appropriate document number (from Table 22) in the “Enter Keyword” search box at the top of the page.

Table 22. Package Information

Pin Count	Type	Document No.
80	LQFP	98ARL10530D
64	LQFP	98ASS23234W
64	QFP	98ASB42844B
44	LQFP	98ASS23225W

4 Revision History

Table 23. Revision History

Revision	Description
1	Initial published
2	Updated ADC channels, Item 1, 4-5 on Table 2.10
3	Completed all the TBDs. Changed RTC to RTI in Figure 1. Corrected the block diagram. Changed V_{DDAD} to V_{DDA} , V_{SSAD} to V_{SSA} . Added charge device model data and removed machine data in Table 8. Updated the specifications of V_{LVDH} , V_{LVDL} , V_{LVWH} and V_{LVWL} in Table 10. Updated $S2I_{DD}$, $S3I_{DD}$ in Table 11. Added C column in Table 14. Updated f_{dco_DMX32} in Table 16.
4	Corrected the expansion of SPI to serial peripheral interface.
5	Updated V_{LVDL} in the Table 10. Updated RI_{DD} in the Table 11.
6	Updated V_{LVDH} , V_{LVDL} , V_{LVWH} and V_{LVWL} in the Table 10. Added LPO on the Figure 1 and LPO features in the Section 1.3, "Features."
7	Added 44-pin LQFP package information for AC256 and AC128.