NXP USA Inc. - MCF51AC256BVLKE Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I^2C, SCI, SPI
Peripherals	LVD, PWM, WDT
Number of I/O	69
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf51ac256bvlke

1 MCF51AC256 Family Configurations

1.1 Device Comparison

The MCF51AC256 series is summarized in Table 1.

Table 1. MCF51AC256 Series Device Comparison

Feature	MCF51AC256A		MCF51AC256B			MCF51AC128A		MCF51AC128C		
	80-pin	64-pin	80-pin	64-pin	44-pin	80-pin	64-pin	80-pin	64-pin	44-pin
Flash memory size (Kbytes)	256					128				
RAM size (Kbytes)	32					32 or 16[1]				
V1 ColdFire core with BDM (background debug module)	Yes									
ACMP1 (analog comparator)	Yes									
ACMP2 (analog comparator)	Yes		Yes		No	Yes				No
ADC (analog-to-digital converter) channels (12-bit)	24	20	24	20	9	24	20	24	20	9
CAN (controller area network)	Yes		No			Yes		No		
COP (computer operating properly)	Yes									
CRC (cyclic redundancy check)	Yes									
RTI	Yes									
DBG (debug)	Yes									
IIC1 (inter-integrated circuit)	Yes									
IRQ (interrupt request input)	Yes									
INTC (interrupt controller)	Yes									
KBI (keyboard interrupts)	Yes									
LVD (low-voltage detector)	Yes									
MCG (multipurpose clock generator)	Yes									
OSC (crystal oscillator)	Yes									
Port I/O[2]	69	54	69	54	36	69	54	69	54	36
RGPIO (rapid general-purpose I/O)	16				12	16				12
SCI1, SCI2 (serial communications interfaces)	Yes									
SPI1 (serial peripheral interface)	Yes									
SPI2 (serial peripheral interface)	Yes	No	Yes	No		Yes	No	Yes	No	
FTM1 (flexible timer module) channels	6				4	6				4
FTM2 channels	6	2	6	2	2	6	2	6	2	2

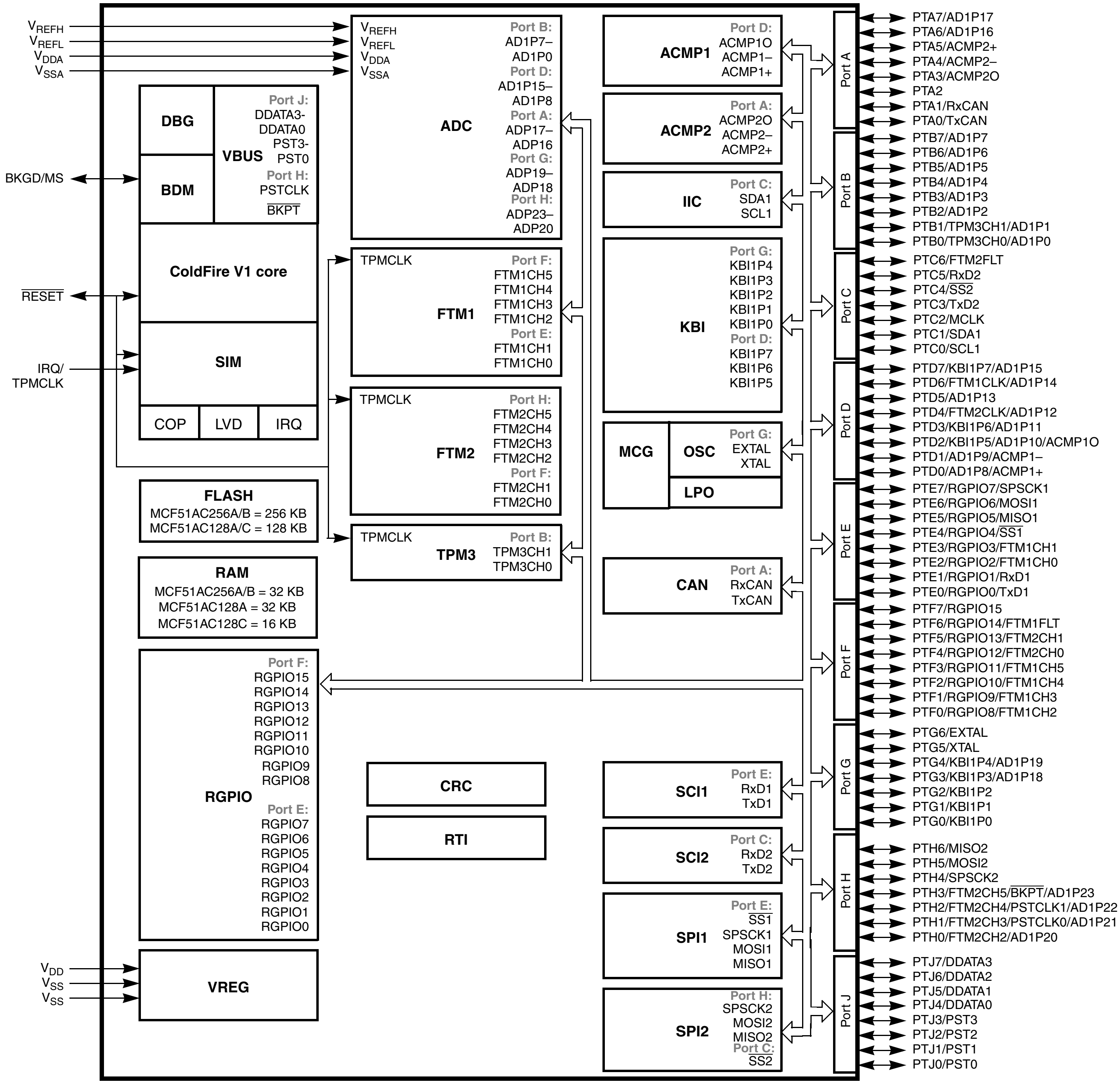


Figure 1. MCF51AC256 Series Block Diagram

1.3 Features

Table 2 describes the functional units of the MCF51AC256 series.

Table 2. MCF51AC256 Series Functional Units

Functional Unit	Function
CF1 Core (V1 ColdFire core)	Executes programs and interrupt handlers
BDM (background debug module)	Provides single pin debugging interface (part of the V1 ColdFire core)
DBG (debug)	Provides debugging and emulation capabilities (part of the V1 ColdFire core)
VBUS (debug visibility bus)	Allows for real-time program traces (part of the V1 ColdFire core)
SIM (system integration module)	Controls resets and chip level interfaces between modules
Flash (flash memory)	Provides storage for program code, constants and variables
RAM (random-access memory)	Provides storage for program variables
RGPIO (rapid general-purpose input/output)	Allows for I/O port access at CPU clock speeds
VREG (voltage regulator)	Controls power management across the device
COP (computer operating properly)	Monitors a countdown timer and generates a reset if the timer is not regularly reset by the software
LVD (low-voltage detect)	Monitors internal and external supply voltage levels, and generates a reset or interrupt when the voltages are too low
CF1_INTC (interrupt controller)	Controls and prioritizes all device interrupts
ADC (analog-to-digital converter)	Measures analog voltages at up to 12 bits of resolution
FTM1, FTM2 (flexible timer/pulse-width modulators)	Provides a variety of timing-based features
TPM3 (timer/pulse-width modulator)	Provides a variety of timing-based features
CRC (cyclic redundancy check)	Accelerates computation of CRC values for ranges of memory
ACMP1, ACMP2 (analog comparators)	Compares two analog inputs
IIC (inter-integrated circuit)	Supports standard IIC communications protocol
KBI (keyboard interrupt)	Provides pin interrupt capabilities
MCG (multipurpose clock generator)	Provides clocking options for the device, including a phase-locked loop (PLL) and frequency-locked loop (FLL) for multiplying slower reference clock sources
OSC (crystal oscillator)	Allows a crystal or ceramic resonator to be used as the system clock source or reference clock for the PLL or FLL
LPO (low-power oscillator)	Provides a second clock source for COP and RTI.
CAN (controller area network)	Supports standard CAN communications protocol
SCI1, SCI2 (serial communications interfaces)	Serial communications UARTs capable of supporting RS-232 and LIN protocols
SPI1 (8-bit serial peripheral interfaces)	Provides 8-bit 4-pin synchronous serial interface
SPI2 (16-bit serial peripheral interfaces)	Provides 16-bit 4-pin synchronous serial interface with FIFO

1.3.1 Feature List

- 32-bit Version 1 ColdFire® central processor unit (CPU)
  - Up to 50.33 MHz at 2.7 V – 5.5 V
  - Provide 0.94 Dhrystone 2.1 DMIPS per MHz performance when running from internal RAM (0.76 DMIPS per MHz when running from flash)
  - Implements instruction set revision C (ISA_C)
- On-chip memory
  - Up to 256 KB flash memory read/program/erase over full operating voltage and temperature
  - Up to 32 KB static random access memory (SRAM)
  - Security circuitry to prevent unauthorized access to SRAM and flash contents
- Power-Saving Modes
  - Three low-power stop plus wait modes
  - Peripheral clock enable register can disable clocks to unused modules, reducing currents; allows clocks to remain enabled to specific peripherals in stop3 mode
- System protection features
  - Watchdog computer operating properly (COP) reset with options to run from independent LPO clock or bus clock
  - Low-voltage detection with reset or interrupt
  - Illegal opcode and illegal address detection with programmable reset or exception response
  - Flash block protection
- Debug support
  - Single-wire background debug interface
  - Real-time debug support, with 6 hardware breakpoints (4 PC, 1 address pair and 1 data) that can be configured into a 1- or 2-level trigger
  - On-chip trace buffer provides programmable start/stop recording conditions plus support for continuous or PC-profiling modes
  - Support for real-time program (and optional partial data) trace using the debug visibility bus
- V1 ColdFire interrupt controller (CF1_INTC)
  - Support of 40 peripheral I/O interrupt requests plus seven software (one per level) interrupt requests
  - Fixed association between interrupt request source and level plus priority, up to two requests can be remapped to the highest maskable level + priority
  - Unique vector number for each interrupt source
  - Support for service routine interrupt acknowledge (software IACK) read cycles for improved system performance
- Multipurpose clock generator (MCG)
  - Oscillator (XOSC); loop-control Pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
  - LPO clock as an optional independent clock source for COP and RTI
  - FLL/PLL controlled by internal or external reference

- — Trimmable internal reference allows 0.2% resolution and 2% deviation
- Analog-to-digital converter (ADC)
  - — 24 analog inputs with 12 bits resolution
  - — Output formatted in 12-, 10- or 8-bit right-justified format
  - — Single or continuous conversion (automatic return to idle after single conversion)
  - — Operation in low-power modes for lower noise operation
  - — Asynchronous clock source for lower noise operation
  - — Automatic compare with interrupt for less-than, or greater-than or equal-to, programmable value
  - — On-chip temperature sensor
- Flexible timer/pulse-width modulators (FTM)
  - — 16-bit Free-running counter or a counter with initial and final value. The counting can be up and unsigned, up and signed, or up-down and unsigned
  - — Up to 6 channels, and each channel can be configured for input capture, output compare or edge-aligned PWM mode, all channels can be configured for center-aligned PWM mode
    - – Channels can operate as pairs with equal outputs, pairs with complimentary outputs or independent channels (with independent outputs)
    - – Each pair of channels can be combined to generate a PWM signal (with independent control of both edges of PWM signal)
    - – Deadtime insertion is available for each complementary pair
  - — The load of the FTM registers which have write buffer can be synchronized; write protection for critical registers
  - — Generation of the triggers to ADC (hardware trigger)
  - — A fault input for global fault control
  - — Backwards compatible with TPM
- Timer/pulse width modulator (TPM)
  - — 16-bit free-running or modulo up/down count operation
  - — Two channels, each channel may be input capture, output compare, or edge-aligned PWM
  - — One interrupt per channel plus terminal count interrupt
- Cyclic redundancy check (CRC) generator
  - — High speed hardware CRC generator circuit using 16-bit shift register
  - — CRC16-CCITT compliancy with $x^{16} + x^{12} + x^5 + 1$ polynomial
  - — Error detection for all single, double, odd, and most multi-bit errors
  - — Programmable initial seed value
- Analog comparators (ACMP)
  - — Full rail to rail supply operation
  - — Selectable interrupt on rising edge, falling edge, or either rising or falling edges of comparator output
  - — Option to compare to fixed internal bandgap reference voltage
  - — Option to allow comparator output to be visible on a pin, ACMPxO

- — Double-buffered transmit and receive
- — Serial clock phase and polarity options
- — Slave select output
- — Selectable MSB-first or LSB-first shifting
- — 16-bit and FIFO operations in SPI2

- Input/Output
  - — 69 GPIOs
  - — 8 keyboard interrupt pins with selectable polarity
  - — Hysteresis and configurable pull-up device on all input pins; Configurable slew rate and drive strength on all output pins
  - — 16-bits Rapid GPIO pins connected to the processor’s local 32-bit platform bus with set, clear, and faster toggle functionality

1.4 Part Numbers

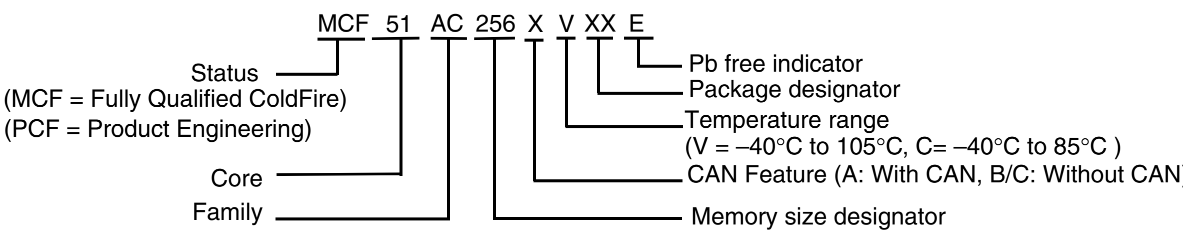


Table 3. Orderable Part Number Summary

Freescale Part Number	Description	Flash / SRAM (Kbytes)	Package	Temperature
MCF51AC256AVFUE	MCF51AC256 ColdFire Microcontroller with CAN	256 / 32	64 QFP	–40°C to 105°C
MCF51AC256BVFUE	MCF51AC256 ColdFire Microcontroller without CAN	256 / 32	64 QFP	–40°C to 105°C
MCF51AC256AVLKE	MCF51AC256 ColdFire Microcontroller with CAN	256 / 32	80 LQFP	–40°C to 105°C
MCF51AC256BVLKE	MCF51AC256 ColdFire Microcontroller without CAN	256 / 32	80 LQFP	–40°C to 105°C
MCF51AC256AVPUE	MCF51AC256 ColdFire Microcontroller with CAN	256 / 32	64 LQFP	–40°C to 105°C
MCF51AC256BVPUE	MCF51AC256 ColdFire Microcontroller without CAN	256 / 32	64 LQFP	–40°C to 105°C
MCF51AC128AVFUE	MCF51AC128 ColdFire Microcontroller with CAN	128 / 32	64 QFP	–40°C to 105°C
MCF51AC128CVFUE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	64 QFP	–40°C to 105°C
MCF51AC128AVLKE	MCF51AC128 ColdFire Microcontroller with CAN	128 / 32	80 LQFP	–40°C to 105°C
MCF51AC128CVLKE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	80 LQFP	–40°C to 105°C
MCF51AC128AVPUE	MCF51AC128 ColdFire Microcontroller with CAN	128 / 32	64 LQFP	–40°C to 105°C
MCF51AC128CVPUE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	64 LQFP	–40°C to 105°C
MCF51AC256ACFUE	MCF51AC256 ColdFire Microcontroller with CAN	256 / 32	64 QFP	–40°C to 85°C
MCF51AC256BCFUE	MCF51AC256 ColdFire Microcontroller without CAN	256 / 32	64 QFP	–40°C to 85°C
MCF51AC256ACLKE	MCF51AC256 ColdFire Microcontroller with CAN	256 / 32	80 LQFP	–40°C to 85°C
MCF51AC256BCLKE	MCF51AC256 ColdFire Microcontroller without CAN	256 / 32	80 LQFP	–40°C to 85°C

Table 4. Pin Availability by Package Pin-Count (continued)

Pin Number			Lowest <-- Priority --> Highest			
80	**64**	**44**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**
8	8	6	PTF4	RGPIO12	FTM2CH0	
9	9	—	PTC6	FTM2FLT		
10	10	—	PTF7	RGPIO15		
11	11	7	PTF5	RGPIO13	FTM2CH1	
12	12	—	PTF6	RGPIO14	FTM1FLT	
13	—	—	PTJ0	PST0		
14	—	—	PTJ1	PST1		
15	—	—	PTJ2	PST2		
16	—	—	PTJ3	PST3		
17	13	8	PTE0	RGPIO0	TxD1	
18	14	9	PTE1	RGPIO1	RxD1	
19	15	10	PTE2	RGPIO2	FTM1CH0	
20	16	11	PTE3	RGPIO3	FTM1CH1	
21	17	12	PTE4	RGPIO4	$\overline{SS1}$	
22	18	13	PTE5	RGPIO5	MISO1	
23	19	14	PTE6	RGPIO6	MOSI1	
24	20	15	PTE7	RGPIO7	SPSCK1	
25	21	16	V_{SS}			
26	22	17	V_{DD}			
27	—	—	PTJ4	DDATA0		
28	—	—	PTJ5	DDATA1		
29	—	—	PTJ6	DDATA2		
30	—	—	PTJ7	DDATA3		
31	23	18	PTG0	KBI1P0		
32	24	19	PTG1	KBI1P1		
33	25	20	PTG2	KBI1P2		
34	26	21	PTA0	TxCAN[2]		
35	27	22	PTA1	RxCAN[3]		
36	28	—	PTA2			
37	29	—	PTA3	ACMP2O		
38	30	—	PTA4	ACMP2–		
39	31	—	PTA5	ACMP2+		
40	32	—	PTA6	AD1P16		
41	33	—	PTA7	AD1P17		
42	—	—	PTH0	FTM2CH2	AD1P20	
43	—	—	PTH1	FTM2CH3	PSTCLK0	AD1P21
44	—	—	PTH2	FTM2CH4	PSTCLK1	AD1P22
45	—	—	PTH3	FTM2CH5	BKPT	AD1P23
46	34	23	PTB0	TPM3CH0	AD1P0	
47	35	24	PTB1	TPM3CH1	AD1P1	
48	36	25	PTB2	AD1P2		

Table 4. Pin Availability by Package Pin-Count (continued)

Pin Number			Lowest <-- Priority --> Highest			
80	**64**	**44**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**
49	37	26	PTB3	AD1P3		
50	38	—	PTB4	AD1P4		
51	39	—	PTB5	AD1P5		
52	40	—	PTB6	AD1P6		
53	41	—	PTB7	AD1P7		
54	42	27	PTD0	AD1P8	ACMP1+	
55	43	28	PTD1	AD1P9	ACMP1–	
56	44	29	V_{DDA}			
57	45	30	V_{SSA}			
58	46	31	PTD2	KBI1P5	AD1P10	ACMP1O
59	47	32	PTD3	KBI1P6	AD1P11	
60	48	33	PTG3	KBI1P3	AD1P18	
61	49	—	PTG4	KBI1P4	AD1P19	
62	50	—	PTD4	FTM2CLK	AD1P12	
63	51	—	PTD5	AD1P13		
64	52	—	PTD6	FTM1CLK	AD1P14	
65	53	—	PTD7	KBI1P7	AD1P15	
66	54	34	V_{REFH}			
67	55	35	V_{REFL}			
68	56	36	BKGD	MS		
69	57	37	PTG5	XTAL		
70	58	38	PTG6	EXTAL		
71	59	39	V_{SS}			
72	—	—	V_{DD}			
73	60	40	PTC0	SCL1		
74	61	41	PTC1	SDA1		
75	—	—	PTH4	SPCK2		
76	—	—	PTH5	MOSI2		
77	—	—	PTH6	MISO2		
78	62	42	PTC2	MCLK		
79	63	43	PTC3	TxD2		
80	64	44	PTC5	RxD2		

[1] TPMCLK, FTM1CLK, and FTM2CLK options are configured via software; out of reset, FTM1CLK, FTM2CLK, and TPMCLK are available to FTM1, FTM2, and TPM3 respectively.

[2] TxCAN is available in the member that supports CAN.

[3] RxCAN is available in the member that supports CAN.

Table 10. DC Characteristics (continued)

Num	C	Parameter	Symbol	Min	Typical[1]	Max	Unit
22	D	DC injection current[5 6 7 8] (single pin limit) $V_{IN} > V_{DD}$ $V_{IN} < V_{SS}$	I_{IC}	0 0	—	2 –0.2	mA
		DC injection current (Total MCU limit, includes sum of all stressed pins) $V_{IN} > V_{DD}$ $V_{IN} < V_{SS}$		0 0	—	25 –5	mA

1 Typical values are based on characterization data at 25°C unless otherwise stated.

2 Measured with $V_{In} = V_{DD}$ or V_{SS}.

3 Measured with $V_{In} = V_{SS}$.

4 Measured with $V_{In} = V_{DD}$.

5 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

6 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

7 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

8 The $\overline{\text{RESET}}$ pin does not have a clamp diode to V_{DD}. Do not drive this pin above V_{DD}.

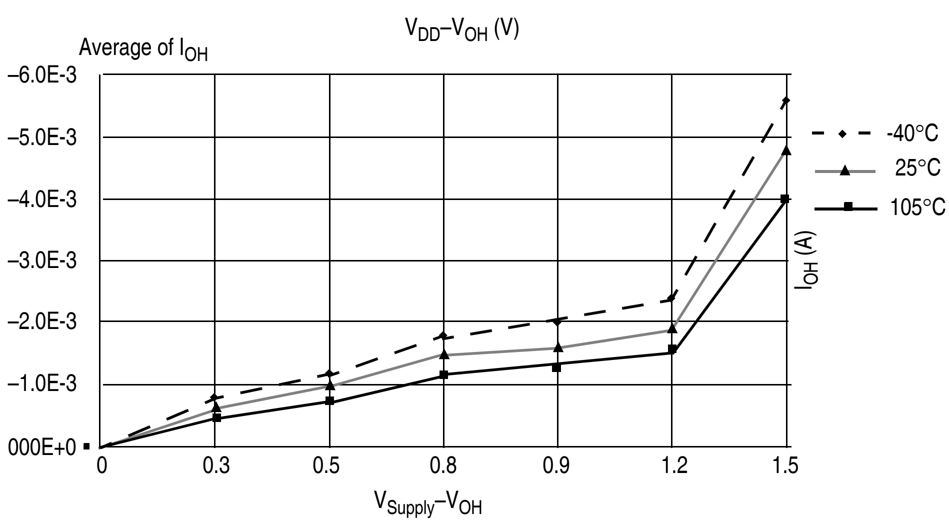


Figure 5. Typical I_{OH} vs. $V_{DD}–V_{OH}$ at V_{DD} = 3 V (Low Drive, PTxDSn = 0)

Table 11. Supply Current Characteristics (continued)

Num	C	Parameter	Symbol	V_{DD} (V)	Typical[1]	Max[2]	Unit
5	C	Wait mode supply[3] current measured at (CPU clock = 2 MHz, f_{Bus} = 1 MHz)	WI_{DD}	5	1.3	2	mA
				3	1.29	2	
6	C	Wait mode supply[3] current measured at (CPU clock = 16 MHz, f_{Bus} = 8 MHz)		5	5.11	8	mA
				3	5.1	8	
7	C	Wait mode supply[3] current measured at (CPU clock = 50 MHz, f_{Bus} = 25 MHz)		5	15.24	25	mA
				3	15.2	25	
8	C	Stop2 mode supply current –40 °C 25 °C 120 °C	$S2I_{DD}$	5	1.40	2.5 2.5 200	µA
		–40 °C 25 °C 120 °C		3	1.16	2.5 2.5 200	µA
9	C	Stop3 mode supply current –40 °C 25 °C 120 °C	$S3I_{DD}$	5	1.60	2.5 2.5 220	µA
		–40 °C 25 °C 120 °C		3	1.35	2.5 2.5 220	µA
10	C	RTI adder to stop2 or stop3[3], 25 °C	$S23I_{DDRTI}$	5	300		nA
				3	300		nA
11	C	Adder to stop3 for oscillator enabled[4] (ERCLKEN =1 and EREFSTEN = 1)	$S3I_{DDOSC}$	5, 3	5		µA

1 Typicals are measured at 25 °C.
2 Values given here are preliminary estimates prior to completing characterization.
3 Most customers are expected to find that auto-wakeup from stop2 or stop3 can be used instead of the higher current wait mode.
4 Values given under the following conditions: low range operation (RANGE = 0), low power mode (HGO = 0).

Figure 9. Typical Run I_{DD} vs. System Clock Freq. for FEI and FBE Modes

2.7 Analog Comparator (ACMP) Electricals

Table 12. Analog Comparator Electrical Specifications

Num	C	Rating	Symbol	Min	Typical	Max	Unit
1	—	Supply voltage	V_{DD}	2.7	—	5.5	V
2	T	Supply current (active)	I_{DDAC}	—	20	35	µA
3	D	Analog input voltage	V_{AIN}	V_{SS} – 0.3	—	V_{DD}	V
4	D	Analog input offset voltage	V_{AIO}	—	20	40	mV
5	D	Analog comparator hysteresis	V_H	3.0	6.0	20.0	mV
6	D	Analog input leakage current	I_{ALKG}	—	—	1.0	µA
7	D	Analog comparator initialization delay	t_{AINIT}	—	—	1.0	µs
8	P	Bandgap voltage reference factory trimmed at V_{DD} = 5.3248 V, Temp = 25 °C	V_{BG}	1.18	1.20	1.21	V

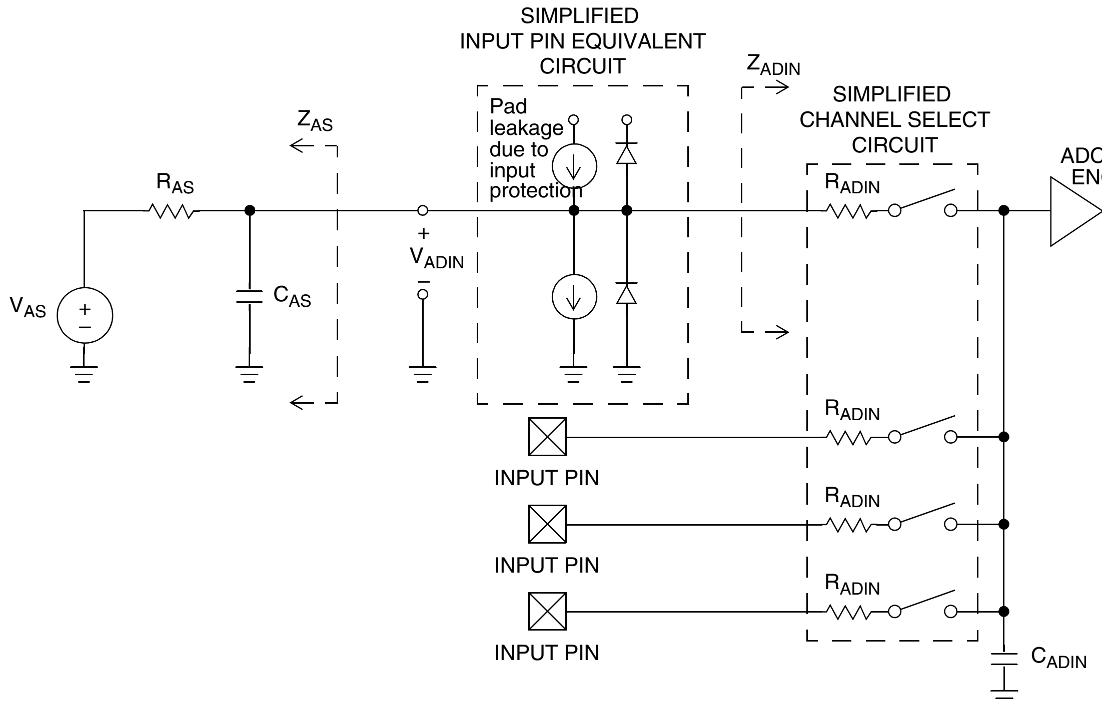


Figure 10. ADC Input Impedance Equivalency Diagram

Table 14. 5 Volt 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Num	C	Characteristic	Conditions	Symb	Min	Typical[1]	Max	Unit	Comment
1	T	Supply current ADLPC = 1 ADLSMP = 1 ADCO = 1		I_{DDA}	—	133	—	μA	
2	T	Supply current ADLPC = 1 ADLSM = 0 ADCO = 1		I_{DDA}	—	218	—	μA	
3	T	Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1		I_{DDA}	—	327	—	μA	
4	D	Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1		I_{DDA}	—	0.582	1	mA	
5	T	Supply current	Stop, reset, module off	I_{DDA}	—	0.011	1	μA	
6	P	ADC asynchronous clock source	High speed (ADLPC = 0)	f_{ADACK}	2	3.3	5	MHz	$t_{ADACK} = 1/f_{ADACK}$
			Low power (ADLPC = 1)		1.25	2	3.3		

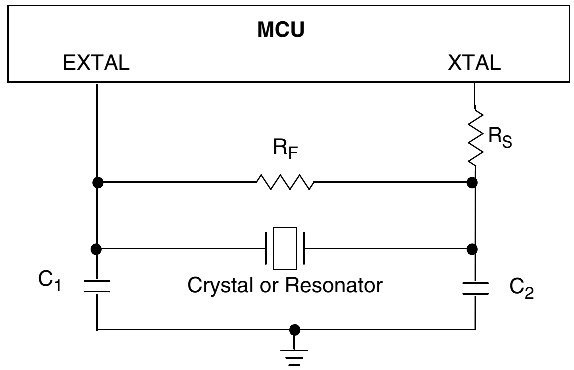
3 Monotonicity and No-Missing-Codes guaranteed in 10-bit and 8-bit modes
4 Based on input pad leakage current. Refer to pad electricals.

2.9 External Oscillator (XOSC) Characteristics

Table 15. Oscillator Electrical Specifications (Temperature Range = –40 to 105 °C Ambient)

Num	C	Rating	Symbol	Min	Typical[1]	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1)					
		Low range (RANGE = 0)	f_{lo}	32	—	38.4	kHz
		High range (RANGE = 1) FEE or FBE mode[2]	$f_{hi\text{-}fll}$	1	—	5	MHz
		High range (RANGE = 1) PEE or PBE mode[3]	$f_{hi\text{-}pll}$	1	—	16	MHz
		High range (RANGE = 1, HGO = 1) BLPE mode	$f_{hi\text{-}hgo}$	1	—	16	MHz
		High range (RANGE = 1, HGO = 0) BLPE mode	$f_{hi\text{-}lp}$	1	—	8	MHz
2	—	Load capacitors	C_1 C_2	See crystal or resonator manufacturer's recommendation.			
3	—	Feedback resistor	R_F				MΩ
		Low range (32 kHz to 38.4 kHz)			10		
		High range (1 MHz to 16 MHz)			1		
4	—	Series resistor	R_S				kΩ
		Low range, low gain (RANGE = 0, HGO = 0)		—	0	—	
		Low range, high gain (RANGE = 0, HGO = 1)		—	100	—	
		High range, low gain (RANGE = 1, HGO = 0)		—	0	—	
		High range, high gain (RANGE = 1, HGO = 1)					
		≥ 8 MHz		—	0	0	
		4 MHz		—	0	10	
		1 MHz		—	0	20	
5	T	Crystal start-up time [4]					ms
		Low range, low gain (RANGE = 0, HGO = 0)	$t_{CSTL\text{-}LP}$	—	200	—	
		Low range, high gain (RANGE = 0, HGO = 1)	$t_{CSTL\text{-}HGO}$	—	400	—	
		High range, low gain (RANGE = 1, HGO = 0)[5]	$t_{CSTH\text{-}LP}$	—	5	—	
		High range, high gain (RANGE = 1, HGO = 1)[5]	$t_{CSTH\text{-}HGO}$	—	15	—	
6	T	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1)	f_{extal}				MHz
		FEE or FBE mode [2]		0.03125	—	5	
		PEE or PBE mode [3]		1	—	16	
		BLPE mode		0	—	40	

1 Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2 When MCG is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.
3 When MCG is configured for PEE or PBE mode, input clock source must be divisible using RDIV to within the range of 1 MHz to 2 MHz.
4 This parameter is characterized and not tested on each device. Proper PC board layout procedures must be followed to achieve specifications.
5 4 MHz crystal



2.10 MCG Specifications

Table 16. MCG Frequency Specifications (Temperature Range = –40 to 105 °C Ambient)

Num	C	Rating		Symbol	Min	Typical[1]	Max	Unit
1	C	Internal reference frequency — factory trimmed at V_{DD} = 5 V and temperature = 25 °C		f_{int_ft}	—	32.768	—	kHz
2	C	Average internal reference frequency — untrimmed		f_{int_ut}	31.25	—	39.0625	kHz
3	T	Internal reference startup time		t_{irefst}	—	60	100	µs
4	C	DCO output frequency range — untrimmed [2]	Low range (DRS=00)	f_{dco_ut}	16	—	20	MHz
	C		Mid range (DRS=01)		32	—	40	
	C		High range (DRS=10)		48	—	60	
5	P	DCO output frequency[2] reference =32768Hz and DMX32 = 1	Low range (DRS=00)	f_{dco_DMX32}	—	16.82	—	MHz
	P		Mid range (DRS=01)		—	33.69	—	
	P		High range (DRS=10)		—	50.48	—	
6	D	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)		$\Delta f_{dco\_res\_t}$	—	±0.1	±0.2	$\%f_{dco}$
7	D	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)		$\Delta f_{dco\_res\_t}$	—	±0.2	±0.4	$\%f_{dco}$
8	D	Total deviation of trimmed DCO output frequency over voltage and temperature		Δf_{dco_t}	—	0.5 –1.0	±2	$\%f_{dco}$
9	D	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0–70 °C		Δf_{dco_t}	—	±0.5	±1	$\%f_{dco}$
10	D	FLL acquisition time[3]		$t_{fll\_acquire}$	—	—	1	ms
11	D	PLL acquisition time[4]		$t_{pll\_acquire}$	—	—	1	ms
12	D	Long term jitter of DCO output clock (averaged over 2ms interval) [5]		C_{Jitter}	—	0.02	0.2	$\%f_{dco}$
13	D	VCO operating frequency		f_{vco}	7.0	—	55.0	MHz
16	D	Jitter of PLL output clock measured over 625 ns[6]		$f_{pll\_jitter\_625ns}$	—	0.566[6]	—	$\%f_{pll}$
17	D	Lock entry frequency tolerance [7]		D_{lock}	±1.49	—	±2.98	%

Table 16. MCG Frequency Specifications (continued)(Temperature Range = –40 to 105 °C Ambient)

Num	C	Rating	Symbol	Min	Typical[1]	Max	Unit
18	D	Lock exit frequency tolerance [8]	D_{unl}	±4.47	—	±5.97	%
19	D	Lock time — FLL	t_{fll_lock}	—	—	$t_{fll\_acquire}$+ 1075(1/f_{int_t})	s
20	D	Lock time — PLL	t_{pll_lock}	—	—	$t_{pll\_acquire}$+ 1075(1/f_{pll_ref})	s
21	D	Loss of external clock minimum frequency — RANGE = 0	f_{loc_low}	(3/5) × f_{int}	—	—	kHz

1 Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.

2 The resulting bus clock frequency must not exceed the maximum specified bus clock frequency of the device.

3 This specification applies when the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

4 This specification applies when the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

5 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

6 625 ns represents 5 time quanta for CAN applications, under worst case conditions of 8 MHz CAN bus clock, 1 Mbps CAN bus speed, and 8 time quanta per bit for bit time settings. 5 time quanta is the minimum time between a synchronization edge and the sample point of a bit using 8 time quanta per bit.

7 Below D_{lock} minimum, the MCG enters lock. Above D_{lock} maximum, the MCG will not enter lock. But if the MCG is already in lock, then the MCG may stay in lock.

8 Below D_{unl} minimum, the MCG will not exit lock if already in lock. Above D_{unl} maximum, the MCG is guaranteed to exit lock.

2.11 AC Characteristics

This section describes ac timing characteristics for each peripheral system.

2.11.2 Timer (TPM/FTM) Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 18. TPM/FTM Input Timing

NUM	C	Function	Symbol	Min	Max	Unit
1	—	External clock frequency	f_{TPMext}	DC	$f_{Bus}/4$	MHz
2	—	External clock period	t_{TPMext}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

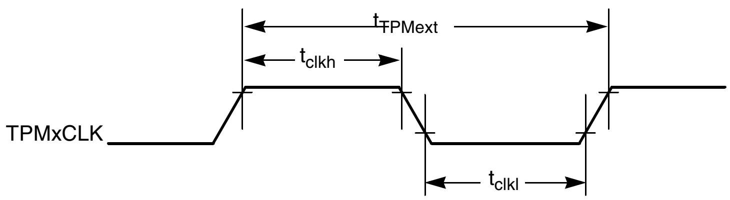


Figure 13. Timer External Clock

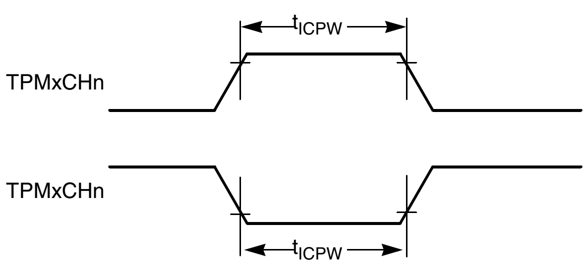


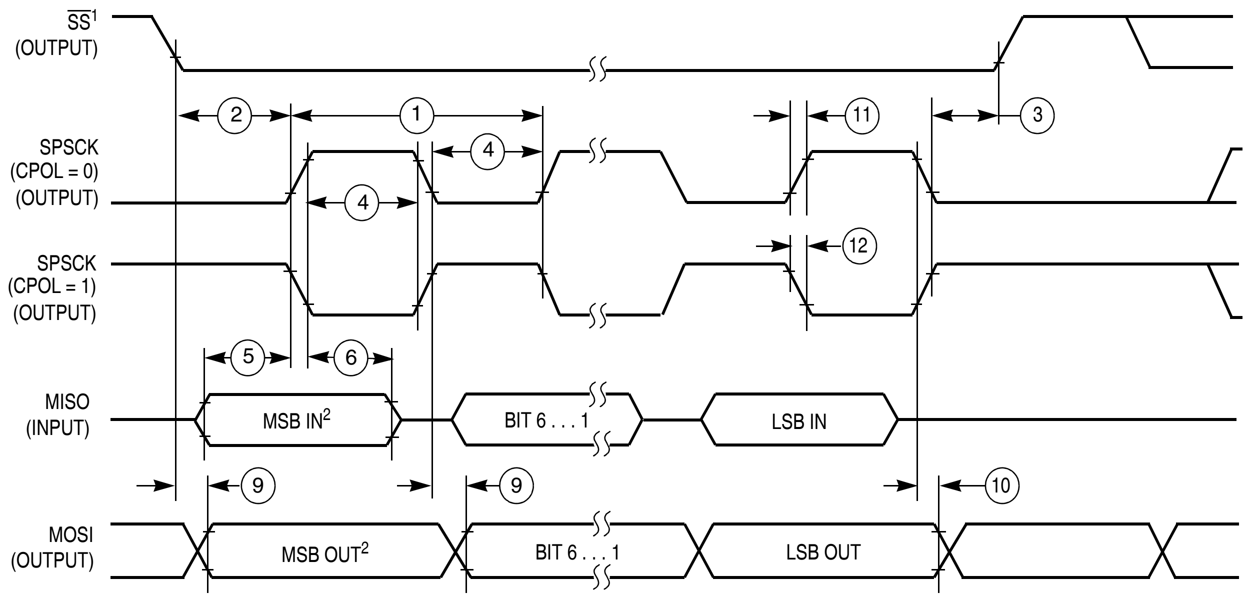
Figure 14. Timer Input Capture Pulse

2.11.3 MSCAN

Table 19. MSCAN Wake-Up Pulse Characteristics

Num	C	Parameter	Symbol	Min	Typical[1]	Max	Unit
1	D	MSCAN wake-up dominant pulse filtered	t_{WUP}	—	—	2	µs
2	D	MSCAN wake-up dominant pulse pass	t_{WUP}	5	—	5	µs

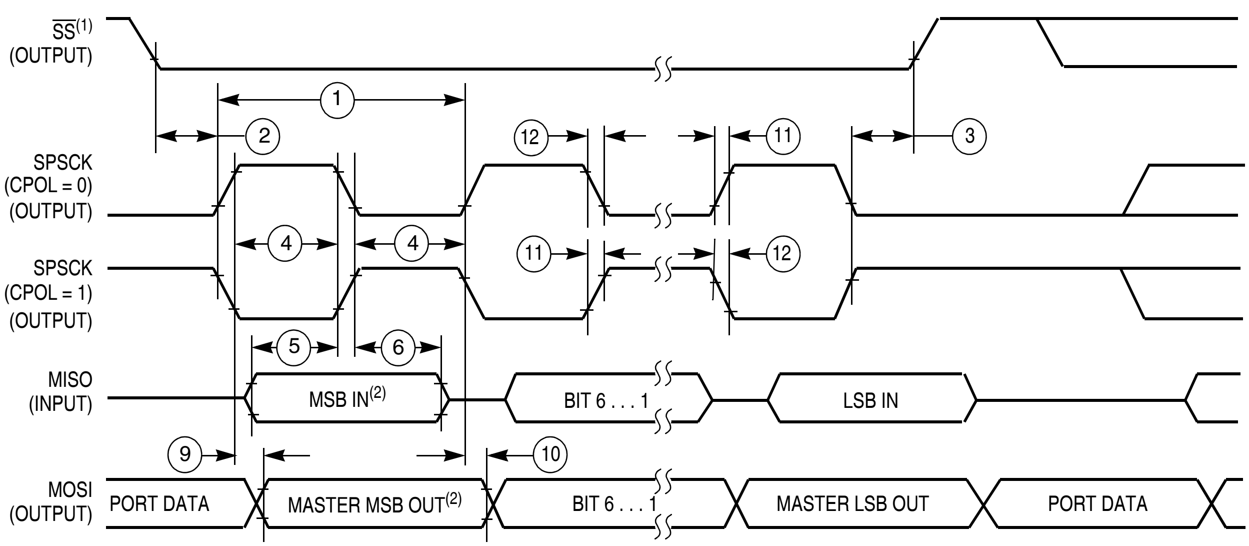
[1] Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.



NOTES:

1. $\overline{SS}$ output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

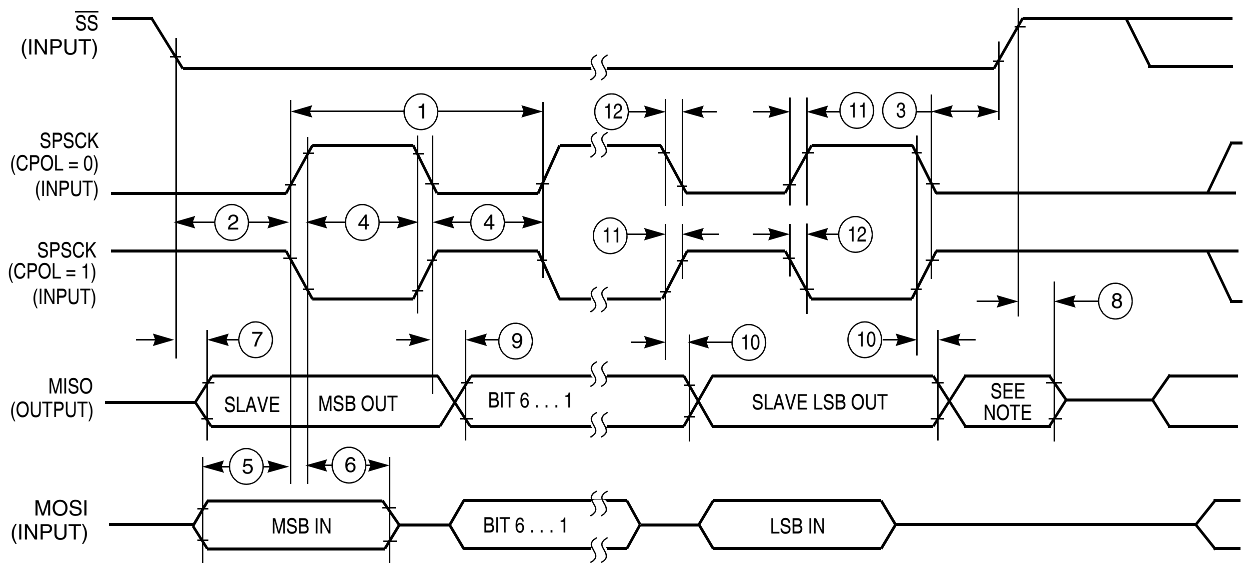
Figure 15. SPI Master Timing (CPHA = 0)



NOTES:

1. $\overline{SS}$ output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

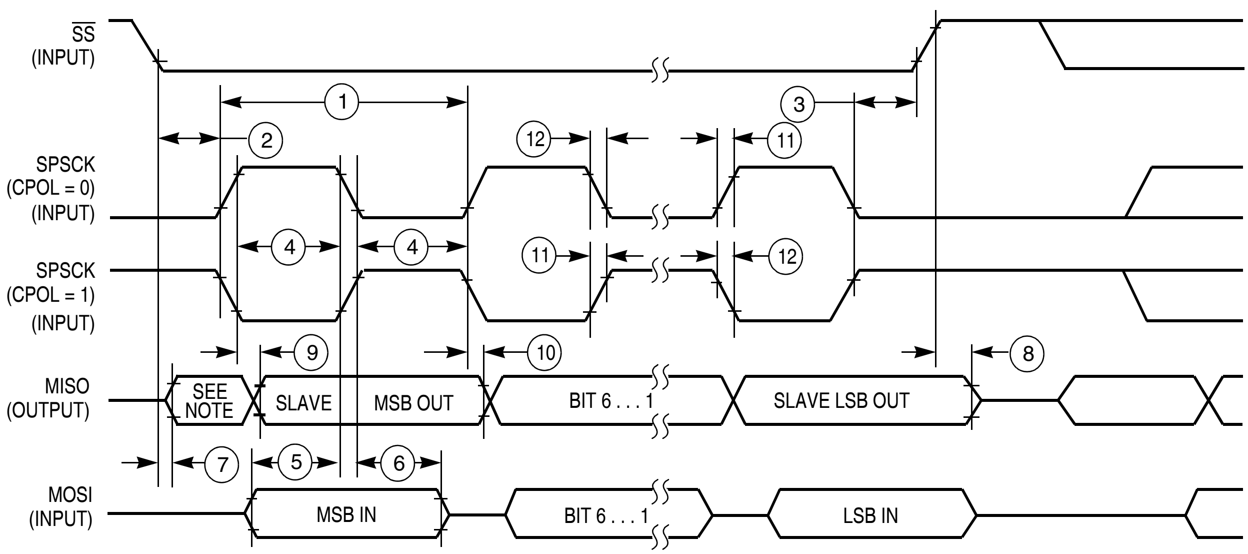
Figure 16. SPI Master Timing (CPHA =1)



NOTE:

1. Not defined but normally MSB of character just received

Figure 17. SPI Slave Timing (CPHA = 0)



NOTE:

1. Not defined but normally LSB of character just received

Figure 18. SPI Slave Timing (CPHA = 1)

2.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the Flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see Chapter 4, “Memory.”

Table 21. Flash Characteristics

Num	C	Characteristic	Symbol	Min	Typical[1]	Max	Unit
1	—	Supply voltage for program/erase	$V_{prog/erase}$	2.7	—	5.5	V
2	—	Supply voltage for read operation	V_{Read}	2.7	—	5.5	V
3	—	Internal FCLK frequency[2]	f_{FCLK}	150	—	200	kHz
4	—	Internal FCLK period (1/FCLK)	t_{Fcyc}	5	—	6.67	μs
5	—	Byte program time (random location)[2]	t_{prog}	9			t_{Fcyc}
6	—	Byte program time (burst mode)[2]	t_{Burst}	4			t_{Fcyc}
7	—	Page erase time[3]	t_{Page}	4000			t_{Fcyc}
8	—	Mass erase time[2]	t_{Mass}	20,000			t_{Fcyc}
9	C	Program/erase endurance[4] T_L to T_H = –40 °C to 105 °C T = 25 °C	—	 10,000 —	 — 100,000	 — —	cycles
10	C	Data retention[5]	t_{D_ret}	15	100	—	years

1 Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.

2 The frequency of this clock is controlled by a software setting.

3 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

4 **Typical endurance for flash** was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale Semiconductor defines typical endurance, please refer to Engineering Bulletin EB619/D, *Typical Endurance for Nonvolatile Memory*.

5 **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale Semiconductor defines typical data retention, please refer to Engineering Bulletin EB618/D, *Typical Data Retention for Nonvolatile Memory.*

2.14 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

2.14.1 Radiated Emissions

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM Cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (North and East). For more detailed information concerning the evaluation results, conditions and setup, please refer to the EMC Evaluation Report for this device.

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