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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	CANbus, I ² C, SCI, SPI
Peripherals	LVD, PWM, WDT
Number of I/O	54
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 20x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/pcf51ac128acpue

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1.3 Features

Table 2 describes the functional units of the MCF51AC256 series.

Table 2. MCF51AC256 Series Functional Units

Functional Unit	Function
CF1 Core (V1 ColdFire core)	Executes programs and interrupt handlers
BDM (background debug module)	Provides single pin debugging interface (part of the V1 ColdFire core)
DBG (debug)	Provides debugging and emulation capabilities (part of the V1 ColdFire core)
VBUS (debug visibility bus)	Allows for real-time program traces (part of the V1 ColdFire core)
SIM (system integration module)	Controls resets and chip level interfaces between modules
Flash (flash memory)	Provides storage for program code, constants and variables
RAM (random-access memory)	Provides storage for program variables
RGPIO (rapid general-purpose input/output)	Allows for I/O port access at CPU clock speeds
VREG (voltage regulator)	Controls power management across the device
COP (computer operating properly)	Monitors a countdown timer and generates a reset if the timer is not regularly reset by the software
LVD (low-voltage detect)	Monitors internal and external supply voltage levels, and generates a reset or interrupt when the voltages are too low
CF1_INTIC (interrupt controller)	Controls and prioritizes all device interrupts
ADC (analog-to-digital converter)	Measures analog voltages at up to 12 bits of resolution
FTM1, FTM2 (flexible timer/pulse-width modulators)	Provides a variety of timing-based features
TPM3 (timer/pulse-width modulator)	Provides a variety of timing-based features
CRC (cyclic redundancy check)	Accelerates computation of CRC values for ranges of memory
ACMP1, ACMP2 (analog comparators)	Compares two analog inputs
IIC (inter-integrated circuit)	Supports standard IIC communications protocol
KBI (keyboard interrupt)	Provides pin interrupt capabilities
MCG (multipurpose clock generator)	Provides clocking options for the device, including a phase-locked loop (PLL) and frequency-locked loop (FLL) for multiplying slower reference clock sources
OSC (crystal oscillator)	Allows a crystal or ceramic resonator to be used as the system clock source or reference clock for the PLL or FLL
LPO (low-power oscillator)	Provides a second clock source for COP and RTI.
CAN (controller area network)	Supports standard CAN communications protocol
SCI1, SCI2 (serial communications interfaces)	Serial communications UARTs capable of supporting RS-232 and LIN protocols
SPI1 (8-bit serial peripheral interfaces)	Provides 8-bit 4-pin synchronous serial interface
SPI2 (16-bit serial peripheral interfaces)	Provides 16-bit 4-pin synchronous serial interface with FIFO

1.3.1 Feature List

- 32-bit Version 1 ColdFire® central processor unit (CPU)
 - Up to 50.33 MHz at 2.7 V – 5.5 V
 - Provide 0.94 Dhrystone 2.1 DMIPS per MHz performance when running from internal RAM (0.76 DMIPS per MHz when running from flash)
 - Implements instruction set revision C (ISA_C)
- On-chip memory
 - Up to 256 KB flash memory read/program/erase over full operating voltage and temperature
 - Up to 32 KB static random access memory (SRAM)
 - Security circuitry to prevent unauthorized access to SRAM and flash contents
- Power-Saving Modes
 - Three low-power stop plus wait modes
 - Peripheral clock enable register can disable clocks to unused modules, reducing currents; allows clocks to remain enabled to specific peripherals in stop3 mode
- System protection features
 - Watchdog computer operating properly (COP) reset with options to run from independent LPO clock or bus clock
 - Low-voltage detection with reset or interrupt
 - Illegal opcode and illegal address detection with programmable reset or exception response
 - Flash block protection
- Debug support
 - Single-wire background debug interface
 - Real-time debug support, with 6 hardware breakpoints (4 PC, 1 address pair and 1 data) that can be configured into a 1- or 2-level trigger
 - On-chip trace buffer provides programmable start/stop recording conditions plus support for continuous or PC-profiling modes
 - Support for real-time program (and optional partial data) trace using the debug visibility bus
- V1 ColdFire interrupt controller (CF1_INTC)
 - Support of 40 peripheral I/O interrupt requests plus seven software (one per level) interrupt requests
 - Fixed association between interrupt request source and level plus priority, up to two requests can be remapped to the highest maskable level + priority
 - Unique vector number for each interrupt source
 - Support for service routine interrupt acknowledge (software IACK) read cycles for improved system performance
- Multipurpose clock generator (MCG)
 - Oscillator (XOSC); loop-control Pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
 - LPO clock as an optional independent clock source for COP and RTI
 - FLL/PLL controlled by internal or external reference

MCF51AC256 Family Configurations

- Double-buffered transmit and receive
- Serial clock phase and polarity options
- Slave select output
- Selectable MSB-first or LSB-first shifting
- 16-bit and FIFO operations in SPI2
- Input/Output
 - 69 GPIOs
 - 8 keyboard interrupt pins with selectable polarity
 - Hysteresis and configurable pull-up device on all input pins; Configurable slew rate and drive strength on all output pins
 - 16-bits Rapid GPIO pins connected to the processor's local 32-bit platform bus with set, clear, and faster toggle functionality

1.4 Part Numbers

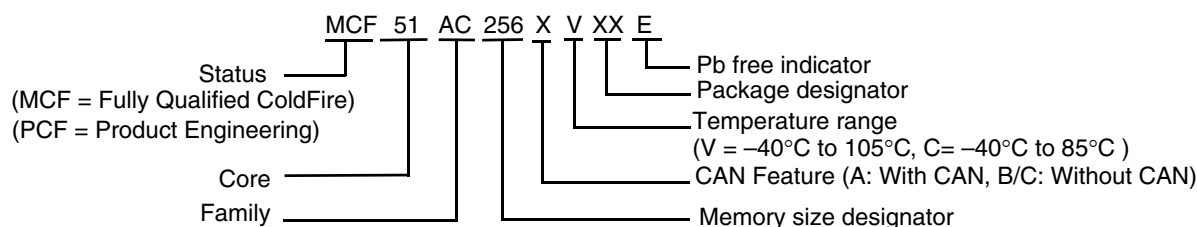


Table 3. Orderable Part Number Summary

Freescall Part Number	Description	Flash / SRAM (Kbytes)	Package	Temperature
MCF51AC256AVFUE	MCF51AC256 ColdFire Microcontroller with CAN	256 / 32	64 QFP	-40°C to 105°C
MCF51AC256BVFUE	MCF51AC256 ColdFire Microcontroller without CAN	256 / 32	64 QFP	-40°C to 105°C
MCF51AC256AVLKE	MCF51AC256 ColdFire Microcontroller with CAN	256 / 32	80 LQFP	-40°C to 105°C
MCF51AC256BVLKE	MCF51AC256 ColdFire Microcontroller without CAN	256 / 32	80 LQFP	-40°C to 105°C
MCF51AC256AVPUE	MCF51AC256 ColdFire Microcontroller with CAN	256 / 32	64 LQFP	-40°C to 105°C
MCF51AC256BVPUE	MCF51AC256 ColdFire Microcontroller without CAN	256 / 32	64 LQFP	-40°C to 105°C
MCF51AC128AVFUE	MCF51AC128 ColdFire Microcontroller with CAN	128 / 32	64 QFP	-40°C to 105°C
MCF51AC128CVFUE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	64 QFP	-40°C to 105°C
MCF51AC128AVLKE	MCF51AC128 ColdFire Microcontroller with CAN	128 / 32	80 LQFP	-40°C to 105°C
MCF51AC128CVLKE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	80 LQFP	-40°C to 105°C
MCF51AC128AVPUE	MCF51AC128 ColdFire Microcontroller with CAN	128 / 32	64 LQFP	-40°C to 105°C
MCF51AC128CVPUE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	64 LQFP	-40°C to 105°C
MCF51AC256ACFUE	MCF51AC256 ColdFire Microcontroller with CAN	256 / 32	64 QFP	-40°C to 85°C
MCF51AC256BCFUE	MCF51AC256 ColdFire Microcontroller without CAN	256 / 32	64 QFP	-40°C to 85°C
MCF51AC256ACLKE	MCF51AC256 ColdFire Microcontroller with CAN	256 / 32	80 LQFP	-40°C to 85°C
MCF51AC256BCLKE	MCF51AC256 ColdFire Microcontroller without CAN	256 / 32	80 LQFP	-40°C to 85°C

Table 3. Orderable Part Number Summary

MCF51AC256ACPUE	MCF51AC256 ColdFire Microcontroller with CAN	256 / 32	64 LQFP	–40°C to 85°C
MCF51AC256BCPUE	MCF51AC256 ColdFire Microcontroller without CAN	256 / 32	64 LQFP	–40°C to 85°C
MCF51AC256BCFGE	MCF51AC256 ColdFire Microcontroller without CAN	256/32	44 LQFP	–40°C to 85°C
MCF51AC128ACFUE	MCF51AC128 ColdFire Microcontroller with CAN	128 / 32	64 QFP	–40°C to 85°C
MCF51AC128CCFUE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	64 QFP	–40°C to 85°C
MCF51AC128ACLKE	MCF51AC128 ColdFire Microcontroller with CAN	128 / 32	80 LQFP	–40°C to 85°C
MCF51AC128CCLKE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	80 LQFP	–40°C to 85°C
MCF51AC128ACPUE	MCF51AC128 ColdFire Microcontroller with CAN	128 / 32	64 LQFP	–40°C to 85°C
MCF51AC128CCPUE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	64 LQFP	–40°C to 85°C
MCF51AC128CCFGE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	44 LQFP	–40°C to 85°C

1.5 Pinouts and Packaging

Figure 2 shows the pinout of the 80-pin LQFP.

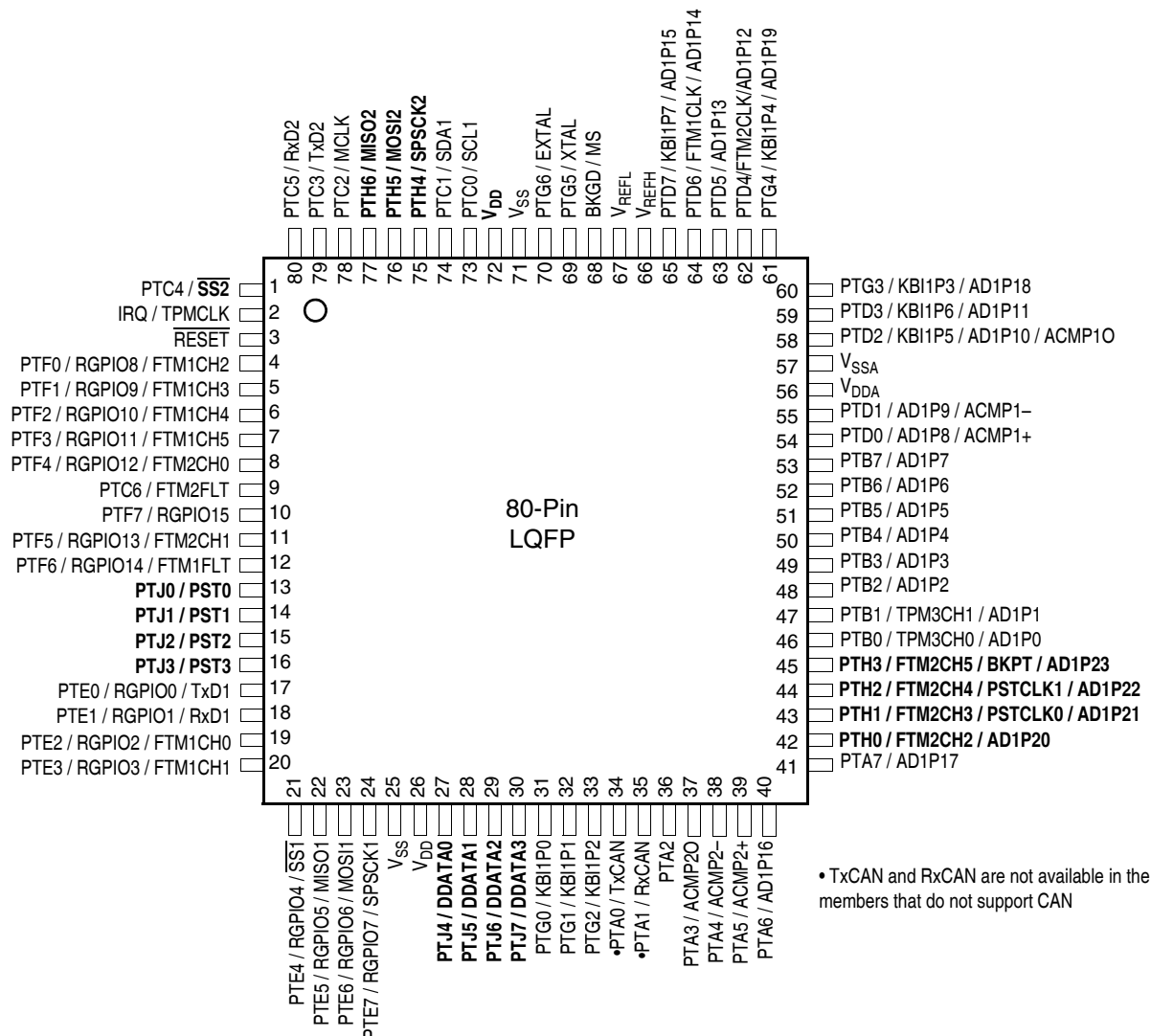


Figure 2. MCF51AC256 Series ColdFire Microcontroller 80-Pin LQFP

Figure 3 shows the pinout of the 64-pin LQFP and QFP.

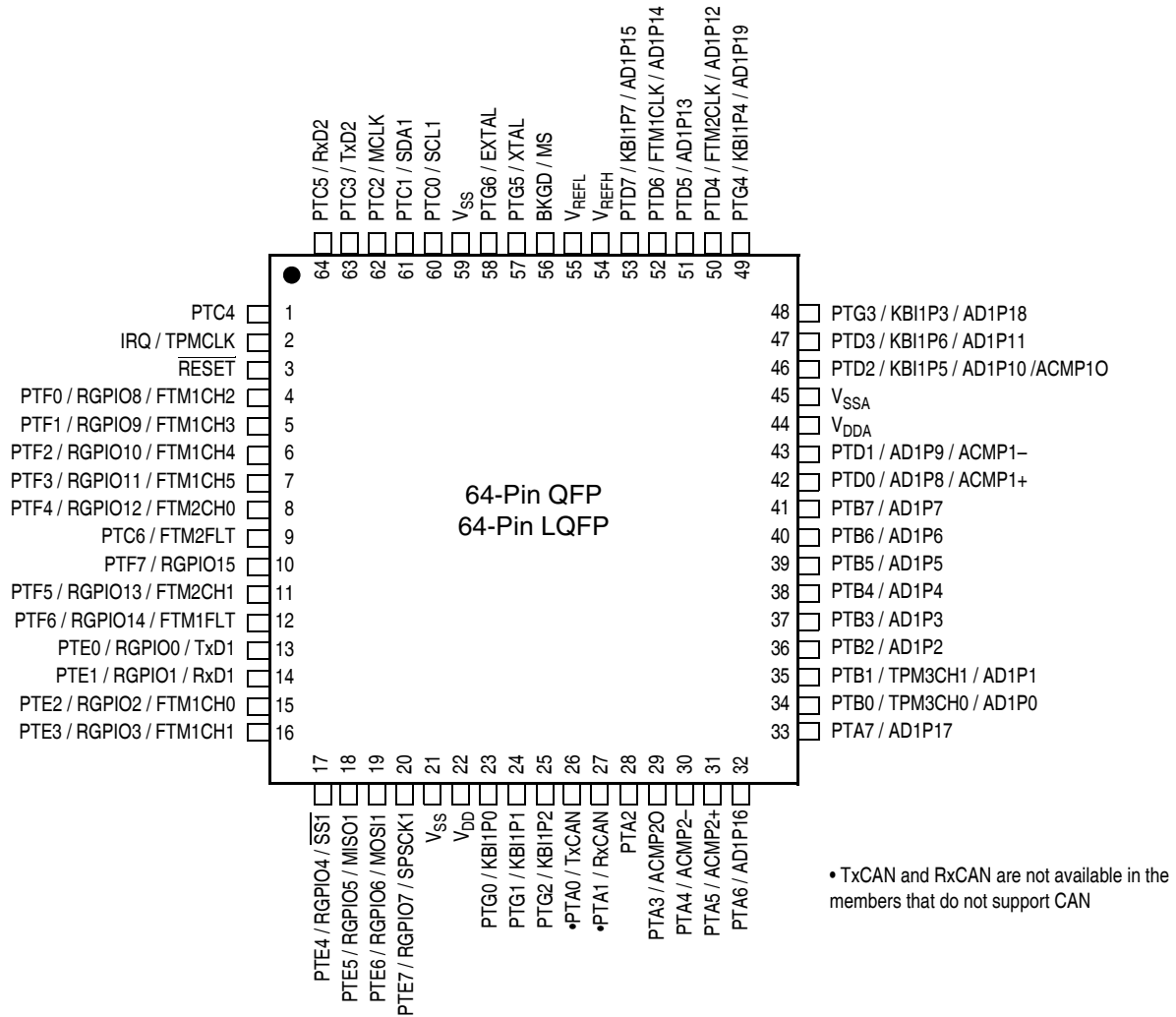


Figure 3. MCF51AC256 Series ColdFire Microcontroller 64-Pin QFP/LQFP

Figure 4 shows the pinout of the 44-pin LQFP.

Table 4. Pin Availability by Package Pin-Count (continued)

Pin Number			Lowest <-- Priority --> Highest			
80	64	44	Port Pin	Alt 1	Alt 2	Alt 3
49	37	26	PTB3	AD1P3		
50	38	—	PTB4	AD1P4		
51	39	—	PTB5	AD1P5		
52	40	—	PTB6	AD1P6		
53	41	—	PTB7	AD1P7		
54	42	27	PTD0	AD1P8	ACMP1+	
55	43	28	PTD1	AD1P9	ACMP1–	
56	44	29	V _{DDA}			
57	45	30	V _{SSA}			
58	46	31	PTD2	KBI1P5	AD1P10	ACMP1O
59	47	32	PTD3	KBI1P6	AD1P11	
60	48	33	PTG3	KBI1P3	AD1P18	
61	49	—	PTG4	KBI1P4	AD1P19	
62	50	—	PTD4	FTM2CLK	AD1P12	
63	51	—	PTD5	AD1P13		
64	52	—	PTD6	FTM1CLK	AD1P14	
65	53	—	PTD7	KBI1P7	AD1P15	
66	54	34	V _{REFH}			
67	55	35	V _{REFL}			
68	56	36	BKGD	MS		
69	57	37	PTG5	XTAL		
70	58	38	PTG6	EXTAL		
71	59	39	V _{SS}			
72	—	—	V _{DD}			
73	60	40	PTC0	SCL1		
74	61	41	PTC1	SDA1		
75	—	—	PTH4	SPCK2		
76	—	—	PTH5	MOSI2		
77	—	—	PTH6	MISO2		
78	62	42	PTC2	MCLK		
79	63	43	PTC3	TxD2		
80	64	44	PTC5	RxD2		

¹ TPMCLK, FTM1CLK, and FTM2CLK options are configured via software; out of reset, FTM1CLK, FTM2CLK, and TPMCLK are available to FTM1, FTM2, and TPM3 respectively.

² TxCAN is available in the member that supports CAN.

³ RxCAN is available in the member that supports CAN.

2 Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the MCF51AC256 microcontroller, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. These specifications will, however, be met for production silicon. Finalized specifications will be published after complete characterization and device qualifications have been completed.

NOTE

The parameters specified in this data sheet supersede any values found in the module specifications.

2.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 5. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

2.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in [Table 6](#) may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}).

Table 6. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	−0.3 to 5.8	V
Input voltage	V_{In}	−0.3 to $V_{DD} + 0.3$	V
Instantaneous maximum current Single pin limit (applies to all port pins) ^{1, 2, 3}	I_D	±25	mA
Maximum current into V_{DD}	I_{DD}	120	mA
Storage temperature	T_{stg}	−55 to 150	°C

¹ Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

² All functional non-supply pins are internally clamped to V_{SS} and V_{DD} .

³ Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD} , the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low which would reduce overall power consumption.

2.3 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and it is user-determined rather than being controlled by the MCU design. In order to take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 7. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	−40 to 105	°C
Maximum junction temperature	T_J	150	°C
Thermal resistance ^{1,2,3,4}			
80-pin LQFP			
1s		51	
2s2p		38	
64-pin LQFP			
1s		59	
2s2p	θ_{JA}	41	°C/W
64-pin QFP			
1s		50	
2s2p		36	
44-pin LQFP			
1s		67	
2s2p		45	

- ¹ Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance
- ² Junction to Ambient Natural Convection
- ³ 1s — Single layer board, one signal layer
- ⁴ 2s2p — Four layer board, 2 signal and 2 power layers

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \text{Eqn. 1}$$

where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power

$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} \ll P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273^\circ\text{C}) \quad \text{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273^\circ\text{C}) + \theta_{JA} \times (P_D)^2 \quad \text{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A . Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A .

2.4 Electrostatic Discharge (ESD) Protection Characteristics

Although damage from static discharge is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with CDF-AEC-Q00 Stress Test Qualification for Automotive Grade Integrated Circuits. (<http://www.aecouncil.com/>) This device was qualified to AEC-Q100 Rev E.

A device is considered to have failed if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete dc parametric and functional testing is performed per the

Electrical Characteristics

applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 8. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human body	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulse per pin	—	3	
Charge device model	Series resistance	R1	0	Ω
	Storage capacitance	C	0	pF
	Number of pulse per pin	—	3	—
Latch-up	Minimum input voltage limit	—	-2.5	V
	Maximum input voltage limit	—	7.5	V

Table 9. ESD and Latch-Up Protection Characteristics

Num	Rating	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	± 2000	—	V
2	Charge device model (CDM)	V_{CDM}	± 500	—	V
3	Latch-up current at $T_A = 85^\circ\text{C}$	I_{LAT}	± 100	—	mA

2.5 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

Table 10. DC Characteristics

Num	C	Parameter	Symbol	Min	Typical ¹	Max	Unit
1	—	Operating voltage		2.7	—	5.5	V
2	P	Output high voltage — Low drive (PTxDSn = 0) 5 V, $I_{Load} = -4$ mA 3 V, $I_{Load} = -2$ mA 5 V, $I_{Load} = -2$ mA 3 V, $I_{Load} = -1$ mA	V_{OH}	$V_{DD} - 1.5$ $V_{DD} - 1.5$ $V_{DD} - 0.8$ $V_{DD} - 0.8$	— — — —	— — — —	V
		Output high voltage — High drive (PTxDSn = 1) 5 V, $I_{Load} = -15$ mA 3 V, $I_{Load} = -8$ mA 5 V, $I_{Load} = -8$ mA 3 V, $I_{Load} = -4$ mA		$V_{DD} - 1.5$ $V_{DD} - 1.5$ $V_{DD} - 0.8$ $V_{DD} - 0.8$	— — — —	— — — —	

Table 10. DC Characteristics (continued)

Num	C	Parameter	Symbol	Min	Typical ¹	Max	Unit
22	D	DC injection current ^{5 6 7 8} (single pin limit) $V_{IN} > V_{DD}$ $V_{IN} < V_{SS}$	I_{IC}	0 0	—	2 -0.2	mA
		DC injection current (Total MCU limit, includes sum of all stressed pins) $V_{IN} > V_{DD}$ $V_{IN} < V_{SS}$		0 0	—	25 -5	mA

¹ Typical values are based on characterization data at 25°C unless otherwise stated.

² Measured with $V_{IN} = V_{DD}$ or V_{SS} .

³ Measured with $V_{IN} = V_{SS}$.

⁴ Measured with $V_{IN} = V_{DD}$.

⁵ Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{IN} > V_{DD}$) is greater than I_{DD} , the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

⁶ All functional non-supply pins are internally clamped to V_{SS} and V_{DD} .

⁷ Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

⁸ The **RESET** pin does not have a clamp diode to V_{DD} . Do not drive this pin above V_{DD} .

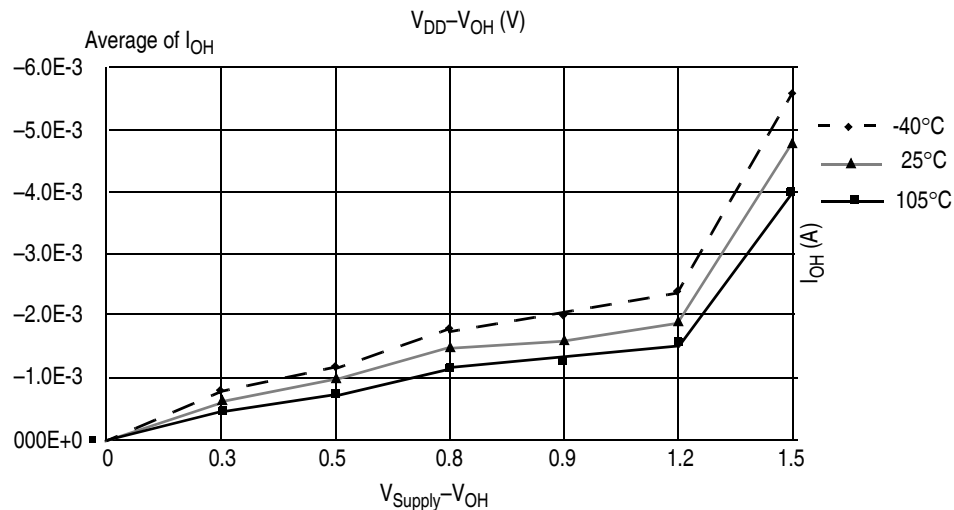


Figure 5. Typical I_{OH} vs. $V_{DD} - V_{OH}$ at $V_{DD} = 3$ V (Low Drive, $PTxDSn = 0$)

2.6 Supply Current Characteristics

Table 11. Supply Current Characteristics

Num	C	Parameter		Symbol	V _{DD} (V)	Typical ¹	Max ²	Unit
1	T	Run supply current measured at FEI mode, all modules off, system clock at:	2 MHz	R _I _{DD}	5	2.27	—	mA
					3.3	2.24	—	
			4 MHz		5	3.67	—	
					3.3	3.64	—	
			8 MHz		5	6.55	—	
					3.3	6.54	—	
			16 MHz		5	11.90	—	
					3.3	11.85	—	
2	T	Run supply current measured at FEI mode, all modules on, system clock at:	2 MHz		5	3.28	—	
					3.3	3.26	—	
			4 MHz		5	4.33	—	
					3.3	4.32	—	
			8 MHz		5	8.17	—	
					3.3	8.05	—	
			16 MHz		5	14.8	—	
					3.3	14.74	—	
3	T	Run supply current measured at FBE mode, all modules off (RANGE = 1, HGO = 0), system clock at:	2 MHz		5	3.28	—	
					3.3	3.26	—	
			4 MHz		5	4.69	—	
					3.3	4.67	—	
			8 MHz		5	7.48	—	
					3.3	7.46	—	
			16 MHz		5	13.10	—	
					3.3	13.07	—	
4	T	Run supply current measured at FBE mode, all modules on (RANGE = 1, HGO = 0), system clock at:	2 MHz		5	3.64	—	
					3.3	3.63	—	
			4 MHz		5	5.38	—	
					3.3	5.35	—	
			8 MHz		5	8.65	—	
					3.3	8.64	—	
			16 MHz		5	15.55	—	
					3.3	15.40	—	

Table 11. Supply Current Characteristics (continued)

Num	C	Parameter	Symbol	V _{DD} (V)	Typical ¹	Max ²	Unit
5	C	Wait mode supply ³ current measured at (CPU clock = 2 MHz, f _{BUS} = 1 MHz)	W _I DD	5	1.3	2	mA
				3	1.29	2	
6	C	Wait mode supply ³ current measured at (CPU clock = 16 MHz, f _{BUS} = 8 MHz)		5	5.11	8	mA
				3	5.1	8	
7	C	Wait mode supply ³ current measured at (CPU clock = 50 MHz, f _{BUS} = 25 MHz)		5	15.24	25	mA
				3	15.2	25	
8	C	Stop2 mode supply current -40 °C 25 °C 120 °C	S2I _{DD}	5	1.40	2.5 2.5 200	μA
				3	1.16	2.5 2.5 200	μA
				5	1.60	2.5 2.5 220	μA
				3	1.35	2.5 2.5 220	μA
9	C	Stop3 mode supply current -40 °C 25 °C 120 °C	S3I _{DD}	5	1.60	2.5 2.5 220	μA
				3	1.35	2.5 2.5 220	μA
10	C	RTI adder to stop2 or stop3 ³ , 25 °C	S23I _{DDRTI}	5	300		nA
				3	300		nA
11	C	Adder to stop3 for oscillator enabled ⁴ (ERCLKEN = 1 and EREFSTEN = 1)	S3I _{DDOSC}	5, 3	5		μA

¹ Typicals are measured at 25 °C.

² Values given here are preliminary estimates prior to completing characterization.

³ Most customers are expected to find that auto-wakeup from stop2 or stop3 can be used instead of the higher current wait mode.

⁴ Values given under the following conditions: low range operation (RANGE = 0), low power mode (HGO = 0).

Table 16. MCG Frequency Specifications (continued)(Temperature Range = –40 to 105 °C Ambient)

Num	C	Rating	Symbol	Min	Typical ¹	Max	Unit
18	D	Lock exit frequency tolerance ⁸	D _{unl}	±4.47	—	±5.97	%
19	D	Lock time — FLL	t _{fil_lock}	—	—	t _{fil_acquire} + 1075(1/f _{int_t})	s
20	D	Lock time — PLL	t _{pll_lock}	—	—	t _{pll_acquire} + 1075(1/f _{pll_ref})	s
21	D	Loss of external clock minimum frequency — RANGE = 0	f _{loc_low}	(3/5) × f _{int}	—	—	kHz

¹ Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.

² The resulting bus clock frequency must not exceed the maximum specified bus clock frequency of the device.

³ This specification applies when the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

⁴ This specification applies when the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

⁵ Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

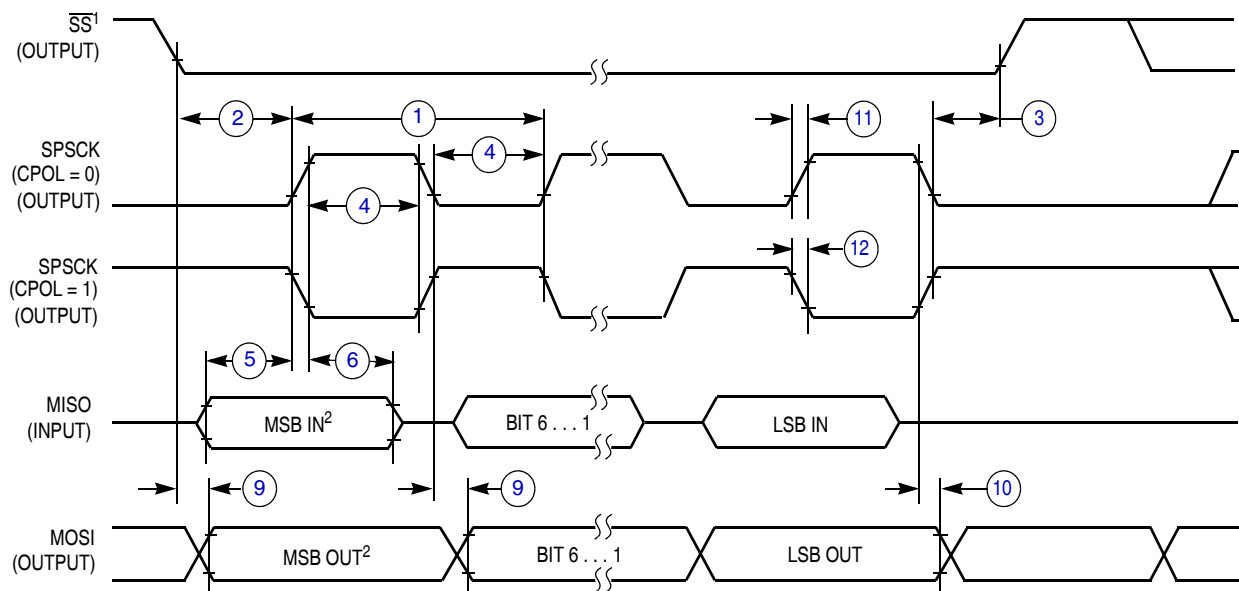
⁶ 625 ns represents 5 time quanta for CAN applications, under worst case conditions of 8 MHz CAN bus clock, 1 Mbps CAN bus speed, and 8 time quanta per bit for bit time settings. 5 time quanta is the minimum time between a synchronization edge and the sample point of a bit using 8 time quanta per bit.

⁷ Below D_{lock} minimum, the MCG enters lock. Above D_{lock} maximum, the MCG will not enter lock. But if the MCG is already in lock, then the MCG may stay in lock.

⁸ Below D_{unl} minimum, the MCG will not exit lock if already in lock. Above D_{unl} maximum, the MCG is guaranteed to exit lock.

2.11 AC Characteristics

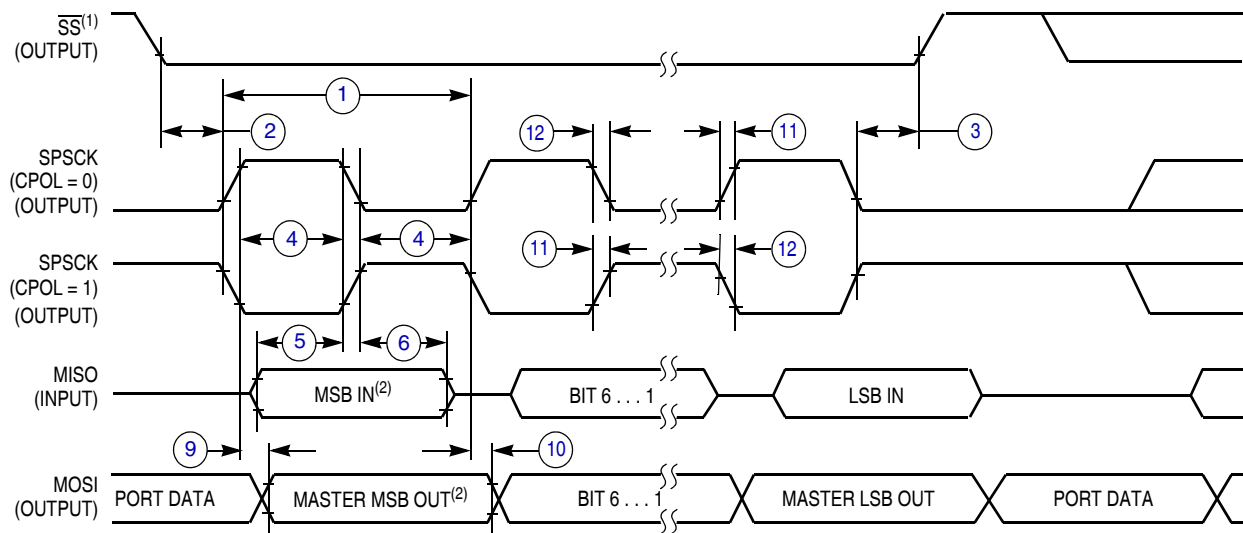
This section describes ac timing characteristics for each peripheral system.



NOTES:

1. \overline{SS} output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

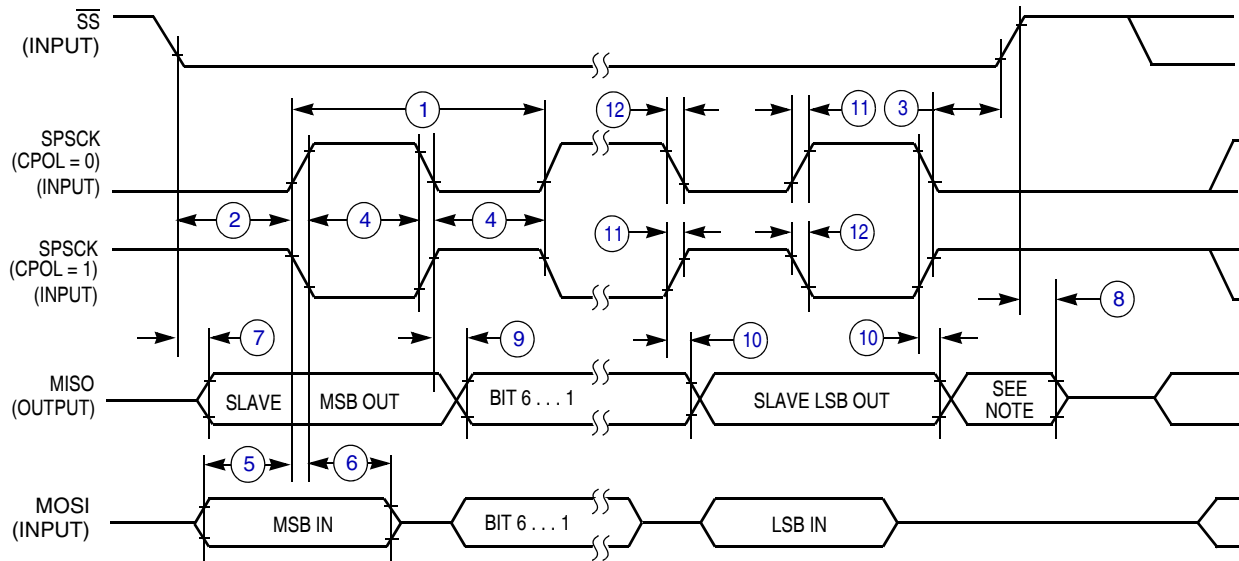
Figure 15. SPI Master Timing (CPHA = 0)



NOTES:

1. \overline{SS} output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

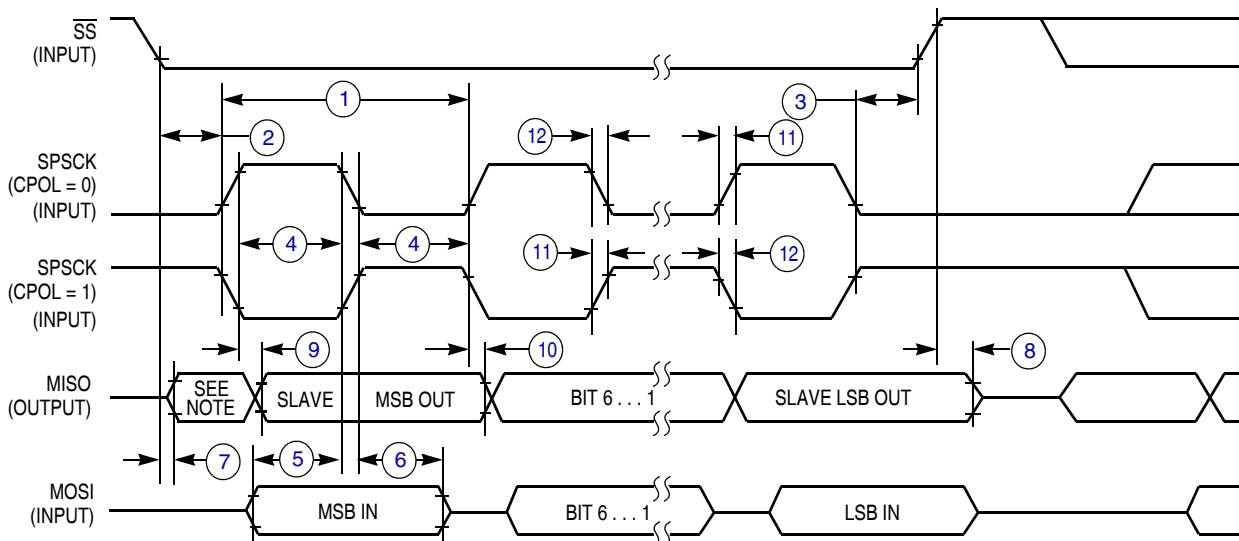
Figure 16. SPI Master Timing (CPHA = 1)



NOTE:

1. Not defined but normally MSB of character just received

Figure 17. SPI Slave Timing (CPHA = 0)



NOTE:

1. Not defined but normally LSB of character just received

Figure 18. SPI Slave Timing (CPHA = 1)

2.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the Flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see [Chapter 4, “Memory.”](#)

3 Mechanical Outline Drawings

Table 22 provides the available package types and their document numbers. The latest package outline/mechanical drawings are available on the MCF51AC256 Series Product Summary pages at <http://www.freescale.com>.

To view the latest drawing, either:

- Click on the appropriate link in Table 22, or
- Open a browser to the Freescale website (<http://www.freescale.com>), and enter the appropriate document number (from Table 22) in the “Enter Keyword” search box at the top of the page.

Table 22. Package Information

Pin Count	Type	Document No.
80	LQFP	98ARL10530D
64	LQFP	98ASS23234W
64	QFP	98ASB42844B
44	LQFP	98ASS23225W

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