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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I ² C, SCI, SPI
Peripherals	LVD, PWM, WDT
Number of I/O	69
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/pcf51ac128cclke

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1 MCF51AC256 Family Configurations

1.1 Device Comparison

The MCF51AC256 series is summarized in [Table 1](#).

Table 1. MCF51AC256 Series Device Comparison

Feature	MCF51AC256A		MCF51AC256B			MCF51AC128A		MCF51AC128C		
	80-pin	64-pin	80-pin	64-pin	44-pin	80-pin	64-pin	80-pin	64-pin	44-pin
Flash memory size (Kbytes)	256					128				
RAM size (Kbytes)	32					32 or 16 ¹				
V1 ColdFire core with BDM (background debug module)	Yes									
ACMP1 (analog comparator)	Yes									
ACMP2 (analog comparator)	Yes		Yes		No	Yes				No
ADC (analog-to-digital converter) channels (12-bit)	24	20	24	20	9	24	20	24	20	9
CAN (controller area network)	Yes		No			Yes		No		
COP (computer operating properly)	Yes									
CRC (cyclic redundancy check)	Yes									
RTI	Yes									
DBG (debug)	Yes									
IIC1 (inter-integrated circuit)	Yes									
IRQ (interrupt request input)	Yes									
INTC (interrupt controller)	Yes									
KBI (keyboard interrupts)	Yes									
LVD (low-voltage detector)	Yes									
MCG (multipurpose clock generator)	Yes									
OSC (crystal oscillator)	Yes									
Port I/O ²	69	54	69	54	36	69	54	69	54	36
RGPIO (rapid general-purpose I/O)	16				12	16				12
SCI1, SCI2 (serial communications interfaces)	Yes									
SPI1 (serial peripheral interface)	Yes									
SPI2 (serial peripheral interface)	Yes	No	Yes	No		Yes	No	Yes	No	
FTM1 (flexible timer module) channels	6				4	6				4
FTM2 channels	6	2	6	2	2	6	2	6	2	2

Table 1. MCF51AC256 Series Device Comparison (continued)

Feature	MCF51AC256A		MCF51AC256B			MCF51AC128A		MCF51AC128C		
	80-pin	64-pin	80-pin	64-pin	44-pin	80-pin	64-pin	80-pin	64-pin	44-pin
TPM3 (timer pulse-width modulator) channels	2									
VBUS (debug visibility bus)	Yes	No	Yes	No		Yes	No	Yes	No	

¹ The members of MCF51AC128A with CAN support have 32 KB RAM. The other members have 16 KB RAM.

² Up to 16 pins on Ports E and F are shared with the ColdFire Rapid GPIO module.

1.2 Block Diagram

Figure 1 shows the connections between the MCF51AC256 series pins and modules.

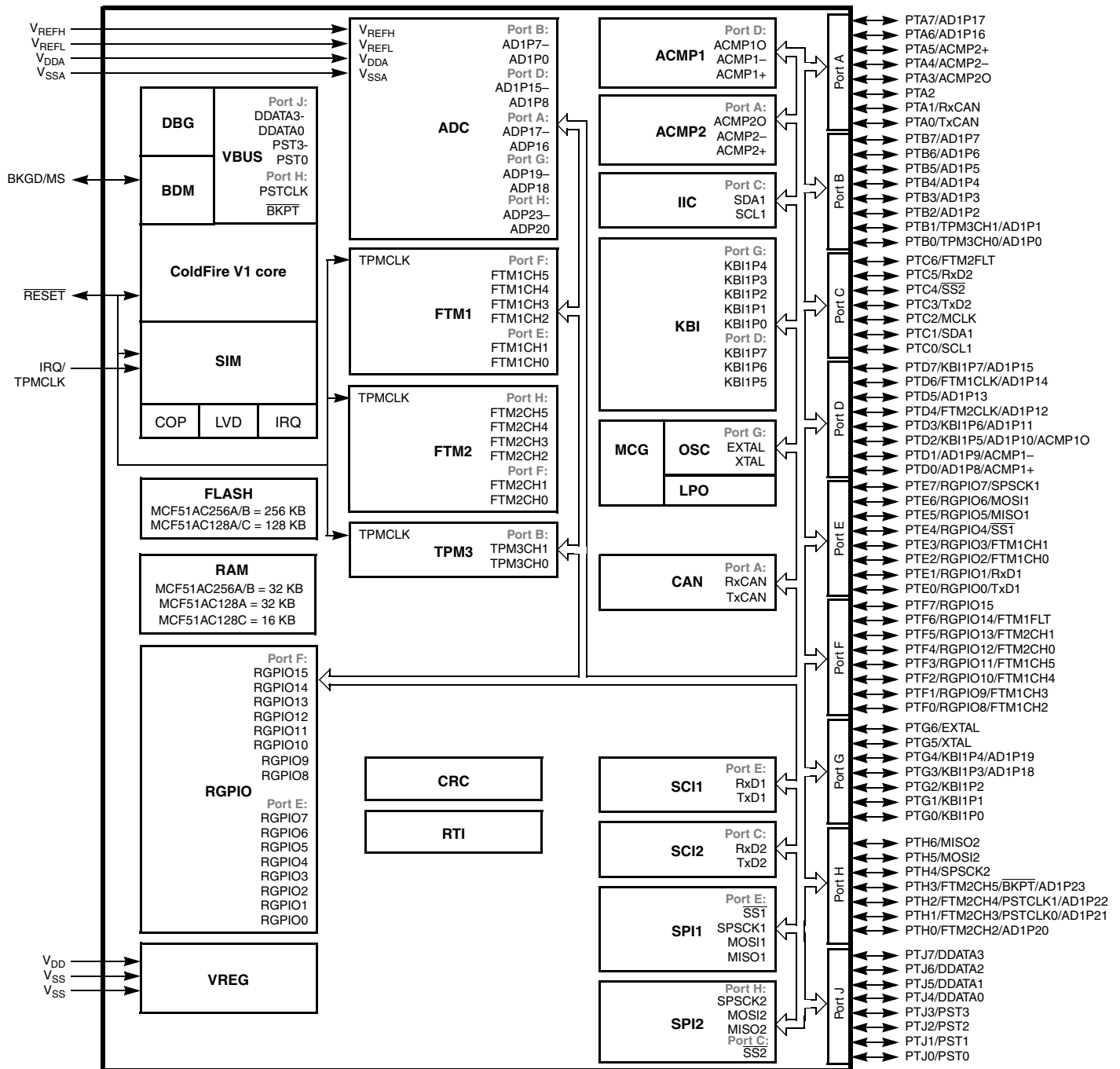


Figure 1. MCF51AC256 Series Block Diagram

MCF51AC256 Family Configurations

- Double-buffered transmit and receive
- Serial clock phase and polarity options
- Slave select output
- Selectable MSB-first or LSB-first shifting
- 16-bit and FIFO operations in SPI2
- Input/Output
 - 69 GPIOs
 - 8 keyboard interrupt pins with selectable polarity
 - Hysteresis and configurable pull-up device on all input pins; Configurable slew rate and drive strength on all output pins
 - 16-bits Rapid GPIO pins connected to the processor's local 32-bit platform bus with set, clear, and faster toggle functionality

1.4 Part Numbers

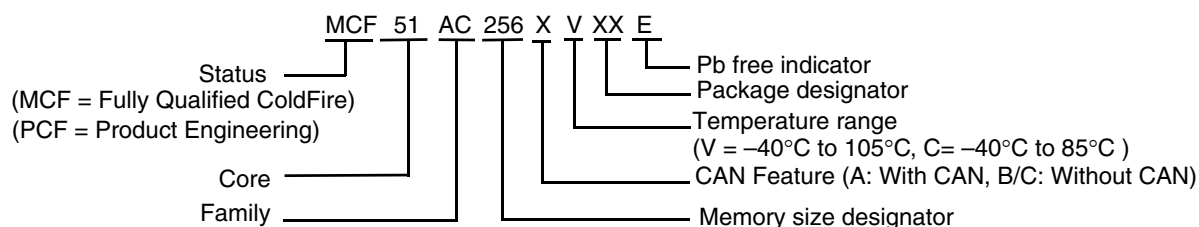


Table 3. Orderable Part Number Summary

Freescall Part Number	Description	Flash / SRAM (Kbytes)	Package	Temperature
MCF51AC256AVFUE	MCF51AC256 ColdFire Microcontroller with CAN	256 / 32	64 QFP	-40°C to 105°C
MCF51AC256BVFUE	MCF51AC256 ColdFire Microcontroller without CAN	256 / 32	64 QFP	-40°C to 105°C
MCF51AC256AVLKE	MCF51AC256 ColdFire Microcontroller with CAN	256 / 32	80 LQFP	-40°C to 105°C
MCF51AC256BVLKE	MCF51AC256 ColdFire Microcontroller without CAN	256 / 32	80 LQFP	-40°C to 105°C
MCF51AC256AVPUE	MCF51AC256 ColdFire Microcontroller with CAN	256 / 32	64 LQFP	-40°C to 105°C
MCF51AC256BVPUE	MCF51AC256 ColdFire Microcontroller without CAN	256 / 32	64 LQFP	-40°C to 105°C
MCF51AC128AVFUE	MCF51AC128 ColdFire Microcontroller with CAN	128 / 32	64 QFP	-40°C to 105°C
MCF51AC128CVFUE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	64 QFP	-40°C to 105°C
MCF51AC128AVLKE	MCF51AC128 ColdFire Microcontroller with CAN	128 / 32	80 LQFP	-40°C to 105°C
MCF51AC128CVLKE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	80 LQFP	-40°C to 105°C
MCF51AC128AVPUE	MCF51AC128 ColdFire Microcontroller with CAN	128 / 32	64 LQFP	-40°C to 105°C
MCF51AC128CVPUE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	64 LQFP	-40°C to 105°C
MCF51AC256ACFUE	MCF51AC256 ColdFire Microcontroller with CAN	256 / 32	64 QFP	-40°C to 85°C
MCF51AC256BCFUE	MCF51AC256 ColdFire Microcontroller without CAN	256 / 32	64 QFP	-40°C to 85°C
MCF51AC256ACLKE	MCF51AC256 ColdFire Microcontroller with CAN	256 / 32	80 LQFP	-40°C to 85°C
MCF51AC256BCLKE	MCF51AC256 ColdFire Microcontroller without CAN	256 / 32	80 LQFP	-40°C to 85°C

1.5 Pinouts and Packaging

Figure 2 shows the pinout of the 80-pin LQFP.

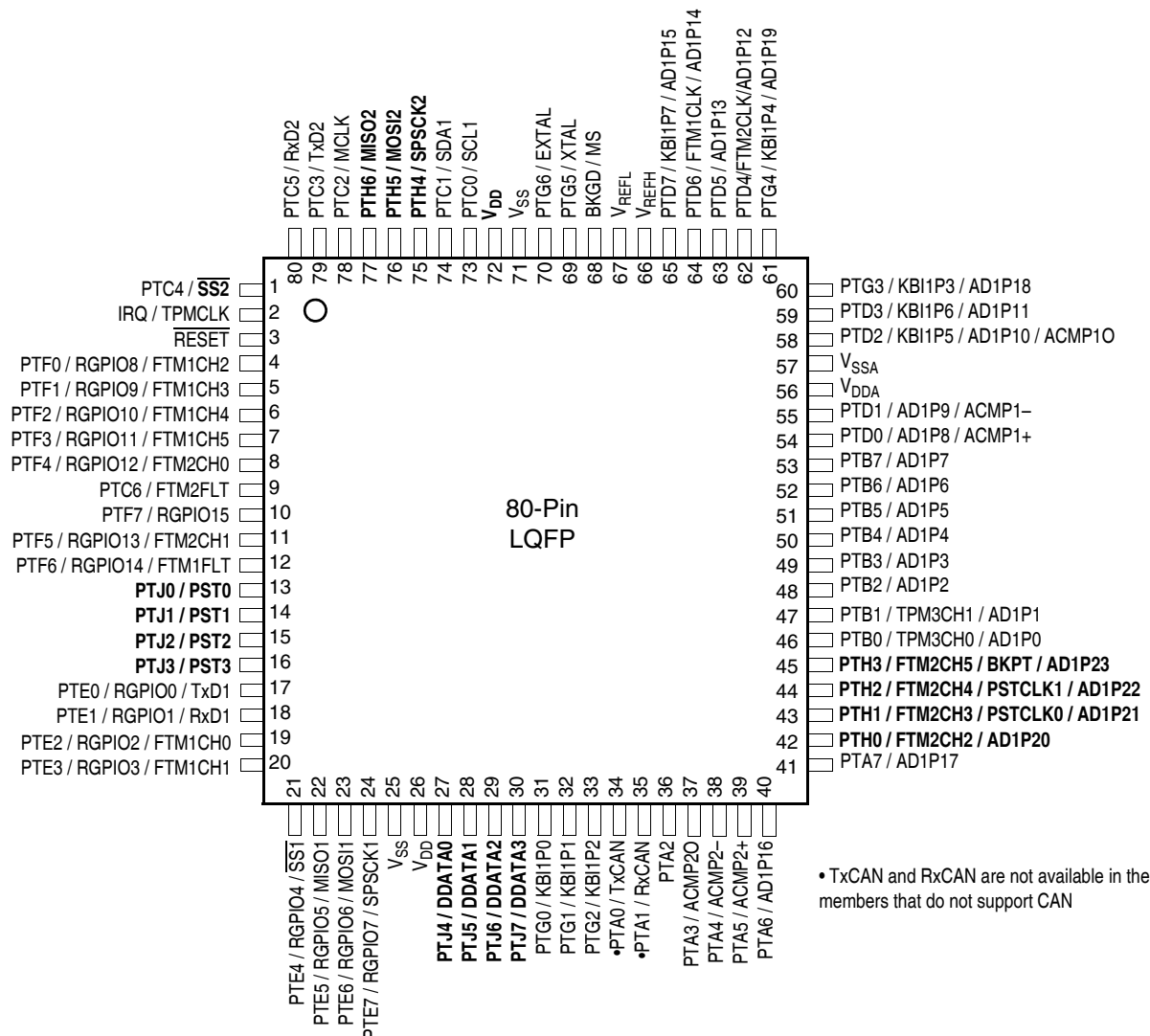


Figure 2. MCF51AC256 Series ColdFire Microcontroller 80-Pin LQFP

Figure 3 shows the pinout of the 64-pin LQFP and QFP.

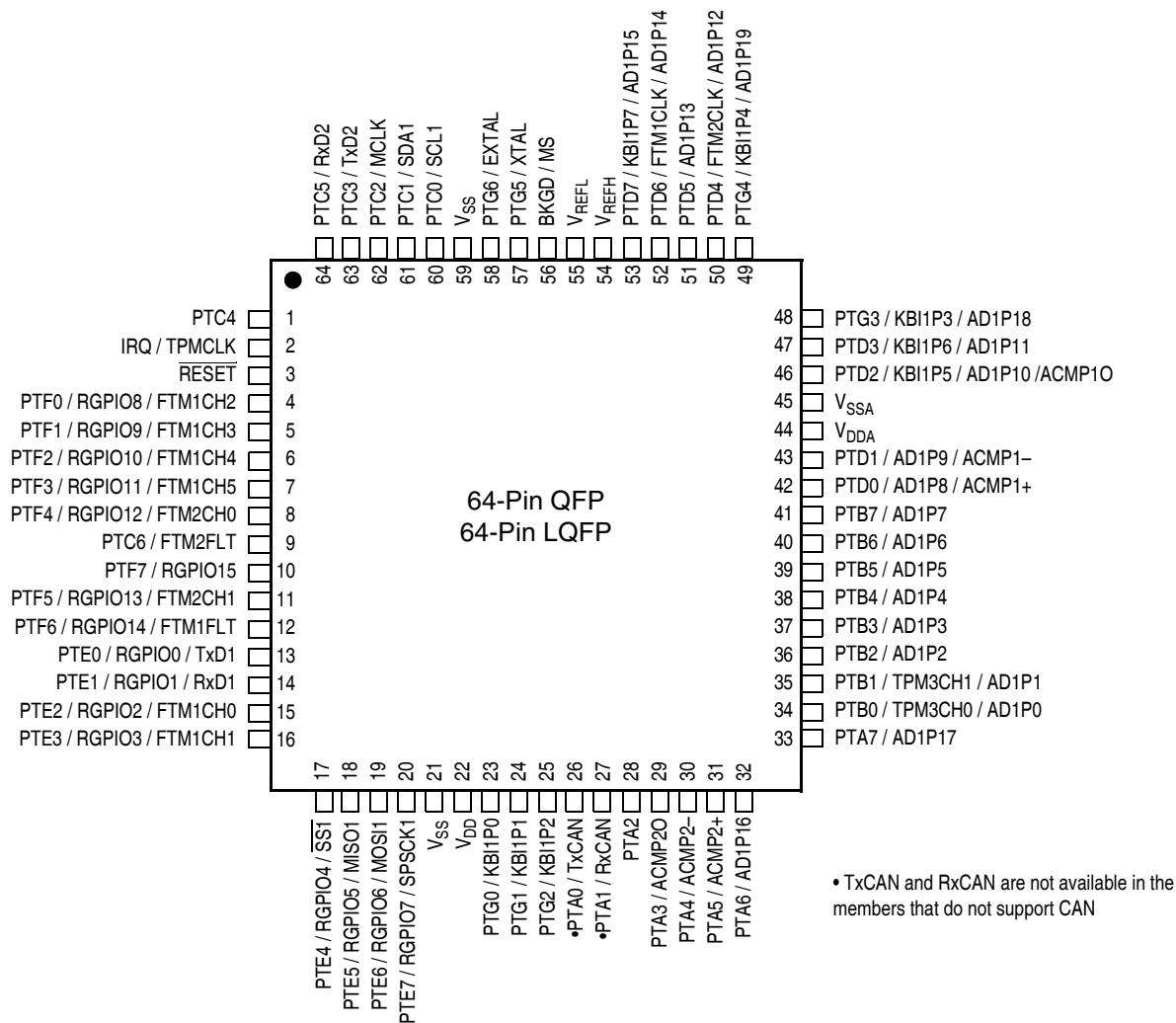


Figure 3. MCF51AC256 Series ColdFire Microcontroller 64-Pin QFP/LQFP

Figure 4 shows the pinout of the 44-pin LQFP.

Table 4. Pin Availability by Package Pin-Count (continued)

Pin Number			Lowest <-- Priority --> Highest			
80	64	44	Port Pin	Alt 1	Alt 2	Alt 3
49	37	26	PTB3	AD1P3		
50	38	—	PTB4	AD1P4		
51	39	—	PTB5	AD1P5		
52	40	—	PTB6	AD1P6		
53	41	—	PTB7	AD1P7		
54	42	27	PTD0	AD1P8	ACMP1+	
55	43	28	PTD1	AD1P9	ACMP1–	
56	44	29	V _{DDA}			
57	45	30	V _{SSA}			
58	46	31	PTD2	KBI1P5	AD1P10	ACMP1O
59	47	32	PTD3	KBI1P6	AD1P11	
60	48	33	PTG3	KBI1P3	AD1P18	
61	49	—	PTG4	KBI1P4	AD1P19	
62	50	—	PTD4	FTM2CLK	AD1P12	
63	51	—	PTD5	AD1P13		
64	52	—	PTD6	FTM1CLK	AD1P14	
65	53	—	PTD7	KBI1P7	AD1P15	
66	54	34	V _{REFH}			
67	55	35	V _{REFL}			
68	56	36	BKGD	MS		
69	57	37	PTG5	XTAL		
70	58	38	PTG6	EXTAL		
71	59	39	V _{SS}			
72	—	—	V _{DD}			
73	60	40	PTC0	SCL1		
74	61	41	PTC1	SDA1		
75	—	—	PTH4	SPCK2		
76	—	—	PTH5	MOSI2		
77	—	—	PTH6	MISO2		
78	62	42	PTC2	MCLK		
79	63	43	PTC3	TxD2		
80	64	44	PTC5	RxD2		

¹ TPMCLK, FTM1CLK, and FTM2CLK options are configured via software; out of reset, FTM1CLK, FTM2CLK, and TPMCLK are available to FTM1, FTM2, and TPM3 respectively.

² TxCAN is available in the member that supports CAN.

³ RxCAN is available in the member that supports CAN.

- ¹ Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance
- ² Junction to Ambient Natural Convection
- ³ 1s — Single layer board, one signal layer
- ⁴ 2s2p — Four layer board, 2 signal and 2 power layers

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \text{Eqn. 1}$$

where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power

$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} \ll P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273^\circ\text{C}) \quad \text{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273^\circ\text{C}) + \theta_{JA} \times (P_D)^2 \quad \text{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A . Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A .

2.4 Electrostatic Discharge (ESD) Protection Characteristics

Although damage from static discharge is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with CDF-AEC-Q00 Stress Test Qualification for Automotive Grade Integrated Circuits. (<http://www.aecouncil.com/>) This device was qualified to AEC-Q100 Rev E.

A device is considered to have failed if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete dc parametric and functional testing is performed per the

Electrical Characteristics

applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 8. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human body	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulse per pin	—	3	
Charge device model	Series resistance	R1	0	Ω
	Storage capacitance	C	0	pF
	Number of pulse per pin	—	3	—
Latch-up	Minimum input voltage limit	—	-2.5	V
	Maximum input voltage limit	—	7.5	V

Table 9. ESD and Latch-Up Protection Characteristics

Num	Rating	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	± 2000	—	V
2	Charge device model (CDM)	V_{CDM}	± 500	—	V
3	Latch-up current at $T_A = 85^\circ\text{C}$	I_{LAT}	± 100	—	mA

2.5 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

Table 10. DC Characteristics

Num	C	Parameter	Symbol	Min	Typical ¹	Max	Unit
1	—	Operating voltage		2.7	—	5.5	V
2	P	Output high voltage — Low drive (PTxDSn = 0) 5 V, $I_{Load} = -4$ mA 3 V, $I_{Load} = -2$ mA 5 V, $I_{Load} = -2$ mA 3 V, $I_{Load} = -1$ mA	V_{OH}	$V_{DD} - 1.5$ $V_{DD} - 1.5$ $V_{DD} - 0.8$ $V_{DD} - 0.8$	— — — —	— — — —	V
		Output high voltage — High drive (PTxDSn = 1) 5 V, $I_{Load} = -15$ mA 3 V, $I_{Load} = -8$ mA 5 V, $I_{Load} = -8$ mA 3 V, $I_{Load} = -4$ mA		$V_{DD} - 1.5$ $V_{DD} - 1.5$ $V_{DD} - 0.8$ $V_{DD} - 0.8$	— — — —	— — — —	

Table 10. DC Characteristics (continued)

Num	C	Parameter	Symbol	Min	Typical ¹	Max	Unit
3	P	Output low voltage — Low Drive (PTxDSn = 0) 5 V, I _{Load} = 4 mA 3 V, I _{Load} = 2 mA 5 V, I _{Load} = 2 mA 3 V, I _{Load} = 1 mA	V _{OL}	—	—	1.5 1.5 0.8 0.8	V
		Output low voltage — High Drive (PTxDSn = 1) 5 V, I _{Load} = 15 mA 3 V, I _{Load} = 8 mA 5 V, I _{Load} = 8 mA 3 V, I _{Load} = 4 mA		—	—	1.5 1.5 0.8 0.8	
4	C	Output high current — Max total I _{OH} for all ports 5V 3V	I _{OHT}	—	—	100 60	mA
5	C	Output low current — Max total I _{OL} for all ports 5 V 3 V	I _{OLT}	—	—	100 60	mA
6	P	Input high voltage; all digital inputs	V _{IH}	0.65 × V _{DD}	—	—	V
7	P	Input low voltage; all digital inputs	V _{IL}	—	—	0.35 × V _{DD}	V
8	D	Input hysteresis; all digital inputs	V _{hys}	0.06 × V _{DD}	—	—	mV
9	P	Input leakage current; input only pins ²	I _{in}	—	0.1	1	μA
10	P	High impedance (off-state) leakage current ²	I _{OZ}	—	0.1	1	μA
11	P	Internal pullup resistors ³	R _{PU}	20	45	65	kΩ
12	P	Internal pulldown resistors ⁴	R _{PD}	20	45	65	kΩ
13	C	Input capacitance; all non-supply pins	C _{In}	—	—	8	pF
14	P	POR rearm voltage	V _{POR}	0.9	1.4	2.0	V
15	D	POR rearm time	t _{POR}	10	—	—	μs
16	P	Low-voltage detection threshold — high range V _{DD} falling V _{DD} rising	V _{LVDH}	4.2 4.27	4.35 4.4	4.5 4.6	V
17	P	Low-voltage detection threshold — low range V _{DD} falling V _{DD} rising	V _{LVDL}	2.48 2.5	2.68 2.7	2.7 2.72	V
18	P	Low-voltage warning threshold — high range V _{DD} falling V _{DD} rising	V _{LVWH}	4.2 4.27	4.4 4.45	4.5 4.6	V
19	P	Low-voltage warning threshold low range V _{DD} falling V _{DD} rising	V _{LVWL}	2.48 2.5	2.68 2.7	2.7 2.72	V
20	T	Low-voltage inhibit reset/recover hysteresis 5 V 3 V	V _{hys}	—	100 60	—	mV
21	D	RAM retention voltage	V _{RAM}	—	0.6	1.0	V

Table 10. DC Characteristics (continued)

Num	C	Parameter	Symbol	Min	Typical ¹	Max	Unit
22	D	DC injection current ^{5 6 7 8} (single pin limit) $V_{IN} > V_{DD}$ $V_{IN} < V_{SS}$	I_{IC}	0 0	—	2 -0.2	mA
		DC injection current (Total MCU limit, includes sum of all stressed pins) $V_{IN} > V_{DD}$ $V_{IN} < V_{SS}$		0 0	—	25 -5	mA

¹ Typical values are based on characterization data at 25°C unless otherwise stated.

² Measured with $V_{IN} = V_{DD}$ or V_{SS} .

³ Measured with $V_{IN} = V_{SS}$.

⁴ Measured with $V_{IN} = V_{DD}$.

⁵ Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{IN} > V_{DD}$) is greater than I_{DD} , the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

⁶ All functional non-supply pins are internally clamped to V_{SS} and V_{DD} .

⁷ Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

⁸ The **RESET** pin does not have a clamp diode to V_{DD} . Do not drive this pin above V_{DD} .

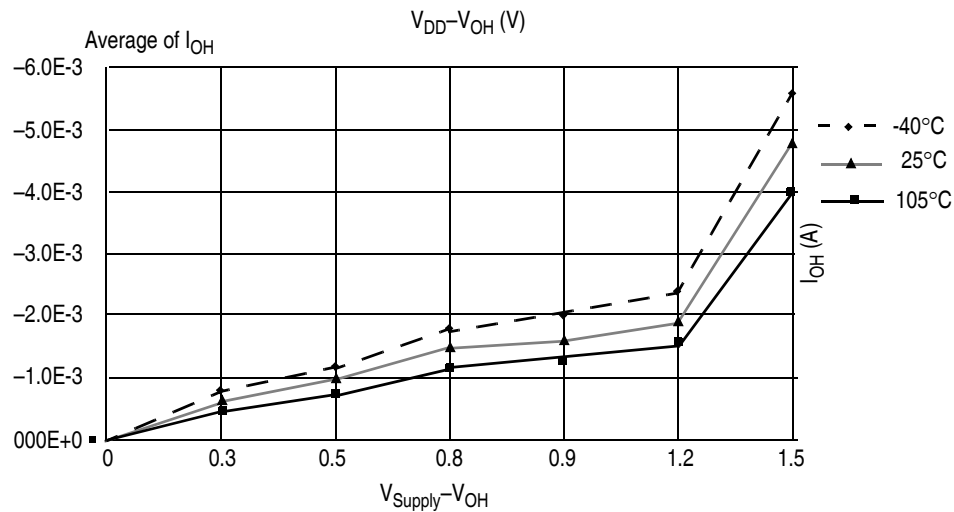


Figure 5. Typical I_{OH} vs. $V_{DD} - V_{OH}$ at $V_{DD} = 3$ V (Low Drive, $PTxDSn = 0$)

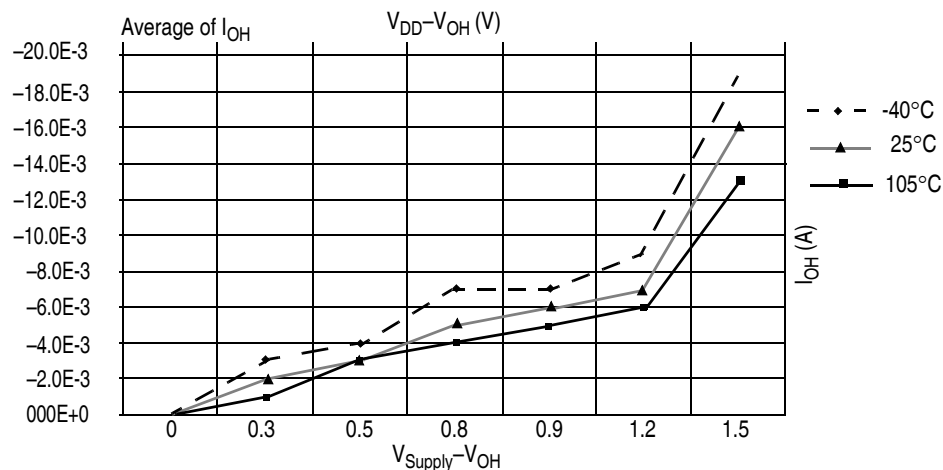


Figure 6. Typical I_{OH} vs. $V_{DD} - V_{OH}$ at $V_{DD} = 3$ V (High Drive, PTxDSn = 1)

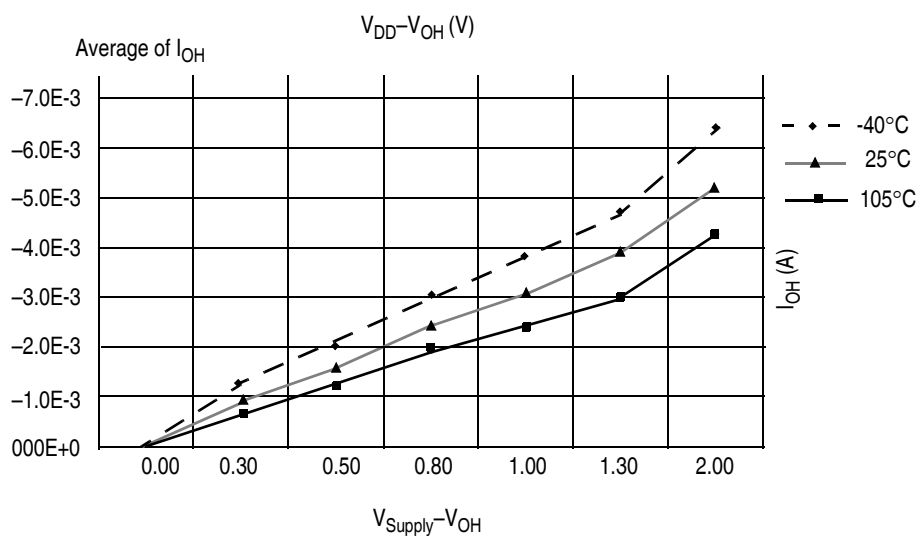
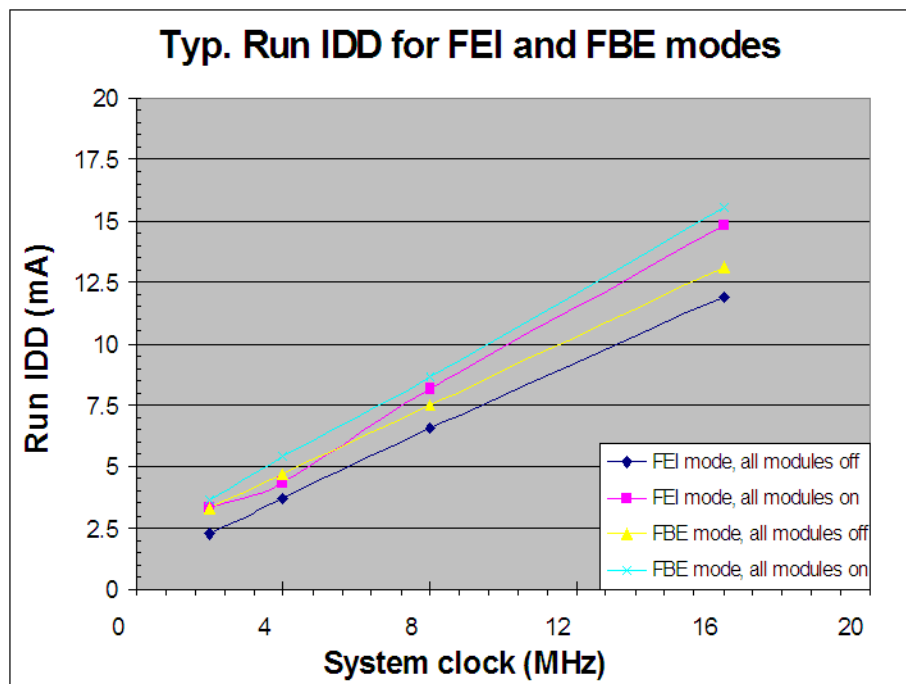


Figure 7. Typical I_{OH} vs. $V_{DD} - V_{OH}$ at $V_{DD} = 5$ V (Low Drive, PTxDSn = 0)


Figure 9. Typical Run I_{DD} vs. System Clock Freq. for FEI and FBE Modes

2.7 Analog Comparator (ACMP) Electricals

Table 12. Analog Comparator Electrical Specifications

Num	C	Rating	Symbol	Min	Typical	Max	Unit
1	—	Supply voltage	V_{DD}	2.7	—	5.5	V
2	T	Supply current (active)	I_{DDAC}	—	20	35	μA
3	D	Analog input voltage	V_{AIN}	$V_{SS} - 0.3$	—	V_{DD}	V
4	D	Analog input offset voltage	V_{AIO}	—	20	40	mV
5	D	Analog comparator hysteresis	V_H	3.0	6.0	20.0	mV
6	D	Analog input leakage current	I_{ALKG}	—	—	1.0	μA
7	D	Analog comparator initialization delay	t_{AINIT}	—	—	1.0	μs
8	P	Bandgap voltage reference factory trimmed at $V_{DD} = 5.3248$ V, Temp = 25 °C	V_{BG}	1.18	1.20	1.21	V

2.8 ADC Characteristics

Table 13. 5 Volt 12-bit ADC Operating Conditions

Num	C	Characteristic	Conditions	Symb	Min	Typical ¹	Max	Unit	Comment
1	D	Supply voltage	Absolute	V_{DDA}	2.7	—	5.5	V	
	D		Delta to V_{DD} ($V_{DD} - V_{DDA}$) ²	ΔV_{DDA}	−100	0	100	mV	
2	D	Ground voltage	Delta to V_{SS} ($V_{SS} - V_{SSA}$) ²	ΔV_{SSA}	−100	0	100	mV	
3	D	Reference voltage high		V_{REFH}	2.7	V_{DDA}	V_{DDA}	V	
4	D	Reference voltage low		V_{REFL}	V_{SSA}	V_{SSA}	V_{SSA}	V	
5	D	Input voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
6	C	Input capacitance		C_{ADIN}	—	4.5	5.5	pF	
7	C	Input resistance		R_{ADIN}	—	3	5	k Ω	
8	C	Analog source resistance	12-bit mode $f_{ADCK} > 4\text{MHz}$ $f_{ADCK} < 4\text{MHz}$	R_{AS}	— —	— —	2 5	k Ω	External to MCU
	C		10-bit mode $f_{ADCK} > 4\text{MHz}$ $f_{ADCK} < 4\text{MHz}$		— —	— —	5 10		
	C		8-bit mode (all valid f_{ADCK})		—	—	10		
9	D	ADC conversion clock frequency	High speed (ADLPC = 0)	f_{ADCK}	0.4	—	8.0	MHz	
	D		Low power (ADLPC = 1)		0.4	—	4.0		

¹ Typical values assume $V_{DDA} = 5.0\text{ V}$, Temp = 25 °C, $f_{ADCK} = 1.0\text{ MHz}$ unless otherwise stated. Typical values are for reference only and are not tested in production.

² DC potential difference.

Table 16. MCG Frequency Specifications (continued)(Temperature Range = –40 to 105 °C Ambient)

Num	C	Rating	Symbol	Min	Typical ¹	Max	Unit
18	D	Lock exit frequency tolerance ⁸	D _{unl}	±4.47	—	±5.97	%
19	D	Lock time — FLL	t _{fil_lock}	—	—	t _{fil_acquire} + 1075(1/f _{int_t})	s
20	D	Lock time — PLL	t _{pll_lock}	—	—	t _{pll_acquire} + 1075(1/f _{pll_ref})	s
21	D	Loss of external clock minimum frequency — RANGE = 0	f _{loc_low}	(3/5) × f _{int}	—	—	kHz

¹ Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.

² The resulting bus clock frequency must not exceed the maximum specified bus clock frequency of the device.

³ This specification applies when the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

⁴ This specification applies when the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

⁵ Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

⁶ 625 ns represents 5 time quanta for CAN applications, under worst case conditions of 8 MHz CAN bus clock, 1 Mbps CAN bus speed, and 8 time quanta per bit for bit time settings. 5 time quanta is the minimum time between a synchronization edge and the sample point of a bit using 8 time quanta per bit.

⁷ Below D_{lock} minimum, the MCG enters lock. Above D_{lock} maximum, the MCG will not enter lock. But if the MCG is already in lock, then the MCG may stay in lock.

⁸ Below D_{unl} minimum, the MCG will not exit lock if already in lock. Above D_{unl} maximum, the MCG is guaranteed to exit lock.

2.11 AC Characteristics

This section describes ac timing characteristics for each peripheral system.

2.11.2 Timer (TPM/FTM) Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 18. TPM/FTM Input Timing

NUM	C	Function	Symbol	Min	Max	Unit
1	—	External clock frequency	f_{TPMext}	DC	$f_{\text{Bus}}/4$	MHz
2	—	External clock period	t_{TPMext}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

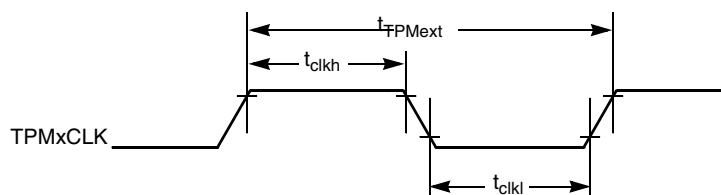


Figure 13. Timer External Clock

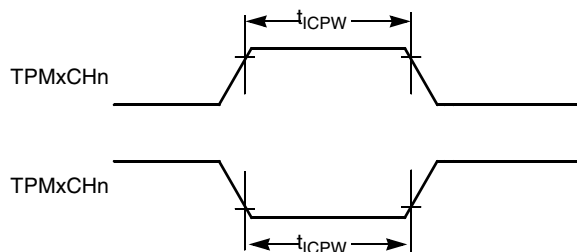


Figure 14. Timer Input Capture Pulse

2.11.3 MSCAN

Table 19. MSCAN Wake-Up Pulse Characteristics

Num	C	Parameter	Symbol	Min	Typical ¹	Max	Unit
1	D	MSCAN wake-up dominant pulse filtered	t_{WUP}	—	—	2	μs
2	D	MSCAN wake-up dominant pulse pass	t_{WUP}	5	—	5	μs

¹ Typical values are based on characterization data at $V_{\text{DD}} = 5.0 \text{ V}$, 25°C unless otherwise stated.

2.12 SPI Characteristics

Table 20 and Figure 15 through Figure 18 describe the timing requirements for the SPI system.

Table 20. SPI Timing

No.	C	Function	Symbol	Min	Max	Unit
—	D	Operating frequency Master Slave	f_{op}	$f_{Bus}/2048$ 0	$f_{Bus}/2$ $f_{Bus}/4$	Hz
1	D	SPSCK period Master Slave	t_{SPSCK}	2 4	2048 —	t_{cyc} t_{cyc}
2	D	Enable lead time Master Slave	t_{Lead}	1/2 1	— —	t_{SPSCK} t_{cyc}
3	D	Enable lag time Master Slave	t_{Lag}	1/2 1	— —	t_{SPSCK} t_{cyc}
4	D	Clock (SPSCK) high or low time Master Slave	t_{WSPSCK}	$t_{cyc} - 30$ $t_{cyc} - 30$	$1024 t_{cyc}$ —	ns ns
5	D	Data setup time (inputs) Master Slave	t_{SU}	15 15	— —	ns ns
6	D	Data hold time (inputs) Master Slave	t_{HI}	0 25	— —	ns ns
7	D	Slave access time	t_a	—	1	t_{cyc}
8	D	Slave MISO disable time	t_{dis}	—	1	t_{cyc}
9	D	Data valid (after SPSCK edge) Master Slave	t_v	— —	25 25	ns ns
10	D	Data hold time (outputs) Master Slave	t_{HO}	0 0	— —	ns ns
11	D	Rise time Input Output	t_{RI} t_{RO}	— —	$t_{cyc} - 25$ 25	ns ns
12	D	Fall time Input Output	t_{FI} t_{FO}	— —	$t_{cyc} - 25$ 25	ns ns

Table 21. Flash Characteristics

Num	C	Characteristic	Symbol	Min	Typical ¹	Max	Unit
1	—	Supply voltage for program/erase	$V_{\text{prog/erase}}$	2.7	—	5.5	V
2	—	Supply voltage for read operation	V_{Read}	2.7	—	5.5	V
3	—	Internal FCLK frequency ²	f_{FCLK}	150	—	200	kHz
4	—	Internal FCLK period (1/FCLK)	t_{Fcyc}	5	—	6.67	μs
5	—	Byte program time (random location) ²	t_{prog}	9			t_{Fcyc}
6	—	Byte program time (burst mode) ²	t_{Burst}	4			t_{Fcyc}
7	—	Page erase time ³	t_{Page}	4000			t_{Fcyc}
8	—	Mass erase time ²	t_{Mass}	20,000			t_{Fcyc}
9	C	Program/erase endurance ⁴ T_L to $T_H = -40\text{ }^{\circ}\text{C}$ to $105\text{ }^{\circ}\text{C}$ $T = 25\text{ }^{\circ}\text{C}$	—	10,000 —	— 100,000	— —	cycles
10	C	Data retention ⁵	$t_{\text{D_ret}}$	15	100	—	years

¹ Typical values are based on characterization data at $V_{\text{DD}} = 5.0\text{ V}$, $25\text{ }^{\circ}\text{C}$ unless otherwise stated.

² The frequency of this clock is controlled by a software setting.

³ These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

⁴ **Typical endurance for flash** was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale Semiconductor defines typical endurance, please refer to Engineering Bulletin EB619/D, *Typical Endurance for Nonvolatile Memory*.

⁵ **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to $25\text{ }^{\circ}\text{C}$ using the Arrhenius equation. For additional information on how Freescale Semiconductor defines typical data retention, please refer to Engineering Bulletin EB618/D, *Typical Data Retention for Nonvolatile Memory*.

2.14 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

2.14.1 Radiated Emissions

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM Cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (North and East). For more detailed information concerning the evaluation results, conditions and setup, please refer to the EMC Evaluation Report for this device.

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