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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I ² C, SCI, SPI
Peripherals	LVD, PWM, WDT
Number of I/O	54
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 20x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/pcf51ac128ccpue

Table of Contents

1	MCF51AC256 Family Configurations	3
1.1	Device Comparison	3
1.2	Block Diagram	4
1.3	Features	6
1.3.1	Feature List	7
1.4	Part Numbers	10
1.5	Pinouts and Packaging	12
2	Electrical Characteristics	17
2.1	Parameter Classification	17
2.2	Absolute Maximum Ratings	17
2.3	Thermal Characteristics	18
2.4	Electrostatic Discharge (ESD) Protection Characteristics	19
2.5	DC Characteristics	20
2.6	Supply Current Characteristics	25
2.7	Analog Comparator (ACMP) Electricals	27
2.8	ADC Characteristics	28
2.9	External Oscillator (XOSC) Characteristics	31
2.10	MCG Specifications	32
2.11	AC Characteristics	33
2.11.1	Control Timing	34
2.11.2	Timer (TPM/FTM) Module Timing	35
2.11.3	MSCAN	35
2.12	SPI Characteristics	36
2.13	Flash Specifications	38
2.14	EMC Performance	39
2.14.1	Radiated Emissions	39
3	Mechanical Outline Drawings	40
4	Revision History	41

List of Figures

Figure 1.	MCF51AC256 Series Block Diagram	5
Figure 2.	MCF51AC256 Series ColdFire Microcontroller 80-Pin LQFP	12
Figure 3.	MCF51AC256 Series ColdFire Microcontroller 64-Pin QFP/LQFP	13
Figure 4.	MCF51AC256 Series ColdFire Microcontroller 44-Pin LQFP	14
Figure 5.	Typical I_{OH} vs. $V_{DD}-V_{OH}$ at $V_{DD} = 3\text{ V}$ (Low Drive, $PTxDSn = 0$)	22
Figure 6.	Typical I_{OH} vs. $V_{DD}-V_{OH}$ at $V_{DD} = 3\text{ V}$ (High Drive, $PTxDSn = 1$)	23
Figure 7.	Typical I_{OH} vs. $V_{DD}-V_{OH}$ at $V_{DD} = 5\text{ V}$ (Low Drive, $PTxDSn = 0$)	23

Figure 8.	Typical I_{OH} vs. $V_{DD}-V_{OH}$ at $V_{DD} = 5\text{ V}$ (High Drive, $PTxDSn = 1$)	24
Figure 9.	Typical Run I_{DD} vs. System Clock Freq. for FEI and FBE Modes	27
Figure 10.	ADC Input Impedance Equivalency Diagram	29
Figure 11.	Reset Timing	34
Figure 12.	IRQ/KBIPx Timing	34
Figure 13.	Timer External Clock	35
Figure 14.	Timer Input Capture Pulse	35
Figure 15.	SPI Master Timing (CPHA = 0)	37
Figure 16.	SPI Master Timing (CPHA = 1)	37
Figure 17.	SPI Slave Timing (CPHA = 0)	38
Figure 18.	SPI Slave Timing (CPHA = 1)	38

List of Tables

Table 1.	MCF51AC256 Series Device Comparison	3
Table 2.	MCF51AC256 Series Functional Units	6
Table 3.	Orderable Part Number Summary	10
Table 4.	Pin Availability by Package Pin-Count	14
Table 5.	Parameter Classifications	17
Table 6.	Absolute Maximum Ratings	18
Table 7.	Thermal Characteristics	18
Table 8.	ESD and Latch-up Test Conditions	20
Table 9.	ESD and Latch-Up Protection Characteristics	20
Table 10.	DC Characteristics	20
Table 11.	Supply Current Characteristics	25
Table 12.	Analog Comparator Electrical Specifications	27
Table 13.	5 Volt 12-bit ADC Operating Conditions	28
Table 14.	5 Volt 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)	29
Table 15.	Oscillator Electrical Specifications (Temperature Range = -40 to $105\text{ }^{\circ}\text{C}$ Ambient)	31
Table 16.	MCG Frequency Specifications (Temperature Range = -40 to $105\text{ }^{\circ}\text{C}$ Ambient)	32
Table 17.	Control Timing	34
Table 18.	TPM/FTM Input Timing	35
Table 19.	MSCAN Wake-Up Pulse Characteristics	35
Table 20.	SPI Timing	36
Table 21.	Flash Characteristics	39
Table 22.	Package Information	40
Table 23.	Revision History	41

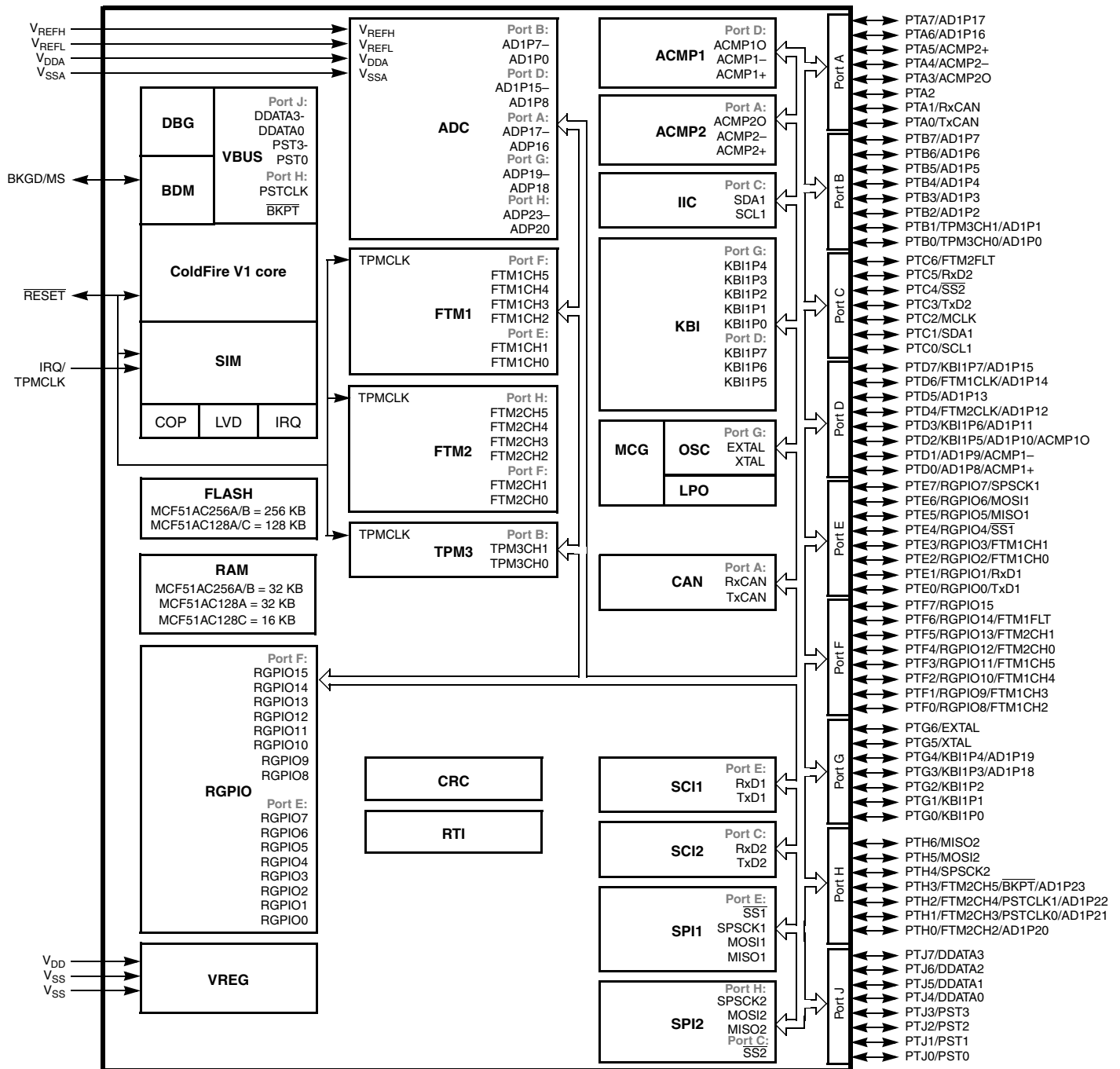


Figure 1. MCF51AC256 Series Block Diagram

1.3 Features

Table 2 describes the functional units of the MCF51AC256 series.

Table 2. MCF51AC256 Series Functional Units

Functional Unit	Function
CF1 Core (V1 ColdFire core)	Executes programs and interrupt handlers
BDM (background debug module)	Provides single pin debugging interface (part of the V1 ColdFire core)
DBG (debug)	Provides debugging and emulation capabilities (part of the V1 ColdFire core)
VBUS (debug visibility bus)	Allows for real-time program traces (part of the V1 ColdFire core)
SIM (system integration module)	Controls resets and chip level interfaces between modules
Flash (flash memory)	Provides storage for program code, constants and variables
RAM (random-access memory)	Provides storage for program variables
RGPIO (rapid general-purpose input/output)	Allows for I/O port access at CPU clock speeds
VREG (voltage regulator)	Controls power management across the device
COP (computer operating properly)	Monitors a countdown timer and generates a reset if the timer is not regularly reset by the software
LVD (low-voltage detect)	Monitors internal and external supply voltage levels, and generates a reset or interrupt when the voltages are too low
CF1_INTIC (interrupt controller)	Controls and prioritizes all device interrupts
ADC (analog-to-digital converter)	Measures analog voltages at up to 12 bits of resolution
FTM1, FTM2 (flexible timer/pulse-width modulators)	Provides a variety of timing-based features
TPM3 (timer/pulse-width modulator)	Provides a variety of timing-based features
CRC (cyclic redundancy check)	Accelerates computation of CRC values for ranges of memory
ACMP1, ACMP2 (analog comparators)	Compares two analog inputs
IIC (inter-integrated circuit)	Supports standard IIC communications protocol
KBI (keyboard interrupt)	Provides pin interrupt capabilities
MCG (multipurpose clock generator)	Provides clocking options for the device, including a phase-locked loop (PLL) and frequency-locked loop (FLL) for multiplying slower reference clock sources
OSC (crystal oscillator)	Allows a crystal or ceramic resonator to be used as the system clock source or reference clock for the PLL or FLL
LPO (low-power oscillator)	Provides a second clock source for COP and RTI.
CAN (controller area network)	Supports standard CAN communications protocol
SCI1, SCI2 (serial communications interfaces)	Serial communications UARTs capable of supporting RS-232 and LIN protocols
SPI1 (8-bit serial peripheral interfaces)	Provides 8-bit 4-pin synchronous serial interface
SPI2 (16-bit serial peripheral interfaces)	Provides 16-bit 4-pin synchronous serial interface with FIFO

- Inter-integrated circuit (IIC)
 - Compatible with IIC bus standard
 - Multi-master operation
 - Software programmable for one of 64 different serial clock frequencies
 - Interrupt driven byte-by-byte data transfer
 - Arbitration lost interrupt with automatic mode switching from master to slave
 - Calling address identification interrupt
 - Bus busy detection
 - 10-bit address extension
- Controller area network (CAN)
 - Implementation of the CAN protocol — Version 2.0A/B
 - Standard and extended data frames
 - Zero to eight bytes data length
 - Programmable bit rate up to 1 Mbps
 - Support for remote frames
 - Five receive buffers with FIFO storage scheme
 - Three transmit buffers with internal prioritization using a “local priority” concept
 - Flexible maskable identifier filter supports two full-size (32-bit) extended identifier filters, four 16-bit filters, or eight 8-bit filters
 - Programmable wakeup functionality with integrated low-pass filter
 - Programmable loopback mode supports self-test operation
 - Programmable listen-only mode for monitoring of CAN bus
 - Programmable bus-off recovery functionality
 - Separate signalling and interrupt capabilities for all CAN receiver and transmitter error states (warning, error passive, bus-off)
 - Internal timer for time-stamping of received and transmitted messages
- Serial communications interfaces (SCI)
 - Full-duplex, standard non-return-to-zero (NRZ) format
 - Double-buffered transmitter and receiver with separate enables
 - Programmable baud rates (13-bit modulo divider)
 - Interrupt-driven or polled operation
 - Hardware parity generation and checking
 - Programmable 8-bit or 9-bit character length
 - Receiver wakeup by idle-line or address-mark
 - Optional 13-bit break character generation / 11-bit break character detection
 - Selectable transmitter output polarity
- Serial peripheral interfaces (SPI)
 - Master or slave mode operation
 - Full-duplex or single-wire bidirectional option
 - Programmable transmit bit rate

MCF51AC256 Family Configurations

- Double-buffered transmit and receive
- Serial clock phase and polarity options
- Slave select output
- Selectable MSB-first or LSB-first shifting
- 16-bit and FIFO operations in SPI2
- Input/Output
 - 69 GPIOs
 - 8 keyboard interrupt pins with selectable polarity
 - Hysteresis and configurable pull-up device on all input pins; Configurable slew rate and drive strength on all output pins
 - 16-bits Rapid GPIO pins connected to the processor's local 32-bit platform bus with set, clear, and faster toggle functionality

1.4 Part Numbers

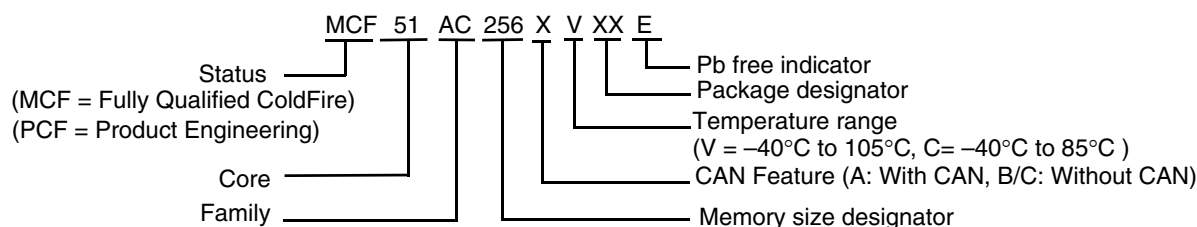


Table 3. Orderable Part Number Summary

Freescal Part Number	Description	Flash / SRAM (Kbytes)	Package	Temperature
MCF51AC256AVFUE	MCF51AC256 ColdFire Microcontroller with CAN	256 / 32	64 QFP	-40°C to 105°C
MCF51AC256BVFUE	MCF51AC256 ColdFire Microcontroller without CAN	256 / 32	64 QFP	-40°C to 105°C
MCF51AC256AVLKE	MCF51AC256 ColdFire Microcontroller with CAN	256 / 32	80 LQFP	-40°C to 105°C
MCF51AC256BVLKE	MCF51AC256 ColdFire Microcontroller without CAN	256 / 32	80 LQFP	-40°C to 105°C
MCF51AC256AVPUE	MCF51AC256 ColdFire Microcontroller with CAN	256 / 32	64 LQFP	-40°C to 105°C
MCF51AC256BVPUE	MCF51AC256 ColdFire Microcontroller without CAN	256 / 32	64 LQFP	-40°C to 105°C
MCF51AC128AVFUE	MCF51AC128 ColdFire Microcontroller with CAN	128 / 32	64 QFP	-40°C to 105°C
MCF51AC128CVFUE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	64 QFP	-40°C to 105°C
MCF51AC128AVLKE	MCF51AC128 ColdFire Microcontroller with CAN	128 / 32	80 LQFP	-40°C to 105°C
MCF51AC128CVLKE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	80 LQFP	-40°C to 105°C
MCF51AC128AVPUE	MCF51AC128 ColdFire Microcontroller with CAN	128 / 32	64 LQFP	-40°C to 105°C
MCF51AC128CVPUE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	64 LQFP	-40°C to 105°C
MCF51AC256ACFUE	MCF51AC256 ColdFire Microcontroller with CAN	256 / 32	64 QFP	-40°C to 85°C
MCF51AC256BCFUE	MCF51AC256 ColdFire Microcontroller without CAN	256 / 32	64 QFP	-40°C to 85°C
MCF51AC256ACLKE	MCF51AC256 ColdFire Microcontroller with CAN	256 / 32	80 LQFP	-40°C to 85°C
MCF51AC256BCLKE	MCF51AC256 ColdFire Microcontroller without CAN	256 / 32	80 LQFP	-40°C to 85°C

Table 3. Orderable Part Number Summary

MCF51AC256ACPUE	MCF51AC256 ColdFire Microcontroller with CAN	256 / 32	64 LQFP	–40°C to 85°C
MCF51AC256BCPUE	MCF51AC256 ColdFire Microcontroller without CAN	256 / 32	64 LQFP	–40°C to 85°C
MCF51AC256BCFGE	MCF51AC256 ColdFire Microcontroller without CAN	256/32	44 LQFP	–40°C to 85°C
MCF51AC128ACFUE	MCF51AC128 ColdFire Microcontroller with CAN	128 / 32	64 QFP	–40°C to 85°C
MCF51AC128CCFUE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	64 QFP	–40°C to 85°C
MCF51AC128ACLKE	MCF51AC128 ColdFire Microcontroller with CAN	128 / 32	80 LQFP	–40°C to 85°C
MCF51AC128CCLKE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	80 LQFP	–40°C to 85°C
MCF51AC128ACPUE	MCF51AC128 ColdFire Microcontroller with CAN	128 / 32	64 LQFP	–40°C to 85°C
MCF51AC128CCPUE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	64 LQFP	–40°C to 85°C
MCF51AC128CCFGE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	44 LQFP	–40°C to 85°C

1.5 Pinouts and Packaging

Figure 2 shows the pinout of the 80-pin LQFP.

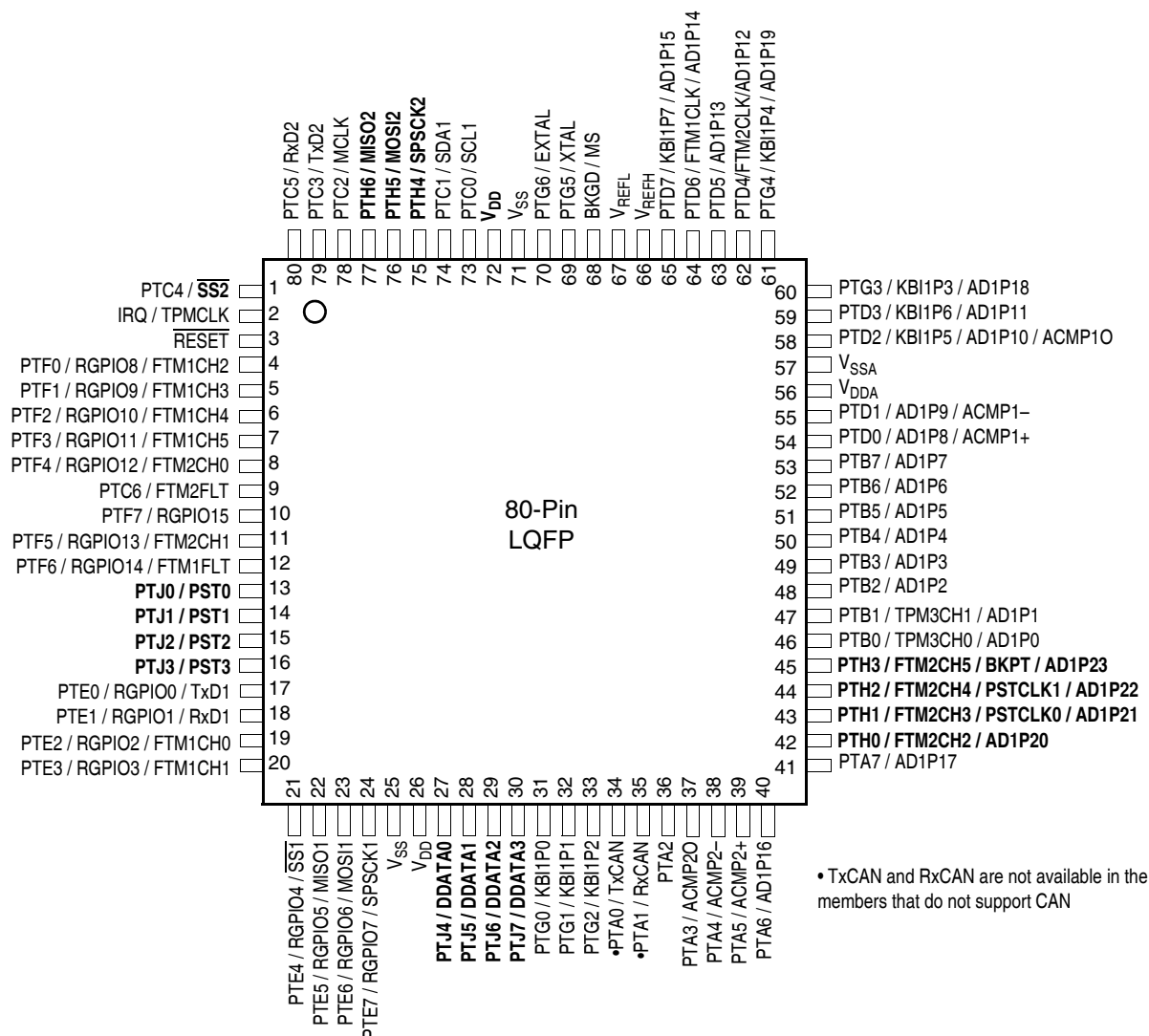
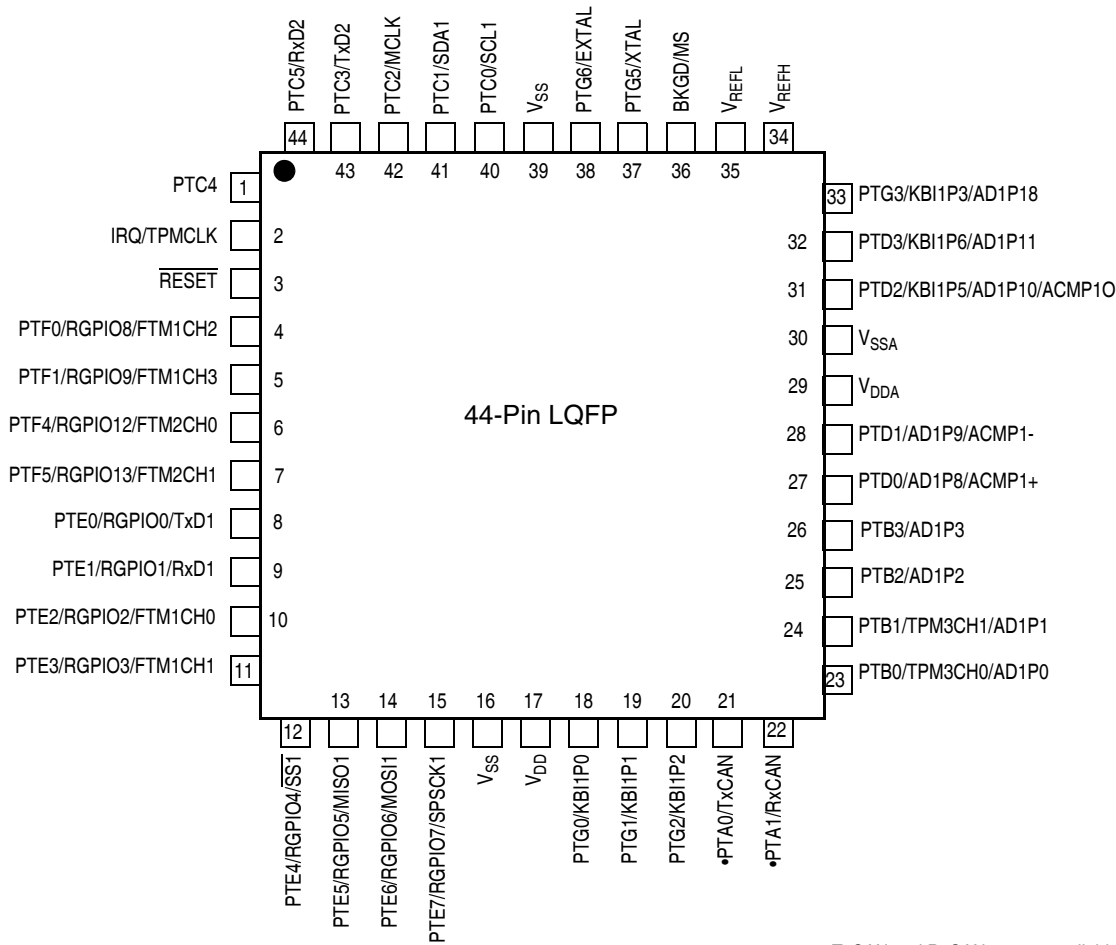


Figure 2. MCF51AC256 Series ColdFire Microcontroller 80-Pin LQFP

Figure 3 shows the pinout of the 64-pin LQFP and QFP.



• TxCAN and RxCAN are not available in the members that do not support CAN

Figure 4. MCF51AC256 Series ColdFire Microcontroller 44-Pin LQFP

Table 4 shows the package pin assignments.

Table 4. Pin Availability by Package Pin-Count

Pin Number			Lowest <-- Priority --> Highest			
80	64	44	Port Pin	Alt 1	Alt 2	Alt 3
1	1	1	PTC4	SS2		
2	2	2	IRQ	TPMCLK ¹		
3	3	3	RESET			
4	4	4	PTF0	RGPIO8	FTM1CH2	
5	5	5	PTF1	RGPIO9	FTM1CH3	
6	6	—	PTF2	RGPIO10	FTM1CH4	
7	7	—	PTF3	RGPIO11	FTM1CH5	

Table 4. Pin Availability by Package Pin-Count (continued)

Pin Number			Lowest <-- Priority --> Highest			
80	64	44	Port Pin	Alt 1	Alt 2	Alt 3
8	8	6	PTF4	RGPIO12	FTM2CH0	
9	9	—	PTC6	FTM2FLT		
10	10	—	PTF7	RGPIO15		
11	11	7	PTF5	RGPIO13	FTM2CH1	
12	12	—	PTF6	RGPIO14	FTM1FLT	
13	—	—	PTJ0	PST0		
14	—	—	PTJ1	PST1		
15	—	—	PTJ2	PST2		
16	—	—	PTJ3	PST3		
17	13	8	PTE0	RGPIO0	TxD1	
18	14	9	PTE1	RGPIO1	RxD1	
19	15	10	PTE2	RGPIO2	FTM1CH0	
20	16	11	PTE3	RGPIO3	FTM1CH1	
21	17	12	PTE4	RGPIO4	SS1	
22	18	13	PTE5	RGPIO5	MISO1	
23	19	14	PTE6	RGPIO6	MOSI1	
24	20	15	PTE7	RGPIO7	SPSCK1	
25	21	16	V _{SS}			
26	22	17	V _{DD}			
27	—	—	PTJ4	DDATA0		
28	—	—	PTJ5	DDATA1		
29	—	—	PTJ6	DDATA2		
30	—	—	PTJ7	DDATA3		
31	23	18	PTG0	KBI1P0		
32	24	19	PTG1	KBI1P1		
33	25	20	PTG2	KBI1P2		
34	26	21	PTA0	TxCAN ²		
35	27	22	PTA1	RxCAN ³		
36	28	—	PTA2			
37	29	—	PTA3	ACMP20		
38	30	—	PTA4	ACMP2–		
39	31	—	PTA5	ACMP2+		
40	32	—	PTA6	AD1P16		
41	33	—	PTA7	AD1P17		
42	—	—	PTH0	FTM2CH2	AD1P20	
43	—	—	PTH1	FTM2CH3	PSTCLK0	AD1P21
44	—	—	PTH2	FTM2CH4	PSTCLK1	AD1P22
45	—	—	PTH3	FTM2CH5	BKPT	AD1P23
46	34	23	PTB0	TPM3CH0	AD1P0	
47	35	24	PTB1	TPM3CH1	AD1P1	
48	36	25	PTB2	AD1P2		

Table 6. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	−0.3 to 5.8	V
Input voltage	V_{In}	−0.3 to $V_{DD} + 0.3$	V
Instantaneous maximum current Single pin limit (applies to all port pins) ^{1, 2, 3}	I_D	±25	mA
Maximum current into V_{DD}	I_{DD}	120	mA
Storage temperature	T_{stg}	−55 to 150	°C

¹ Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

² All functional non-supply pins are internally clamped to V_{SS} and V_{DD} .

³ Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD} , the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low which would reduce overall power consumption.

2.3 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and it is user-determined rather than being controlled by the MCU design. In order to take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 7. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	−40 to 105	°C
Maximum junction temperature	T_J	150	°C
Thermal resistance ^{1,2,3,4}			
80-pin LQFP			
1s		51	
2s2p		38	
64-pin LQFP			
1s		59	
2s2p	θ_{JA}	41	°C/W
64-pin QFP			
1s		50	
2s2p		36	
44-pin LQFP			
1s		67	
2s2p		45	

Electrical Characteristics

applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 8. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human body	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulse per pin	—	3	
Charge device model	Series resistance	R1	0	Ω
	Storage capacitance	C	0	pF
	Number of pulse per pin	—	3	—
Latch-up	Minimum input voltage limit	—	-2.5	V
	Maximum input voltage limit	—	7.5	V

Table 9. ESD and Latch-Up Protection Characteristics

Num	Rating	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	± 2000	—	V
2	Charge device model (CDM)	V_{CDM}	± 500	—	V
3	Latch-up current at $T_A = 85^\circ\text{C}$	I_{LAT}	± 100	—	mA

2.5 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

Table 10. DC Characteristics

Num	C	Parameter	Symbol	Min	Typical ¹	Max	Unit
1	—	Operating voltage		2.7	—	5.5	V
2	P	Output high voltage — Low drive (PTxDSn = 0) 5 V, $I_{Load} = -4$ mA 3 V, $I_{Load} = -2$ mA 5 V, $I_{Load} = -2$ mA 3 V, $I_{Load} = -1$ mA	V_{OH}	$V_{DD} - 1.5$ $V_{DD} - 1.5$ $V_{DD} - 0.8$ $V_{DD} - 0.8$	— — — —	— — — —	V
		Output high voltage — High drive (PTxDSn = 1) 5 V, $I_{Load} = -15$ mA 3 V, $I_{Load} = -8$ mA 5 V, $I_{Load} = -8$ mA 3 V, $I_{Load} = -4$ mA		$V_{DD} - 1.5$ $V_{DD} - 1.5$ $V_{DD} - 0.8$ $V_{DD} - 0.8$	— — — —	— — — —	

Table 10. DC Characteristics (continued)

Num	C	Parameter	Symbol	Min	Typical ¹	Max	Unit
3	P	Output low voltage — Low Drive (PTxDSn = 0) 5 V, I _{Load} = 4 mA 3 V, I _{Load} = 2 mA 5 V, I _{Load} = 2 mA 3 V, I _{Load} = 1 mA	V _{OL}	—	—	1.5 1.5 0.8 0.8	V
		Output low voltage — High Drive (PTxDSn = 1) 5 V, I _{Load} = 15 mA 3 V, I _{Load} = 8 mA 5 V, I _{Load} = 8 mA 3 V, I _{Load} = 4 mA		—	—	1.5 1.5 0.8 0.8	
4	C	Output high current — Max total I _{OH} for all ports 5V 3V	I _{OHT}	—	—	100 60	mA
5	C	Output low current — Max total I _{OL} for all ports 5 V 3 V	I _{OLT}	—	—	100 60	mA
6	P	Input high voltage; all digital inputs	V _{IH}	0.65 × V _{DD}	—	—	V
7	P	Input low voltage; all digital inputs	V _{IL}	—	—	0.35 × V _{DD}	V
8	D	Input hysteresis; all digital inputs	V _{hys}	0.06 × V _{DD}	—	—	mV
9	P	Input leakage current; input only pins ²	I _{in}	—	0.1	1	μA
10	P	High impedance (off-state) leakage current ²	I _{OZ}	—	0.1	1	μA
11	P	Internal pullup resistors ³	R _{PU}	20	45	65	kΩ
12	P	Internal pulldown resistors ⁴	R _{PD}	20	45	65	kΩ
13	C	Input capacitance; all non-supply pins	C _{In}	—	—	8	pF
14	P	POR rearm voltage	V _{POR}	0.9	1.4	2.0	V
15	D	POR rearm time	t _{POR}	10	—	—	μs
16	P	Low-voltage detection threshold — high range V _{DD} falling V _{DD} rising	V _{LVDH}	4.2 4.27	4.35 4.4	4.5 4.6	V
17	P	Low-voltage detection threshold — low range V _{DD} falling V _{DD} rising	V _{LVDL}	2.48 2.5	2.68 2.7	2.7 2.72	V
18	P	Low-voltage warning threshold — high range V _{DD} falling V _{DD} rising	V _{LVWH}	4.2 4.27	4.4 4.45	4.5 4.6	V
19	P	Low-voltage warning threshold low range V _{DD} falling V _{DD} rising	V _{LVWL}	2.48 2.5	2.68 2.7	2.7 2.72	V
20	T	Low-voltage inhibit reset/recover hysteresis 5 V 3 V	V _{hys}	—	100 60	—	mV
21	D	RAM retention voltage	V _{RAM}	—	0.6	1.0	V

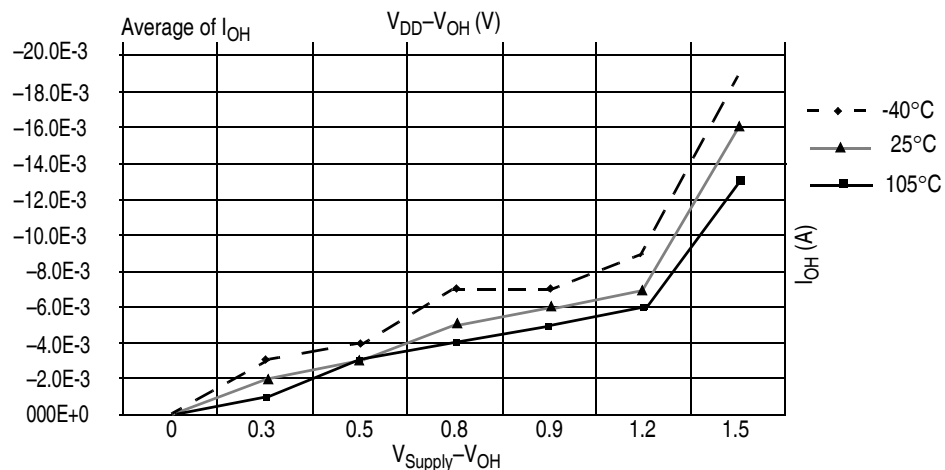


Figure 6. Typical I_{OH} vs. $V_{DD} - V_{OH}$ at $V_{DD} = 3$ V (High Drive, PTxDSn = 1)

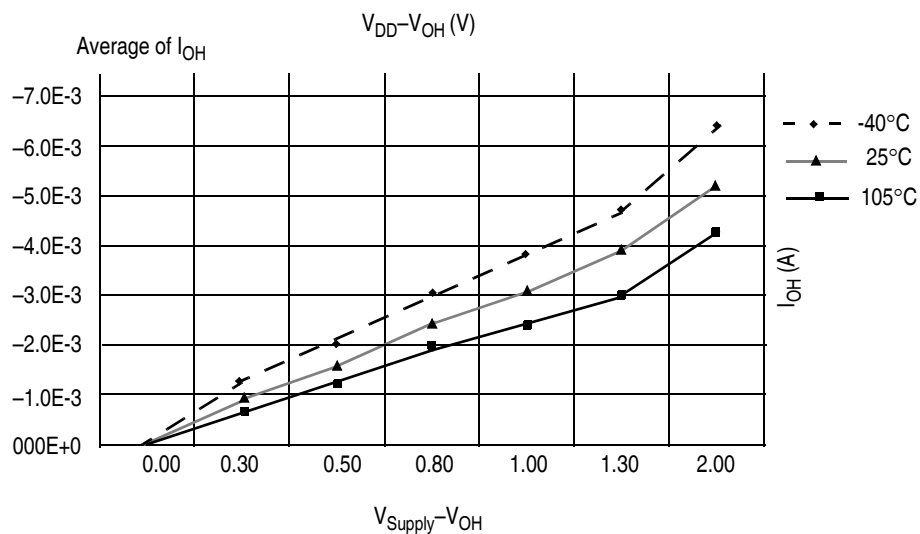


Figure 7. Typical I_{OH} vs. $V_{DD} - V_{OH}$ at $V_{DD} = 5$ V (Low Drive, PTxDSn = 0)

Table 11. Supply Current Characteristics (continued)

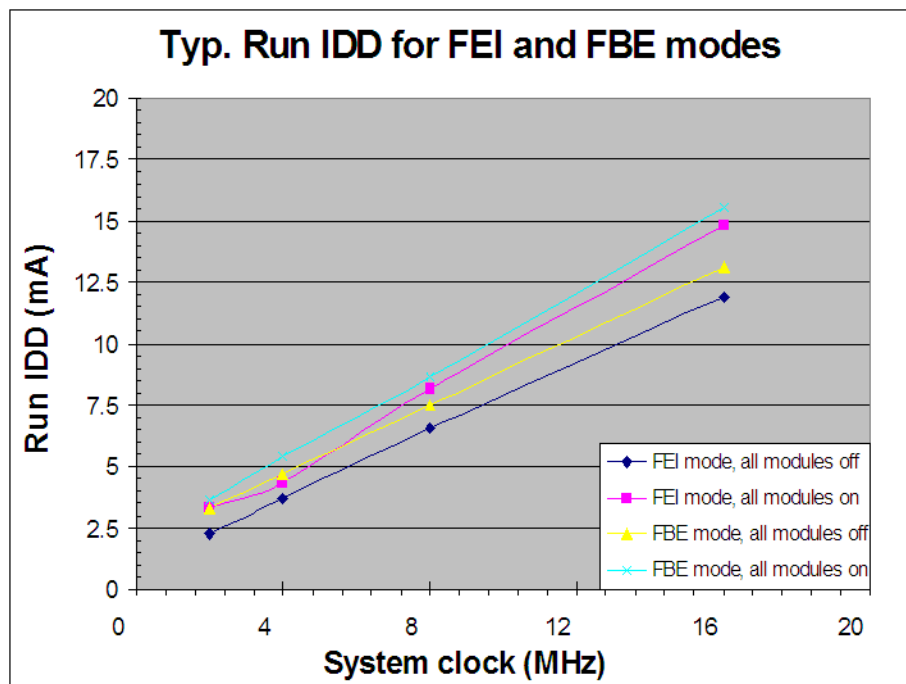
Num	C	Parameter	Symbol	V _{DD} (V)	Typical ¹	Max ²	Unit
5	C	Wait mode supply ³ current measured at (CPU clock = 2 MHz, f _{BUS} = 1 MHz)	W _I DD	5	1.3	2	mA
				3	1.29	2	
6	C	Wait mode supply ³ current measured at (CPU clock = 16 MHz, f _{BUS} = 8 MHz)		5	5.11	8	mA
				3	5.1	8	
7	C	Wait mode supply ³ current measured at (CPU clock = 50 MHz, f _{BUS} = 25 MHz)		5	15.24	25	mA
				3	15.2	25	
8	C	Stop2 mode supply current -40 °C 25 °C 120 °C	S2I _{DD}	5	1.40	2.5 2.5 200	μA
				3	1.16	2.5 2.5 200	μA
				5	1.60	2.5 2.5 220	μA
				3	1.35	2.5 2.5 220	μA
9	C	Stop3 mode supply current -40 °C 25 °C 120 °C	S3I _{DD}	5	1.60	2.5 2.5 220	μA
				3	1.35	2.5 2.5 220	μA
10	C	RTI adder to stop2 or stop3 ³ , 25 °C	S23I _{DDRTI}	5	300		nA
				3	300		nA
11	C	Adder to stop3 for oscillator enabled ⁴ (ERCLKEN = 1 and EREFSTEN = 1)	S3I _{DDOSC}	5, 3	5		μA

¹ Typicals are measured at 25 °C.

² Values given here are preliminary estimates prior to completing characterization.

³ Most customers are expected to find that auto-wakeup from stop2 or stop3 can be used instead of the higher current wait mode.

⁴ Values given under the following conditions: low range operation (RANGE = 0), low power mode (HGO = 0).


Figure 9. Typical Run I_{DD} vs. System Clock Freq. for FEI and FBE Modes

2.7 Analog Comparator (ACMP) Electricals

Table 12. Analog Comparator Electrical Specifications

Num	C	Rating	Symbol	Min	Typical	Max	Unit
1	—	Supply voltage	V_{DD}	2.7	—	5.5	V
2	T	Supply current (active)	I_{DDAC}	—	20	35	μA
3	D	Analog input voltage	V_{AIN}	$V_{SS} - 0.3$	—	V_{DD}	V
4	D	Analog input offset voltage	V_{AIO}	—	20	40	mV
5	D	Analog comparator hysteresis	V_H	3.0	6.0	20.0	mV
6	D	Analog input leakage current	I_{ALKG}	—	—	1.0	μA
7	D	Analog comparator initialization delay	t_{AINIT}	—	—	1.0	μs
8	P	Bandgap voltage reference factory trimmed at $V_{DD} = 5.3248$ V, Temp = 25 °C	V_{BG}	1.18	1.20	1.21	V

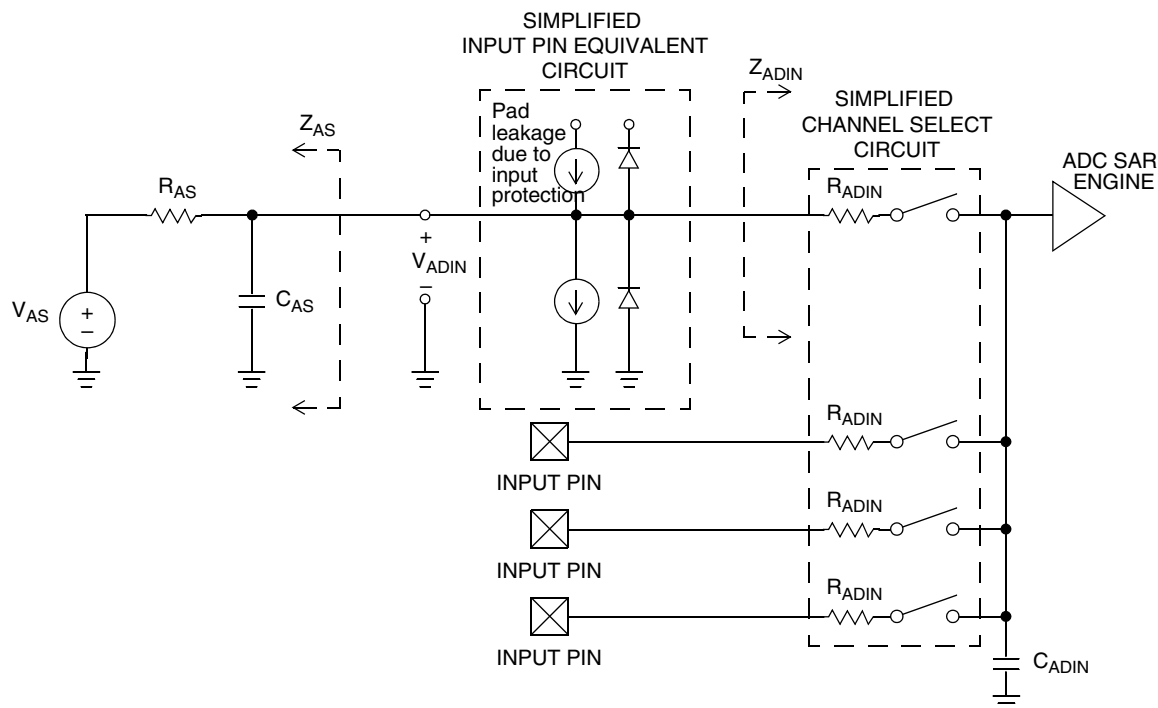


Figure 10. ADC Input Impedance Equivalency Diagram

Table 14. 5 Volt 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Num	C	Characteristic	Conditions	Symb	Min	Typical ¹	Max	Unit	Comment
1	T	Supply current ADLPC = 1 ADLSMP = 1 ADCO = 1		I_{DDA}	—	133	—	μA	
2	T	Supply current ADLPC = 1 ADLSM = 0 ADCO = 1		I_{DDA}	—	218	—	μA	
3	T	Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1		I_{DDA}	—	327	—	μA	
4	D	Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1		I_{DDA}	—	0.582	1	mA	
5	T	Supply current	Stop, reset, module off	I_{DDA}	—	0.011	1	μA	
6	P	ADC asynchronous clock source	High speed (ADLPC = 0)	f_{ADACK}	2	3.3	5	MHz	$t_{ADACK} = 1/f_{ADACK}$
			Low power (ADLPC = 1)		1.25	2	3.3		

³ Monotonicity and No-Missing-Codes guaranteed in 10-bit and 8-bit modes

⁴ Based on input pad leakage current. Refer to pad electricals.

2.9 External Oscillator (XOSC) Characteristics

Table 15. Oscillator Electrical Specifications (Temperature Range = –40 to 105 °C Ambient)

Num	C	Rating	Symbol	Min	Typical ¹	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1)					
		Low range (RANGE = 0)	f_{lo}	32	—	38.4	kHz
		High range (RANGE = 1) FEE or FBE mode ²	f_{hi-ll}	1	—	5	MHz
		High range (RANGE = 1) PEE or PBE mode ³	f_{hi-pll}	1	—	16	MHz
		High range (RANGE = 1, HGO = 1) BLPE mode	f_{hi-hgo}	1	—	16	MHz
		High range (RANGE = 1, HGO = 0) BLPE mode	f_{hi-lp}	1	—	8	MHz
2	—	Load capacitors	C_1 C_2	See crystal or resonator manufacturer's recommendation.			
3	—	Feedback resistor	R_F		10		MΩ
		Low range (32 kHz to 38.4 kHz) High range (1 MHz to 16 MHz)			1		
4	—	Series resistor	R_S				kΩ
		Low range, low gain (RANGE = 0, HGO = 0)		—	0	—	
		Low range, high gain (RANGE = 0, HGO = 1)		—	100	—	
		High range, low gain (RANGE = 1, HGO = 0)		—	0	—	
		High range, high gain (RANGE = 1, HGO = 1)		—	0	0	
		≥ 8 MHz		—	0	0	
5	T	Crystal start-up time ⁴					ms
		Low range, low gain (RANGE = 0, HGO = 0)	$t_{CSTL-LP}$	—	200	—	
		Low range, high gain (RANGE = 0, HGO = 1)	$t_{CSTL-HGO}$	—	400	—	
		High range, low gain (RANGE = 1, HGO = 0) ⁵	$t_{CSTH-LP}$	—	5	—	
		High range, high gain (RANGE = 1, HGO = 1) ⁵	$t_{CSTH-HGO}$	—	15	—	
6	T	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1)					MHz
		FEE or FBE mode ²	f_{extal}	0.03125	—	5	
		PEE or PBE mode ³		1	—	16	
		BLPE mode		0	—	40	

¹ Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.

² When MCG is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.

³ When MCG is configured for PEE or PBE mode, input clock source must be divisible using RDIV to within the range of 1 MHz to 2 MHz.

⁴ This parameter is characterized and not tested on each device. Proper PC board layout procedures must be followed to achieve specifications.

⁵ 4 MHz crystal

Table 16. MCG Frequency Specifications (continued)(Temperature Range = –40 to 105 °C Ambient)

Num	C	Rating	Symbol	Min	Typical ¹	Max	Unit
18	D	Lock exit frequency tolerance ⁸	D _{unl}	±4.47	—	±5.97	%
19	D	Lock time — FLL	t _{fil_lock}	—	—	t _{fil_acquire} + 1075(1/f _{int_t})	s
20	D	Lock time — PLL	t _{pll_lock}	—	—	t _{pll_acquire} + 1075(1/f _{pll_ref})	s
21	D	Loss of external clock minimum frequency — RANGE = 0	f _{loc_low}	(3/5) × f _{int}	—	—	kHz

¹ Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.

² The resulting bus clock frequency must not exceed the maximum specified bus clock frequency of the device.

³ This specification applies when the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

⁴ This specification applies when the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

⁵ Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

⁶ 625 ns represents 5 time quanta for CAN applications, under worst case conditions of 8 MHz CAN bus clock, 1 Mbps CAN bus speed, and 8 time quanta per bit for bit time settings. 5 time quanta is the minimum time between a synchronization edge and the sample point of a bit using 8 time quanta per bit.

⁷ Below D_{lock} minimum, the MCG enters lock. Above D_{lock} maximum, the MCG will not enter lock. But if the MCG is already in lock, then the MCG may stay in lock.

⁸ Below D_{unl} minimum, the MCG will not exit lock if already in lock. Above D_{unl} maximum, the MCG is guaranteed to exit lock.

2.11 AC Characteristics

This section describes ac timing characteristics for each peripheral system.

Table 21. Flash Characteristics

Num	C	Characteristic	Symbol	Min	Typical ¹	Max	Unit
1	—	Supply voltage for program/erase	$V_{\text{prog/erase}}$	2.7	—	5.5	V
2	—	Supply voltage for read operation	V_{Read}	2.7	—	5.5	V
3	—	Internal FCLK frequency ²	f_{FCLK}	150	—	200	kHz
4	—	Internal FCLK period (1/FCLK)	t_{Fcyc}	5	—	6.67	μs
5	—	Byte program time (random location) ²	t_{prog}	9			t_{Fcyc}
6	—	Byte program time (burst mode) ²	t_{Burst}	4			t_{Fcyc}
7	—	Page erase time ³	t_{Page}	4000			t_{Fcyc}
8	—	Mass erase time ²	t_{Mass}	20,000			t_{Fcyc}
9	C	Program/erase endurance ⁴ T_L to $T_H = -40\text{ }^{\circ}\text{C}$ to $105\text{ }^{\circ}\text{C}$ $T = 25\text{ }^{\circ}\text{C}$	—	10,000 —	— 100,000	— —	cycles
10	C	Data retention ⁵	$t_{\text{D-ret}}$	15	100	—	years

¹ Typical values are based on characterization data at $V_{\text{DD}} = 5.0\text{ V}$, $25\text{ }^{\circ}\text{C}$ unless otherwise stated.

² The frequency of this clock is controlled by a software setting.

³ These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

⁴ **Typical endurance for flash** was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale Semiconductor defines typical endurance, please refer to Engineering Bulletin EB619/D, *Typical Endurance for Nonvolatile Memory*.

⁵ **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to $25\text{ }^{\circ}\text{C}$ using the Arrhenius equation. For additional information on how Freescale Semiconductor defines typical data retention, please refer to Engineering Bulletin EB618/D, *Typical Data Retention for Nonvolatile Memory*.

2.14 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

2.14.1 Radiated Emissions

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM Cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (North and East). For more detailed information concerning the evaluation results, conditions and setup, please refer to the EMC Evaluation Report for this device.

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