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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	CANbus, I ² C, SCI, SPI
Peripherals	LVD, PWM, WDT
Number of I/O	69
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/pcf51ac256aclke

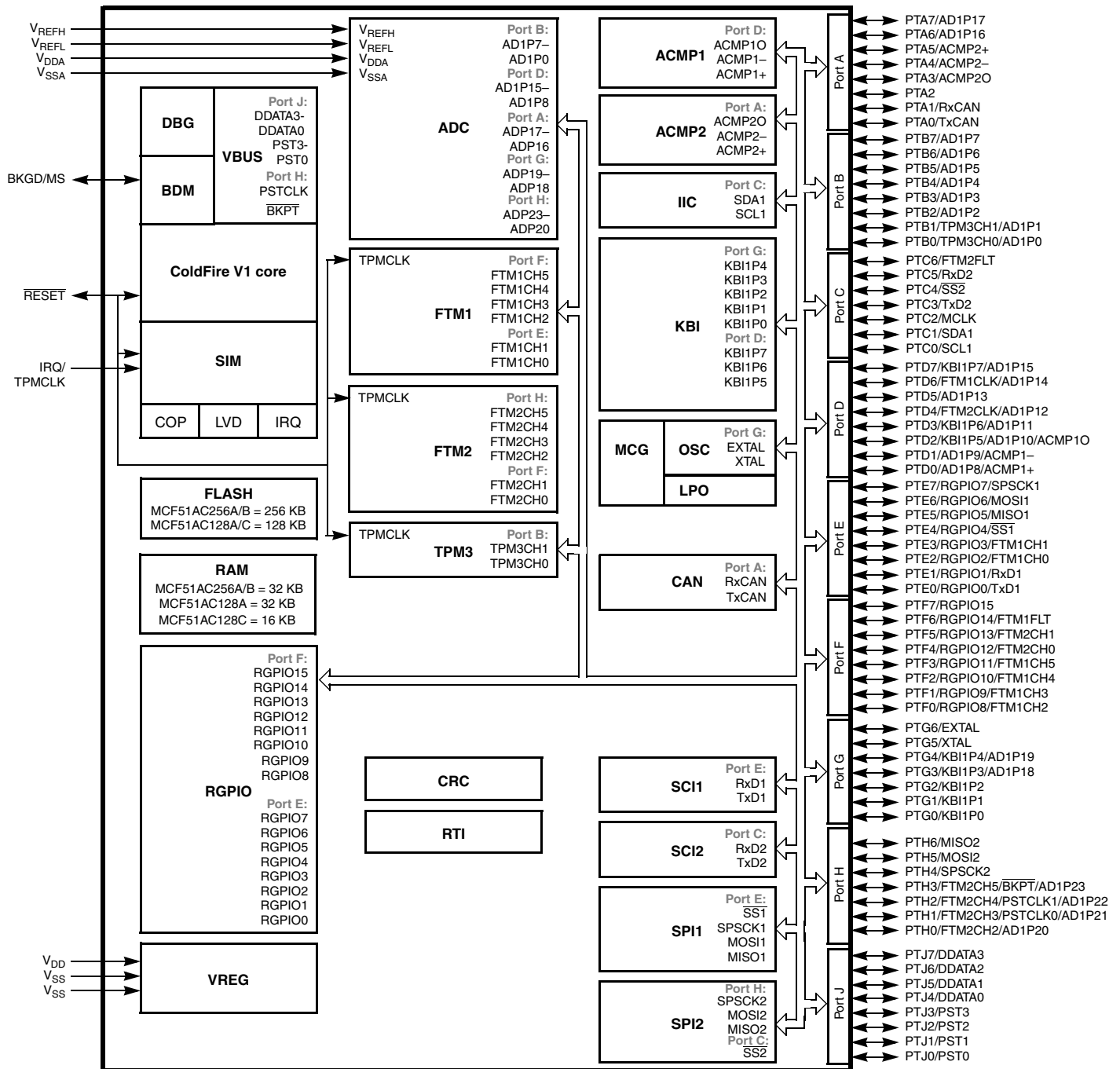


Figure 1. MCF51AC256 Series Block Diagram

1.3.1 Feature List

- 32-bit Version 1 ColdFire® central processor unit (CPU)
 - Up to 50.33 MHz at 2.7 V – 5.5 V
 - Provide 0.94 Dhrystone 2.1 DMIPS per MHz performance when running from internal RAM (0.76 DMIPS per MHz when running from flash)
 - Implements instruction set revision C (ISA_C)
- On-chip memory
 - Up to 256 KB flash memory read/program/erase over full operating voltage and temperature
 - Up to 32 KB static random access memory (SRAM)
 - Security circuitry to prevent unauthorized access to SRAM and flash contents
- Power-Saving Modes
 - Three low-power stop plus wait modes
 - Peripheral clock enable register can disable clocks to unused modules, reducing currents; allows clocks to remain enabled to specific peripherals in stop3 mode
- System protection features
 - Watchdog computer operating properly (COP) reset with options to run from independent LPO clock or bus clock
 - Low-voltage detection with reset or interrupt
 - Illegal opcode and illegal address detection with programmable reset or exception response
 - Flash block protection
- Debug support
 - Single-wire background debug interface
 - Real-time debug support, with 6 hardware breakpoints (4 PC, 1 address pair and 1 data) that can be configured into a 1- or 2-level trigger
 - On-chip trace buffer provides programmable start/stop recording conditions plus support for continuous or PC-profiling modes
 - Support for real-time program (and optional partial data) trace using the debug visibility bus
- V1 ColdFire interrupt controller (CF1_INTC)
 - Support of 40 peripheral I/O interrupt requests plus seven software (one per level) interrupt requests
 - Fixed association between interrupt request source and level plus priority, up to two requests can be remapped to the highest maskable level + priority
 - Unique vector number for each interrupt source
 - Support for service routine interrupt acknowledge (software IACK) read cycles for improved system performance
- Multipurpose clock generator (MCG)
 - Oscillator (XOSC); loop-control Pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
 - LPO clock as an optional independent clock source for COP and RTI
 - FLL/PLL controlled by internal or external reference

- Trimmable internal reference allows 0.2% resolution and 2% deviation
- Analog-to-digital converter (ADC)
 - 24 analog inputs with 12 bits resolution
 - Output formatted in 12-, 10- or 8-bit right-justified format
 - Single or continuous conversion (automatic return to idle after single conversion)
 - Operation in low-power modes for lower noise operation
 - Asynchronous clock source for lower noise operation
 - Automatic compare with interrupt for less-than, or greater-than or equal-to, programmable value
 - On-chip temperature sensor
- Flexible timer/pulse-width modulators (FTM)
 - 16-bit Free-running counter or a counter with initial and final value. The counting can be up and unsigned, up and signed, or up-down and unsigned
 - Up to 6 channels, and each channel can be configured for input capture, output compare or edge-aligned PWM mode, all channels can be configured for center-aligned PWM mode
 - Channels can operate as pairs with equal outputs, pairs with complimentary outputs or independent channels (with independent outputs)
 - Each pair of channels can be combined to generate a PWM signal (with independent control of both edges of PWM signal)
 - Deadtime insertion is available for each complementary pair
 - The load of the FTM registers which have write buffer can be synchronized; write protection for critical registers
 - Generation of the triggers to ADC (hardware trigger)
 - A fault input for global fault control
 - Backwards compatible with TPM
- Timer/pulse width modulator (TPM)
 - 16-bit free-running or modulo up/down count operation
 - Two channels, each channel may be input capture, output compare, or edge-aligned PWM
 - One interrupt per channel plus terminal count interrupt
- Cyclic redundancy check (CRC) generator
 - High speed hardware CRC generator circuit using 16-bit shift register
 - CRC16-CCITT compliancy with $x^{16} + x^{12} + x^5 + 1$ polynomial
 - Error detection for all single, double, odd, and most multi-bit errors
 - Programmable initial seed value
- Analog comparators (ACMP)
 - Full rail to rail supply operation
 - Selectable interrupt on rising edge, falling edge, or either rising or falling edges of comparator output
 - Option to compare to fixed internal bandgap reference voltage
 - Option to allow comparator output to be visible on a pin, ACMPxO

Table 3. Orderable Part Number Summary

MCF51AC256ACPUE	MCF51AC256 ColdFire Microcontroller with CAN	256 / 32	64 LQFP	–40°C to 85°C
MCF51AC256BCPUE	MCF51AC256 ColdFire Microcontroller without CAN	256 / 32	64 LQFP	–40°C to 85°C
MCF51AC256BCFGE	MCF51AC256 ColdFire Microcontroller without CAN	256/32	44 LQFP	–40°C to 85°C
MCF51AC128ACFUE	MCF51AC128 ColdFire Microcontroller with CAN	128 / 32	64 QFP	–40°C to 85°C
MCF51AC128CCFUE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	64 QFP	–40°C to 85°C
MCF51AC128ACLKE	MCF51AC128 ColdFire Microcontroller with CAN	128 / 32	80 LQFP	–40°C to 85°C
MCF51AC128CCLKE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	80 LQFP	–40°C to 85°C
MCF51AC128ACPUE	MCF51AC128 ColdFire Microcontroller with CAN	128 / 32	64 LQFP	–40°C to 85°C
MCF51AC128CCPUE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	64 LQFP	–40°C to 85°C
MCF51AC128CCFGE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	44 LQFP	–40°C to 85°C

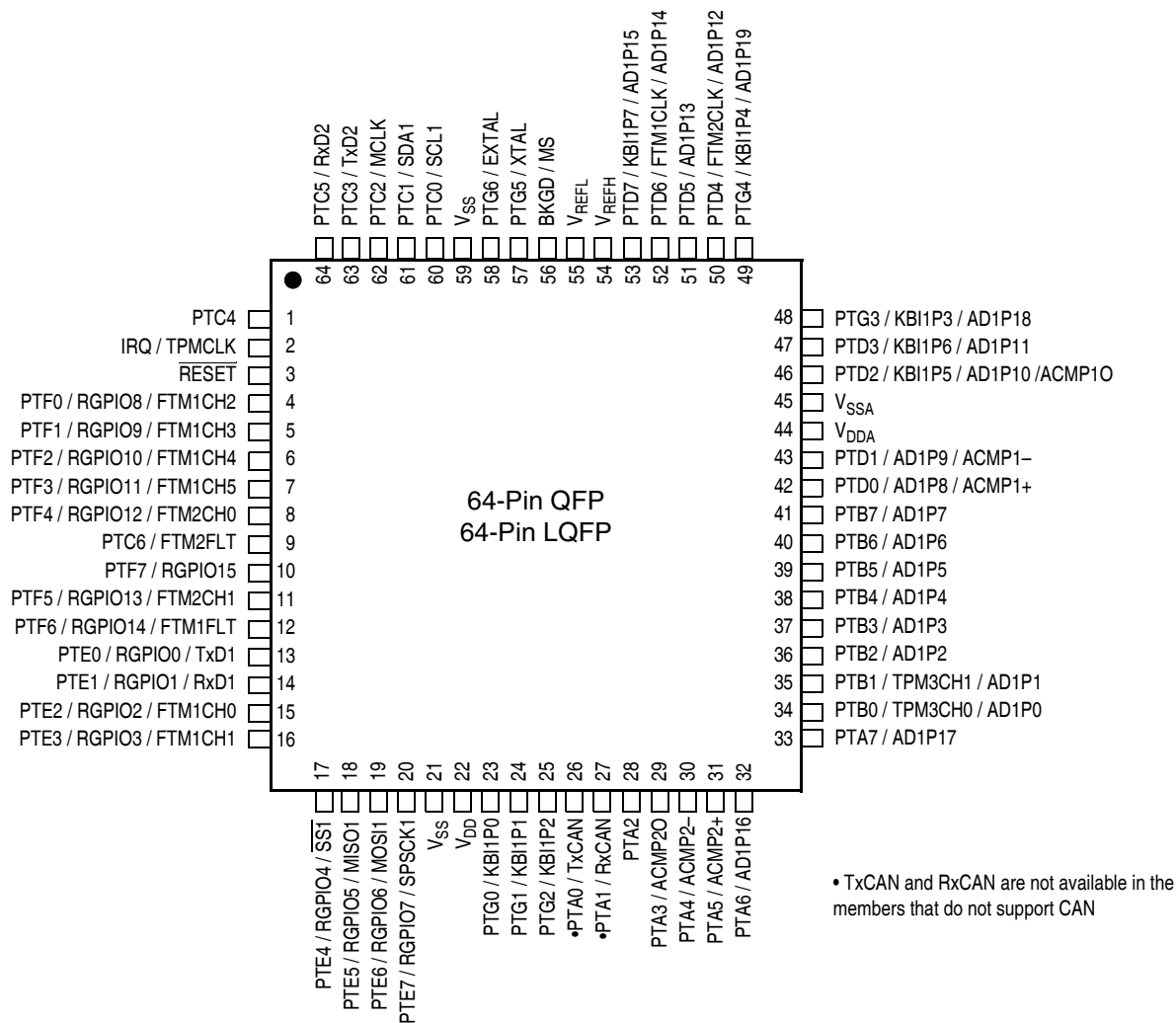
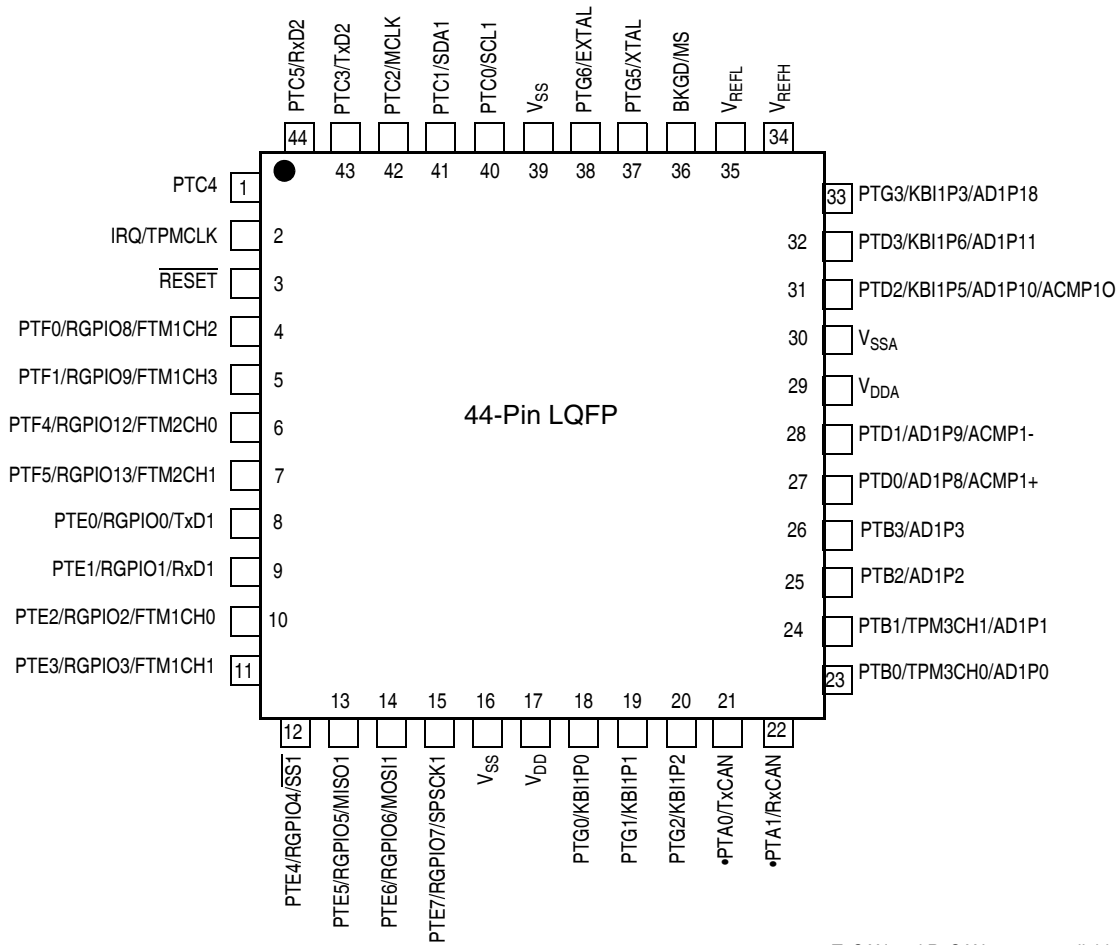


Figure 3. MCF51AC256 Series ColdFire Microcontroller 64-Pin QFP/LQFP

Figure 4 shows the pinout of the 44-pin LQFP.



• TxCAN and RxCAN are not available in the members that do not support CAN

Figure 4. MCF51AC256 Series ColdFire Microcontroller 44-Pin LQFP

Table 4 shows the package pin assignments.

Table 4. Pin Availability by Package Pin-Count

Pin Number			Lowest <-- Priority --> Highest			
80	64	44	Port Pin	Alt 1	Alt 2	Alt 3
1	1	1	PTC4	SS2		
2	2	2	IRQ	TPMCLK ¹		
3	3	3	RESET			
4	4	4	PTF0	RGPIO8	FTM1CH2	
5	5	5	PTF1	RGPIO9	FTM1CH3	
6	6	—	PTF2	RGPIO10	FTM1CH4	
7	7	—	PTF3	RGPIO11	FTM1CH5	

Table 4. Pin Availability by Package Pin-Count (continued)

Pin Number			Lowest <-- Priority --> Highest			
80	64	44	Port Pin	Alt 1	Alt 2	Alt 3
8	8	6	PTF4	RGPIO12	FTM2CH0	
9	9	—	PTC6	FTM2FLT		
10	10	—	PTF7	RGPIO15		
11	11	7	PTF5	RGPIO13	FTM2CH1	
12	12	—	PTF6	RGPIO14	FTM1FLT	
13	—	—	PTJ0	PST0		
14	—	—	PTJ1	PST1		
15	—	—	PTJ2	PST2		
16	—	—	PTJ3	PST3		
17	13	8	PTE0	RGPIO0	TxD1	
18	14	9	PTE1	RGPIO1	RxD1	
19	15	10	PTE2	RGPIO2	FTM1CH0	
20	16	11	PTE3	RGPIO3	FTM1CH1	
21	17	12	PTE4	RGPIO4	SS1	
22	18	13	PTE5	RGPIO5	MISO1	
23	19	14	PTE6	RGPIO6	MOSI1	
24	20	15	PTE7	RGPIO7	SPSCK1	
25	21	16	V _{SS}			
26	22	17	V _{DD}			
27	—	—	PTJ4	DDATA0		
28	—	—	PTJ5	DDATA1		
29	—	—	PTJ6	DDATA2		
30	—	—	PTJ7	DDATA3		
31	23	18	PTG0	KBI1P0		
32	24	19	PTG1	KBI1P1		
33	25	20	PTG2	KBI1P2		
34	26	21	PTA0	TxCAN ²		
35	27	22	PTA1	RxCAN ³		
36	28	—	PTA2			
37	29	—	PTA3	ACMP20		
38	30	—	PTA4	ACMP2–		
39	31	—	PTA5	ACMP2+		
40	32	—	PTA6	AD1P16		
41	33	—	PTA7	AD1P17		
42	—	—	PTH0	FTM2CH2	AD1P20	
43	—	—	PTH1	FTM2CH3	PSTCLK0	AD1P21
44	—	—	PTH2	FTM2CH4	PSTCLK1	AD1P22
45	—	—	PTH3	FTM2CH5	BKPT	AD1P23
46	34	23	PTB0	TPM3CH0	AD1P0	
47	35	24	PTB1	TPM3CH1	AD1P1	
48	36	25	PTB2	AD1P2		

2 Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the MCF51AC256 microcontroller, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. These specifications will, however, be met for production silicon. Finalized specifications will be published after complete characterization and device qualifications have been completed.

NOTE

The parameters specified in this data sheet supersede any values found in the module specifications.

2.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 5. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

2.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 6 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}).

Table 6. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	−0.3 to 5.8	V
Input voltage	V_{In}	−0.3 to $V_{DD} + 0.3$	V
Instantaneous maximum current Single pin limit (applies to all port pins) ^{1, 2, 3}	I_D	±25	mA
Maximum current into V_{DD}	I_{DD}	120	mA
Storage temperature	T_{stg}	−55 to 150	°C

¹ Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

² All functional non-supply pins are internally clamped to V_{SS} and V_{DD} .

³ Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD} , the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low which would reduce overall power consumption.

2.3 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and it is user-determined rather than being controlled by the MCU design. In order to take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 7. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	−40 to 105	°C
Maximum junction temperature	T_J	150	°C
Thermal resistance ^{1,2,3,4}			
80-pin LQFP			
1s		51	
2s2p		38	
64-pin LQFP			
1s		59	
2s2p	θ_{JA}	41	°C/W
64-pin QFP			
1s		50	
2s2p		36	
44-pin LQFP			
1s		67	
2s2p		45	

- ¹ Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance
- ² Junction to Ambient Natural Convection
- ³ 1s — Single layer board, one signal layer
- ⁴ 2s2p — Four layer board, 2 signal and 2 power layers

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \text{Eqn. 1}$$

where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power

$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} \ll P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273^\circ\text{C}) \quad \text{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273^\circ\text{C}) + \theta_{JA} \times (P_D)^2 \quad \text{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A . Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A .

2.4 Electrostatic Discharge (ESD) Protection Characteristics

Although damage from static discharge is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with CDF-AEC-Q00 Stress Test Qualification for Automotive Grade Integrated Circuits. (<http://www.aecouncil.com/>) This device was qualified to AEC-Q100 Rev E.

A device is considered to have failed if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete dc parametric and functional testing is performed per the

Table 10. DC Characteristics (continued)

Num	C	Parameter	Symbol	Min	Typical ¹	Max	Unit
3	P	Output low voltage — Low Drive (PTxDSn = 0) 5 V, I _{Load} = 4 mA 3 V, I _{Load} = 2 mA 5 V, I _{Load} = 2 mA 3 V, I _{Load} = 1 mA	V _{OL}	—	—	1.5 1.5 0.8 0.8	V
		Output low voltage — High Drive (PTxDSn = 1) 5 V, I _{Load} = 15 mA 3 V, I _{Load} = 8 mA 5 V, I _{Load} = 8 mA 3 V, I _{Load} = 4 mA		—	—	1.5 1.5 0.8 0.8	
4	C	Output high current — Max total I _{OH} for all ports 5V 3V	I _{OHT}	—	—	100 60	mA
5	C	Output low current — Max total I _{OL} for all ports 5 V 3 V	I _{OLT}	—	—	100 60	mA
6	P	Input high voltage; all digital inputs	V _{IH}	0.65 × V _{DD}	—	—	V
7	P	Input low voltage; all digital inputs	V _{IL}	—	—	0.35 × V _{DD}	V
8	D	Input hysteresis; all digital inputs	V _{hys}	0.06 × V _{DD}	—	—	mV
9	P	Input leakage current; input only pins ²	I _{in}	—	0.1	1	μA
10	P	High impedance (off-state) leakage current ²	I _{OZ}	—	0.1	1	μA
11	P	Internal pullup resistors ³	R _{PU}	20	45	65	kΩ
12	P	Internal pulldown resistors ⁴	R _{PD}	20	45	65	kΩ
13	C	Input capacitance; all non-supply pins	C _{In}	—	—	8	pF
14	P	POR rearm voltage	V _{POR}	0.9	1.4	2.0	V
15	D	POR rearm time	t _{POR}	10	—	—	μs
16	P	Low-voltage detection threshold — high range V _{DD} falling V _{DD} rising	V _{LVDH}	4.2 4.27	4.35 4.4	4.5 4.6	V
17	P	Low-voltage detection threshold — low range V _{DD} falling V _{DD} rising	V _{LVDL}	2.48 2.5	2.68 2.7	2.7 2.72	V
18	P	Low-voltage warning threshold — high range V _{DD} falling V _{DD} rising	V _{LVWH}	4.2 4.27	4.4 4.45	4.5 4.6	V
19	P	Low-voltage warning threshold low range V _{DD} falling V _{DD} rising	V _{LVWL}	2.48 2.5	2.68 2.7	2.7 2.72	V
20	T	Low-voltage inhibit reset/recover hysteresis 5 V 3 V	V _{hys}	—	100 60	—	mV
21	D	RAM retention voltage	V _{RAM}	—	0.6	1.0	V

Table 10. DC Characteristics (continued)

Num	C	Parameter	Symbol	Min	Typical ¹	Max	Unit
22	D	DC injection current ^{5 6 7 8} (single pin limit) $V_{IN} > V_{DD}$ $V_{IN} < V_{SS}$	I_{IC}	0 0	—	2 -0.2	mA
		DC injection current (Total MCU limit, includes sum of all stressed pins) $V_{IN} > V_{DD}$ $V_{IN} < V_{SS}$		0 0	—	25 -5	mA

¹ Typical values are based on characterization data at 25°C unless otherwise stated.

² Measured with $V_{IN} = V_{DD}$ or V_{SS} .

³ Measured with $V_{IN} = V_{SS}$.

⁴ Measured with $V_{IN} = V_{DD}$.

⁵ Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{IN} > V_{DD}$) is greater than I_{DD} , the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

⁶ All functional non-supply pins are internally clamped to V_{SS} and V_{DD} .

⁷ Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

⁸ The **RESET** pin does not have a clamp diode to V_{DD} . Do not drive this pin above V_{DD} .

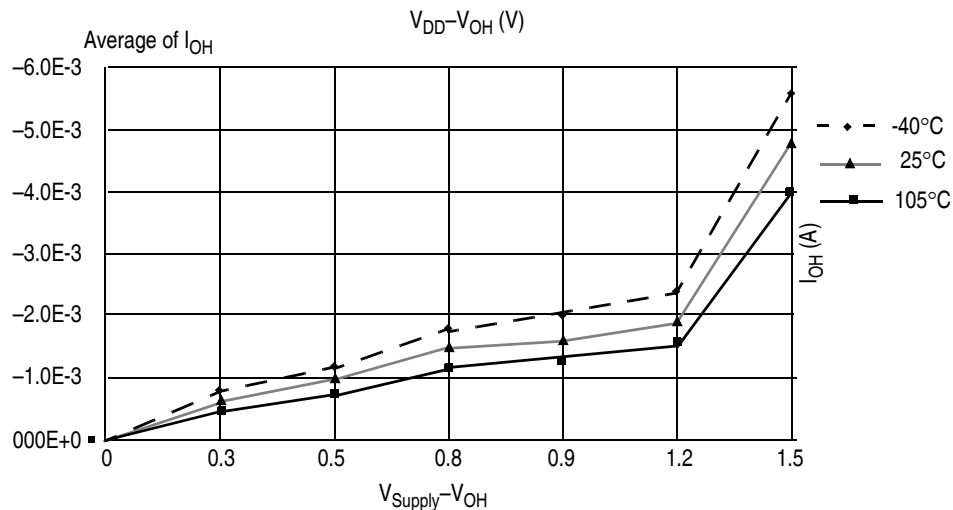


Figure 5. Typical I_{OH} vs. $V_{DD} - V_{OH}$ at $V_{DD} = 3$ V (Low Drive, $PTxDSn = 0$)

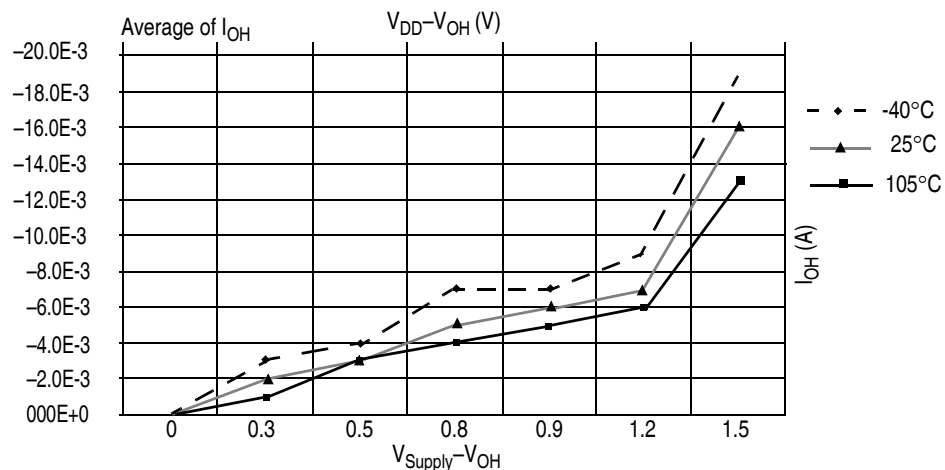


Figure 6. Typical I_{OH} vs. $V_{DD} - V_{OH}$ at $V_{DD} = 3$ V (High Drive, PTxDSn = 1)

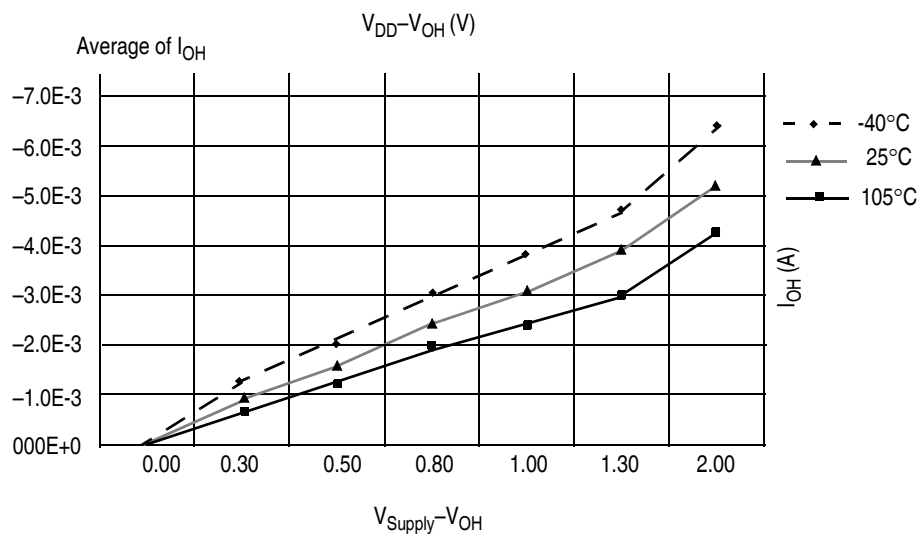


Figure 7. Typical I_{OH} vs. $V_{DD} - V_{OH}$ at $V_{DD} = 5$ V (Low Drive, PTxDSn = 0)

2.8 ADC Characteristics

Table 13. 5 Volt 12-bit ADC Operating Conditions

Num	C	Characteristic	Conditions	Symb	Min	Typical ¹	Max	Unit	Comment
1	D	Supply voltage	Absolute	V_{DDA}	2.7	—	5.5	V	
	D		Delta to V_{DD} ($V_{DD} - V_{DDA}$) ²	ΔV_{DDA}	−100	0	100	mV	
2	D	Ground voltage	Delta to V_{SS} ($V_{SS} - V_{SSA}$) ²	ΔV_{SSA}	−100	0	100	mV	
3	D	Reference voltage high		V_{REFH}	2.7	V_{DDA}	V_{DDA}	V	
4	D	Reference voltage low		V_{REFL}	V_{SSA}	V_{SSA}	V_{SSA}	V	
5	D	Input voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
6	C	Input capacitance		C_{ADIN}	—	4.5	5.5	pF	
7	C	Input resistance		R_{ADIN}	—	3	5	k Ω	
8	C	Analog source resistance	12-bit mode $f_{ADCK} > 4\text{MHz}$ $f_{ADCK} < 4\text{MHz}$	R_{AS}	— —	— —	2 5	k Ω	External to MCU
	C		10-bit mode $f_{ADCK} > 4\text{MHz}$ $f_{ADCK} < 4\text{MHz}$		— —	— —	5 10		
	C		8-bit mode (all valid f_{ADCK})		—	—	10		
9	D	ADC conversion clock frequency	High speed (ADLPC = 0)	f_{ADCK}	0.4	—	8.0	MHz	
	D		Low power (ADLPC = 1)		0.4	—	4.0		

¹ Typical values assume $V_{DDA} = 5.0\text{ V}$, Temp = 25 °C, $f_{ADCK} = 1.0\text{ MHz}$ unless otherwise stated. Typical values are for reference only and are not tested in production.

² DC potential difference.

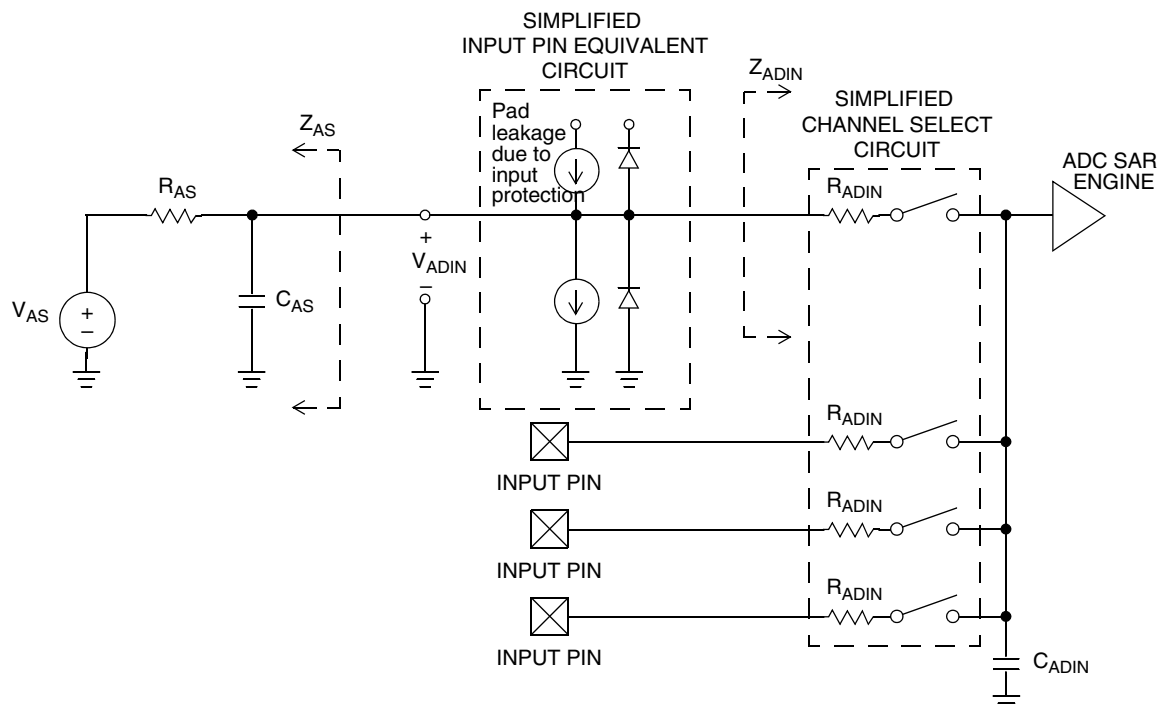


Figure 10. ADC Input Impedance Equivalency Diagram

Table 14. 5 Volt 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Num	C	Characteristic	Conditions	Symb	Min	Typical ¹	Max	Unit	Comment
1	T	Supply current ADLPC = 1 ADLSMP = 1 ADCO = 1		I_{DDA}	—	133	—	μA	
2	T	Supply current ADLPC = 1 ADLSM = 0 ADCO = 1		I_{DDA}	—	218	—	μA	
3	T	Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1		I_{DDA}	—	327	—	μA	
4	D	Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1		I_{DDA}	—	0.582	1	mA	
5	T	Supply current	Stop, reset, module off	I_{DDA}	—	0.011	1	μA	
6	P	ADC asynchronous clock source	High speed (ADLPC = 0)	f_{ADACK}	2	3.3	5	MHz	$t_{ADACK} = 1/f_{ADACK}$
			Low power (ADLPC = 1)		1.25	2	3.3		

³ Monotonicity and No-Missing-Codes guaranteed in 10-bit and 8-bit modes

⁴ Based on input pad leakage current. Refer to pad electricals.

2.9 External Oscillator (XOSC) Characteristics

Table 15. Oscillator Electrical Specifications (Temperature Range = –40 to 105 °C Ambient)

Num	C	Rating	Symbol	Min	Typical ¹	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1)					
		Low range (RANGE = 0)	f_{lo}	32	—	38.4	kHz
		High range (RANGE = 1) FEE or FBE mode ²	f_{hi-ll}	1	—	5	MHz
		High range (RANGE = 1) PEE or PBE mode ³	f_{hi-pll}	1	—	16	MHz
		High range (RANGE = 1, HGO = 1) BLPE mode	f_{hi-hgo}	1	—	16	MHz
		High range (RANGE = 1, HGO = 0) BLPE mode	f_{hi-lp}	1	—	8	MHz
2	—	Load capacitors	C_1 C_2	See crystal or resonator manufacturer's recommendation.			
3	—	Feedback resistor	R_F		10		MΩ
		Low range (32 kHz to 38.4 kHz) High range (1 MHz to 16 MHz)			1		
4	—	Series resistor	R_S				kΩ
		Low range, low gain (RANGE = 0, HGO = 0)		—	0	—	
		Low range, high gain (RANGE = 0, HGO = 1)		—	100	—	
		High range, low gain (RANGE = 1, HGO = 0)		—	0	—	
		High range, high gain (RANGE = 1, HGO = 1)		—	0	0	
		≥ 8 MHz		—	0	0	
5	T	Crystal start-up time ⁴					ms
		Low range, low gain (RANGE = 0, HGO = 0)	$t_{CSTL-LP}$	—	200	—	
		Low range, high gain (RANGE = 0, HGO = 1)	$t_{CSTL-HGO}$	—	400	—	
		High range, low gain (RANGE = 1, HGO = 0) ⁵	$t_{CSTH-LP}$	—	5	—	
		High range, high gain (RANGE = 1, HGO = 1) ⁵	$t_{CSTH-HGO}$	—	15	—	
6	T	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1)					MHz
		FEE or FBE mode ²	f_{extal}	0.03125	—	5	
		PEE or PBE mode ³		1	—	16	
		BLPE mode		0	—	40	

¹ Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.

² When MCG is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.

³ When MCG is configured for PEE or PBE mode, input clock source must be divisible using RDIV to within the range of 1 MHz to 2 MHz.

⁴ This parameter is characterized and not tested on each device. Proper PC board layout procedures must be followed to achieve specifications.

⁵ 4 MHz crystal

2.11.1 Control Timing

Table 17. Control Timing

Num	C	Parameter	Symbol	Min	Typical ¹	Max	Unit
1	D	Bus frequency ($t_{cyc} = 1/f_{Bus}$)	f_{Bus}	dc	—	24	MHz
2	D	Internal low-power oscillator period	t_{LPO}	800	—	1500	μs
3	D	External reset pulse width ² ($t_{cyc} = 1/f_{Self_reset}$)	t_{extrst}	100	—	—	ns
4	D	Reset low drive	t_{rstdrv}	$66 \times t_{cyc}$	—	—	ns
5	D	Active background debug mode latch setup time	t_{MSSU}	500	—	—	ns
6	D	Active background debug mode latch hold time	t_{MSH}	100	—	—	ns
7	D	IRQ pulse width Asynchronous path ² Synchronous path ³	t_{ILIH}, t_{IHIL}	100 $1.5 \times t_{cyc}$	—	—	ns
8	D	KBIPx pulse width Asynchronous path ² Synchronous path ³	t_{ILIH}, t_{IHIL}	100 $1.5 \times t_{cyc}$	—	—	ns
9	D	Port rise and fall time (load = 50 pF) ⁴ Slew rate control disabled (PTxSE = 0), Low Drive Slew rate control enabled (PTxSE = 1), Low Drive Slew rate control disabled (PTxSE = 0), Low Drive Slew rate control enabled (PTxSE = 1), Low Drive	t_{Rise}, t_{Fall}	— — — —	11 35 40 75	—	ns

¹ Typical values are based on characterization data at $V_{DD} = 5.0 V$, 25 °C unless otherwise stated.

² This is the shortest pulse that is guaranteed to be recognized as a reset pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

³ This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

⁴ Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40 °C to 105 °C.

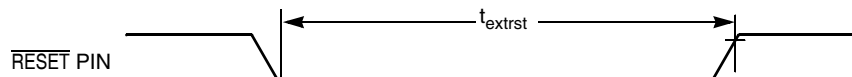


Figure 11. Reset Timing

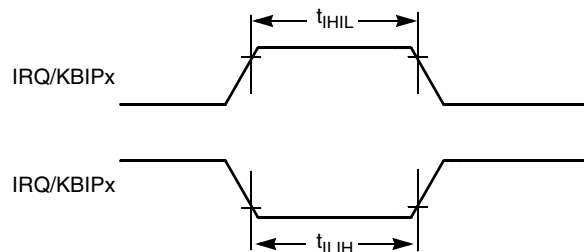


Figure 12. IRQ/KBIPx Timing

2.11.2 Timer (TPM/FTM) Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 18. TPM/FTM Input Timing

NUM	C	Function	Symbol	Min	Max	Unit
1	—	External clock frequency	f_{TPMext}	DC	$f_{\text{Bus}}/4$	MHz
2	—	External clock period	t_{TPMext}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

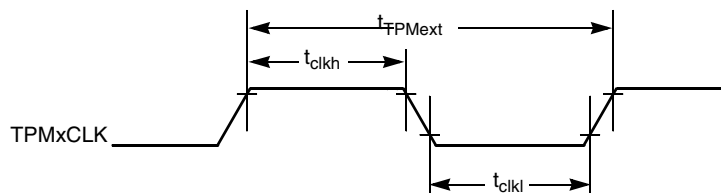


Figure 13. Timer External Clock

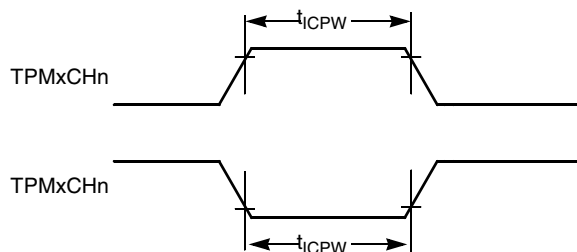


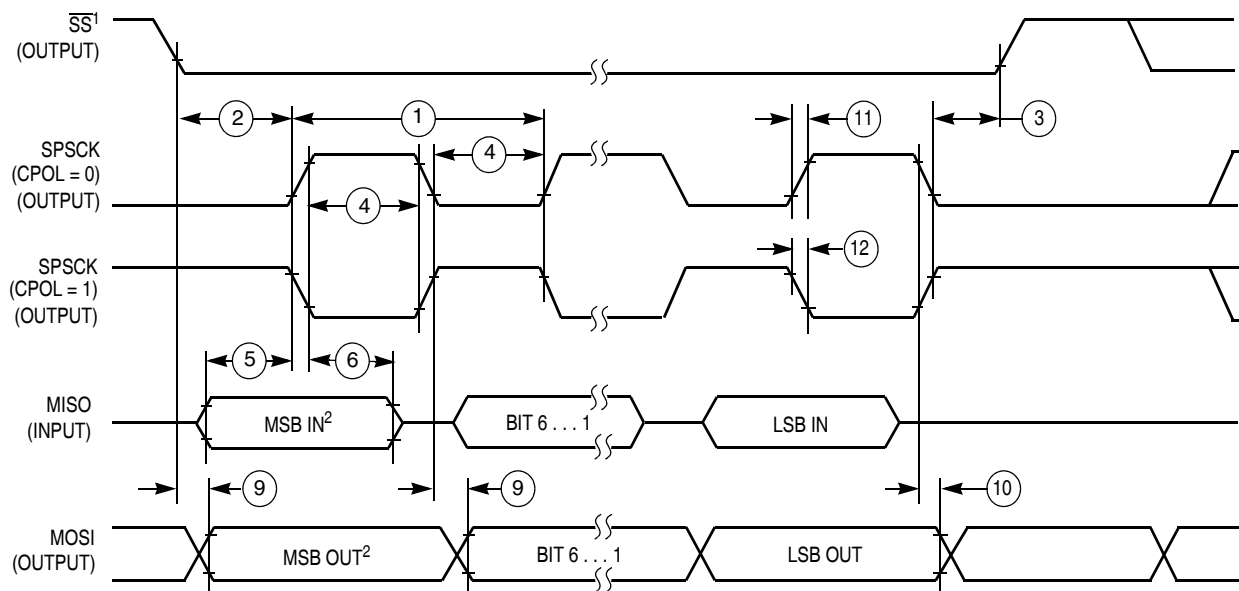
Figure 14. Timer Input Capture Pulse

2.11.3 MSCAN

Table 19. MSCAN Wake-Up Pulse Characteristics

Num	C	Parameter	Symbol	Min	Typical ¹	Max	Unit
1	D	MSCAN wake-up dominant pulse filtered	t_{WUP}	—	—	2	μs
2	D	MSCAN wake-up dominant pulse pass	t_{WUP}	5	—	5	μs

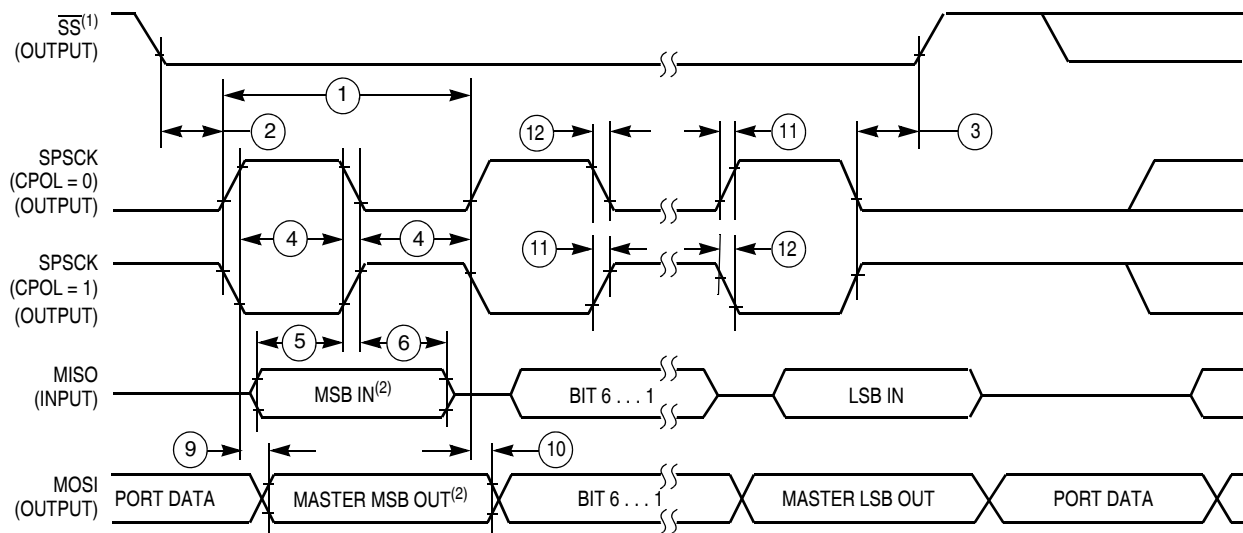
¹ Typical values are based on characterization data at $V_{\text{DD}} = 5.0 \text{ V}$, 25°C unless otherwise stated.



NOTES:

1. \overline{SS} output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 15. SPI Master Timing (CPHA = 0)



NOTES:

1. \overline{SS} output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 16. SPI Master Timing (CPHA = 1)

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