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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M210
Core Size	16/32-Bit
Speed	33MHz
Connectivity	EBI/EMI, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	72
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mmc2107cfcaf33

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1.3 Features

Features of the MMC2107 include:

- M•CORE M210 integer processor:
  - 32-bit reduced instruction set computer (RISC) architecture
  - Low power and high performance
- OnCE™ debug support
- On-chip 128-Kbyte FLASH:
  - Motorola's one transistor, CDR MoneT(1) FLASH bit cell
  - Page mode (2111) read access
  - External V_{PP} required for programming
  - 16-K block size
- On-chip, 8-Kbyte static random-access memory (SRAM):
  - One clock per access (including bytes, half-words, and words)
  - Byte, half-word (16 bits), and word (32 bits) read/write accesses
  - Standby power supply support
- Serial peripheral interface (SPI):
  - Master mode and slave mode
  - Wired-OR mode
  - Slave select output
  - Mode fault error flag with CPU interrupt capability
  - Double-buffered operation
  - Serial clock with programmable polarity and phase
  - Control of SPI operation during wait mode
  - Reduced drive control

™OnCE is a trademark of Motorola, Inc.
1. CDR MoneT designates the Motorola one-transistor bitcell.

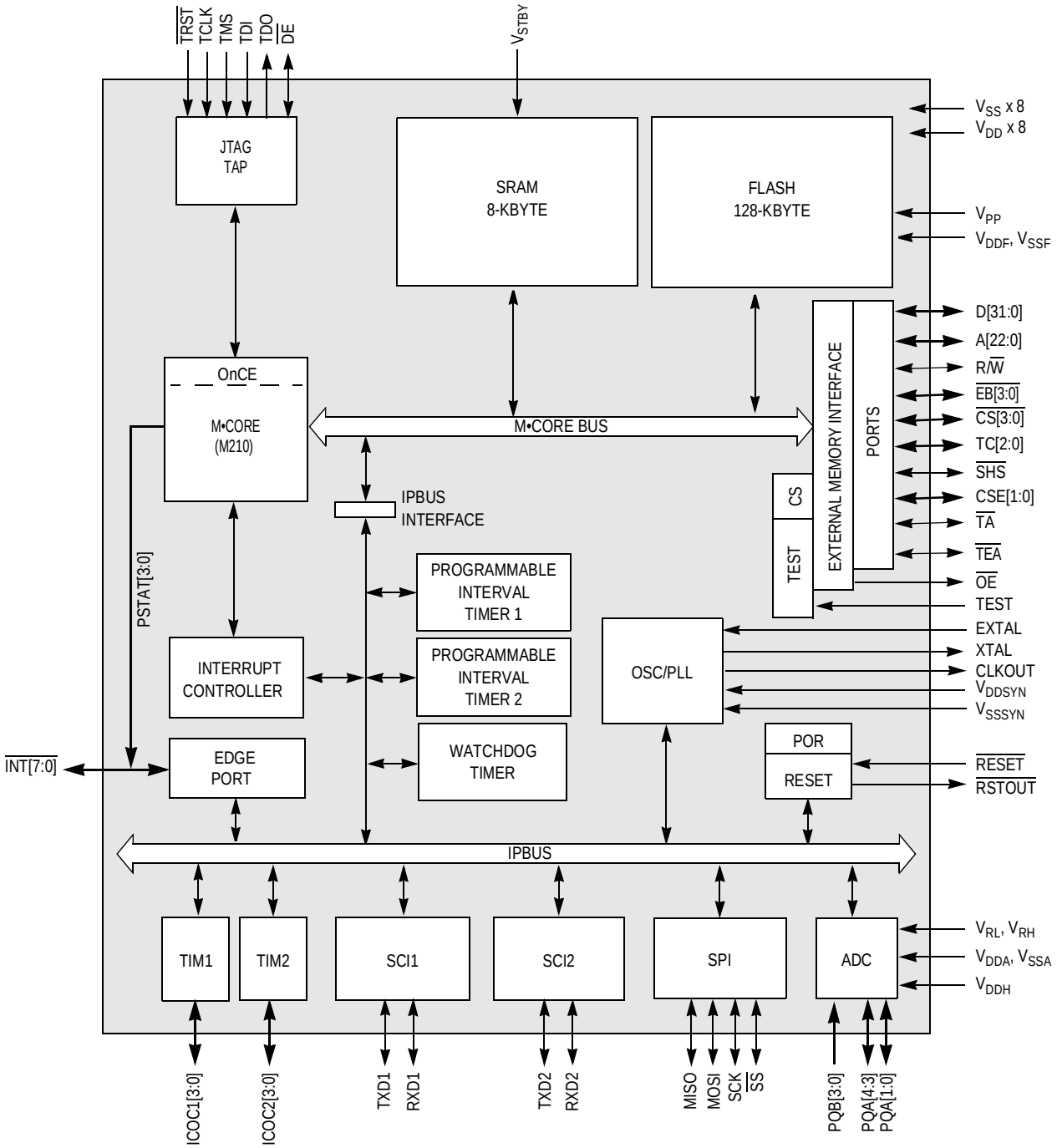

Figure 1-1. Block Diagram

Address	Register Name		Bit Number							
			Bit 7	6	5	4	3	2	1	Bit 0
0x00cb_0002	SPI Baud Rate Register (SPIBR) See page 379.	Read:	0	SPPR6	SPPR5	SPPR4	0	SPR2	SPR1	SPR0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00cb_0003	SPI Status Register (SPISR) See page 381.	Read:	SPIF	WCOL	0	MODF	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00cb_0004	Reserved		Writes have no effect, reads return 0s, and the access terminates without a transfer error exception.							
			Bit 7	6	5	4	3	2	1	Bit 0
0x00cb_0005	SPI Data Register (SPIDR) See page 382.	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00cb_0006	SPI Pullup and Reduced Drive Register (SPIPURD) See page 383.	Read:	0	0	RSVD5	RDPSP	0	0	RSVD1	PUPSP
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00cb_0007	SPI Port Data Register (SPIPORT) See page 384.	Read:	RSVD7	RSVD6	RSVD5	RSVD4	PORTSP3	PORTSP2	PORTSP1	PORTSP0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00cb_0008	SPI Port Data Direction Register (SPIDDR) See page 385.	Read:	RSVD7	RSVD6	RSVD5	RSVD4	DDRSP3	DDRSP2	DDRSP1	DDRSP0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00cb_0009 ↓ 0x00cb_000f	Reserved		Writes have no effect, reads return 0s, and the access terminates without a transfer error exception.							

P = Current pin state U = Unaffected = Writes have no effect and the access terminates without a transfer error exception.

Figure 2-2. Register Summary (Sheet 25 of 34)

NVR — Negative Voltage Range Select Bit

The read-always NVR bit modulates the negative pump output to select the negative voltage range in program and erase modes as shown in **Table 9-2**. NVR is writable when the HVS bit is clear but has no effect when the GDB bit is clear.

1 = Negative voltage low range
0 = Negative voltage high range

Table 9-2. Negative Voltage Modulation

PAWS[2:0]	NVR = 0	NVR = 1
100	–6 V	–2 V
101	–7 V	–3 V
110	–8 V	–4 V
111	–9 V	–5 V
0XX	Reserved(1)	

1. When PAWS[2] = 0 and PAWS[1:0] have no effect.

PAWS[2:0] — Pulse Amplitude/Width Select Field

The read-always PAWS[2:0] field selects the pulse drain amplitude and width for program or erase operations. PAWS[2:0] is writable when the HVS bit is clear. PAWS[2] must be set for all program and erase operations. If GDB = 1, the gate/source voltage applied during program/erase is determined by PAWS[1:0] and NVR and shown in **Table 9-2**.

NOTE: *The program pulse time is equal to the value selected by the pulse width timing control. When SES = 1, write to SCLKR[2:0], CLKPE[1:0], and CLKPM[6:0] only when PAWS[2] = 1. Do not write to PAWS[2:0] during high-voltage operations.*

RSVD6 — Reserved

Reserved for factory test and must remain clear at all times

Table 10-8. Stop Mode Operation (Sheet 3 of 3)

MODE In	LOCEN	LOCRE	LOLRE	PLL	OSC	FWKUP	Expected PLL Action at Stop	PLL Action During Stop	MODE Out	LOCKS	LOCK	LOCS	Comments
NRM	1	1	0	On	On	1	—	—	NRM	‘LK	1	‘LC	
								Lose clock	RESET	—	—	—	Reset immediately
								Lose lock	Unstable NRM	0	0–>1	‘LC	
								Lose lock, regain	NRM	0	1	‘LC	
NRM	1	1	1	On	On	X	—	—	NRM	‘LK	1	‘LC	
								Lose clock or lock	RESET	—	—	—	Reset immediately
REF	1	0	0	X	X	X	—	—	REF	0	X	1	
								Lose reference clock	Stuck	—	—	—	
SCM	1	0	0	Off	X	0	PLL disabled	Regain SCM	SCM	0	0	1	Wakeup without lock
SCM	1	0	0	Off	X	1	PLL disabled	Regain SCM	SCM	0	0	1	
SCM	1	0	0	On	On	0	—	—	SCM	0	0	1	Wakeup without lock
								Lose reference clock	SCM				
SCM	1	0	0	On	On	1	—	—	SCM	0	0	1	
								Lose reference clock	SCM				

PLL = PLL enabled during STOP mode. PLL = On when STPMD[1:0] = 00 or 01
OSC = OSC enabled during STOP mode. OSC = On when STPMD[1:0] = 00, 01, or 10
MODES
NRM = normal PLL crystal clock reference or normal PLL external reference or PLL 1:1 mode. During PLL 1:1 or normal external reference mode, the oscillator is never enabled. Therefore, during these modes, refer to the OSC = On case regardless of STPMD values.
EXT = external clock mode
REF = PLL reference mode due to losing PLL clock or lock from NRM mode
SCM = PLL self-clocked mode due to losing reference clock from NRM mode
RESET = immediate reset
LOCKS
‘LK = expecting previous value of LOCKS before entering stop
0–>‘LK = current value is 0 until lock is regained which then will be the previous value before entering stop
0–> = current value is 0 until lock is regained but lock is never expected to regain
LOCS
‘LC = expecting previous value of LOCS before entering stop
1–>‘LC = current value is 1 until clock is regained which then will be the previous value before entering stop
1–> = current value is 1 until clock is regained but CLK is never expected to regain

10.8.4.2 Loss-of-Clock Reset

When a loss-of-clock condition is recognized, reset is asserted if the LOCRE bit in SYNCR is set. The LOCS bit in SYNSR is cleared after reset. Therefore, the LOC bit must be read in RSR to determine that a loss of clock condition occurred. LOCRE has no effect in external clock mode.

To exit reset in PLL mode, the reference must be present, and the PLL must acquire lock.

11.5.2 Port Digital I/O Timing

Input data on all pins configured as digital I/O is synchronized to the rising edge of CLKOUT. See **Figure 11-8**.

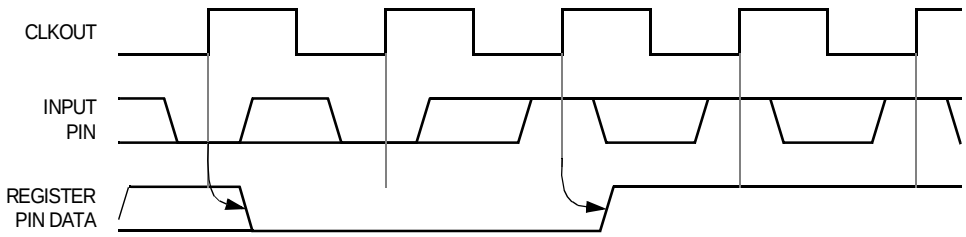

Figure 11-8. Digital Input Timing

Data written to PORTx of any pin configured as a digital output is immediately driven to its respective pin. See **Figure 11-9**.

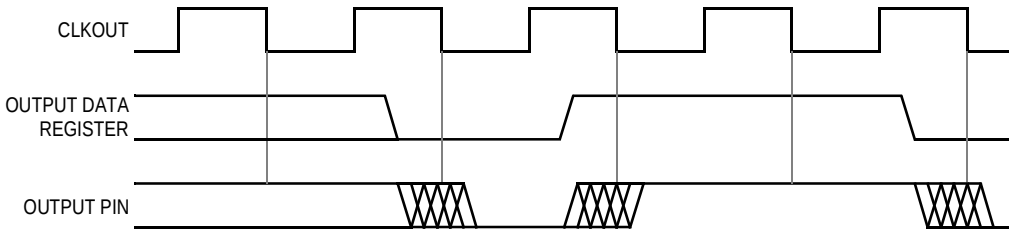

Figure 11-9. Digital Output Timing

11.6 Interrupts

The ports module does not generate interrupt requests.

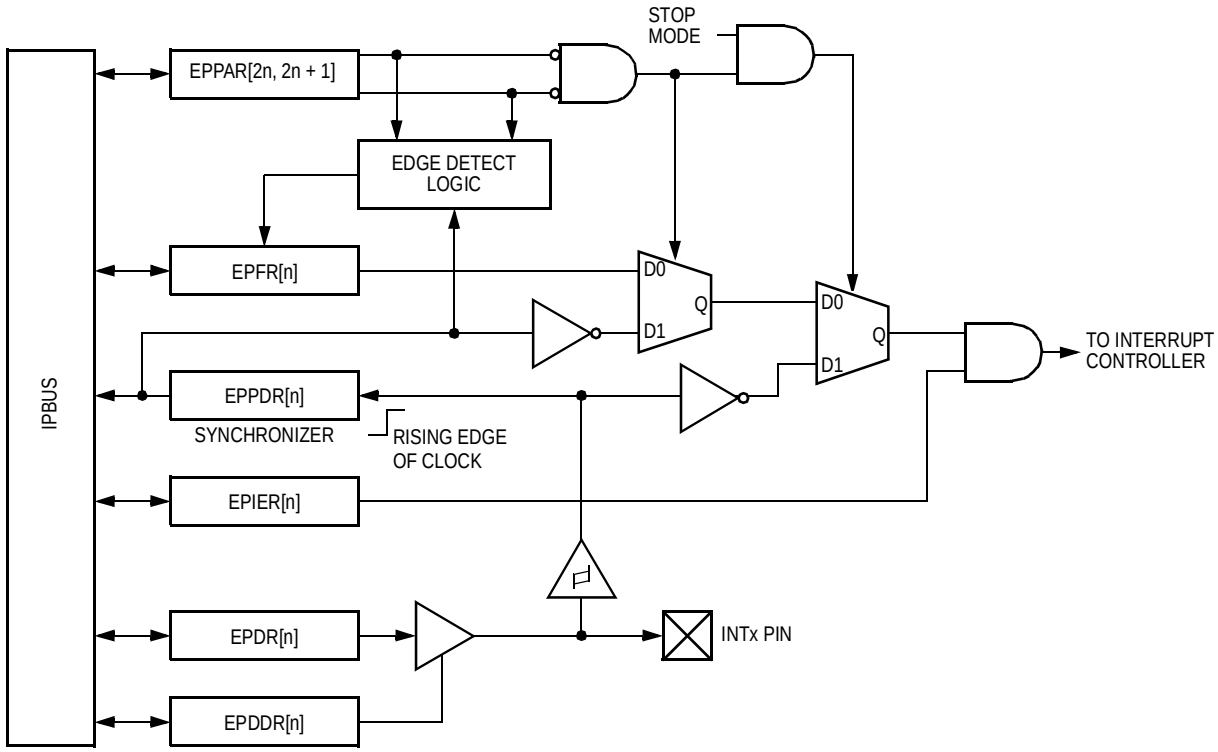

Figure 12-1. EPORT Block Diagram

12.3 Low-Power Mode Operation

This subsection describes the operation of the EPORT module in low-power modes.

12.3.1 Wait and Doze Modes

In wait and doze modes, the EPORT module continues to operate normally and may be configured to exit the low-power modes by generating an interrupt request on either a selected edge or a low level on an external pin.

14.6.2.2 PIT Modulus Register

The 16-bit read/write PIT modulus register (PMR) contains the timer modulus value for loading into the PIT counter when the count reaches 0x0000 and the RLD bit is set.

When the OVW bit is set, PMR is transparent, and the value written to PMR is immediately loaded into the PIT counter. The prescaler counter is reset anytime a new value is loaded into the PIT counter and also during reset. Reading the PMR returns the value written in the modulus latch. Reset initializes PMR to 0xFFFF.

Address: PIT1 — 0x00c8_0002 and 0x00c8_0003
PIT2 — 0x00c9_0002 and 0x00c9_0003

	Bit 15	14	13	12	11	10	9	Bit 8
Read: Write:	PM15	PM14	PM13	PM12	PM11	PM10	PM9	PM8
Reset:	1	1	1	1	1	1	1	1

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PM7	PM6	PM5	PM4	PM3	PM2	PM1	PM0
Reset:	1	1	1	1	1	1	1	1

Figure 14-3. PIT Modulus Register (PMR)

16.7.6 SCI Data Registers

Address: SCI1 — 0x00cc_0006
SCI2 — 0x00cd_0006

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	R8	T8	0	0	0	0	0	0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 16-8. SCI Data Register High (SCIDRH)

Address: SCI1 — 0x00cc_0007
SCI2 — 0x00cd_0007

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	R7	R6	R5	R4	R3	R2	R1	R0
Write:	T7	T6	T5	T4	T3	T2	T1	T0
Reset:	0	0	0	0	0	0	0	0

Figure 16-9. SCI Data Register Low (SCIDRL)

Read: Anytime

Write: Anytime; writing to R8 has no effect

R8 — Receive Bit 8

The R8 bit is the ninth received data bit when using the 9-bit data format (M = 1). Reset clears R8.

T8 — Transmit Bit 8

The T8 bit is the ninth transmitted data bit when using the 9-bit data format (M = 1). Reset clears T8.

R[7:0] — Receive Bits [7:0]

The R[7:0] bits are receive bits [7:0] when using the 9-bit or 8-bit data format. Reset clears R[7:0].

T[7:0] — Transmit Bits [7:0]

The T[7:0] bits are transmit bits [7:0] when using the 9-bit or 8-bit data format. Reset clears T[7:0].

16.11.3 Break Frames

Setting the SBK bit in SCICR2 loads the transmit shift register with a break frame. A break frame contains all logic 0s and has no start, stop, or parity bit. Break frame length depends on the M bit in the SCICR1 register. As long as SBK is set, the SCI continuously loads break frames into the transmit shift register. After SBK is clear, the transmit shift register finishes transmitting the last break frame and then transmits at least one logic 1. The automatic logic 1 at the end of a break frame guarantees the recognition of the next start bit.

The SCI recognizes a break frame when a start bit is followed by eight or nine 0 data bits and a 0 where the stop bit should be. Receiving a break frame has these effects on SCI registers:

- Sets the FE flag
- Sets the RDRF flag
- Clears the SCIDRH and SCIDRL
- May set the OR flag, NF flag, PE flag, or the RAF flag

16.11.4 Idle Frames

An idle frame contains all logic 1s and has no start, stop, or parity bit. Idle frame length depends on the M bit in the SCICR1 register. The preamble is a synchronizing idle frame that begins the first transmission after writing the TE bit from 0 to 1.

If the TE bit is cleared during a transmission, the TXD pin becomes idle after completion of the transmission in progress. Clearing and then setting the TE bit during a transmission queues an idle frame to be sent after the frame currently being transmitted.

NOTE: *When queueing an idle frame, return the TE bit to logic 1 before the stop bit of the current frame shifts out to the TXD pin. Setting TE after the stop bit appears on TXD causes data previously written to SCIDRH and SCIDRL to be lost toggle TE for a queued idle frame while the TDRE flag is set and immediately before writing new data to SCIDRH and SCIDRL.*

16.12.6 Receiver Wakeup

So that the SCI can ignore transmissions intended only for other devices in multiple-receiver systems, the receiver can be put into a standby state. Setting the RWU bit in SCICR2 puts the receiver into a standby state during which receiver interrupts are disabled.

The transmitting device can address messages to selected receivers by including addressing information in the initial frame or frames of each message.

The WAKE bit in SCICR1 determines how the SCI is brought out of the standby state to process an incoming message. The WAKE bit enables either idle line wakeup or address mark wakeup.

16.12.6.1 Idle Input Line Wakeup (WAKE = 0)

When WAKE = 0, an idle condition on the RXD pin clears the RWU bit and wakes up the receiver. The initial frame or frames of every message contain addressing information. All receivers evaluate the addressing information, and receivers for which the message is addressed process the frames that follow. Any receiver for which a message is not addressed can set its RWU bit and return to the standby state. The RWU bit remains set and the receiver remains on standby until another idle frame appears on the RXD pin.

Idle line wakeup requires that messages be separated by at least one idle frame and that no message contains idle frames.

The idle frame that wakes up the receiver does not set the IDLE flag or the RDRF flag.

The ILT bit in SCICR1 determines whether the receiver begins counting logic 1s as idle frame bits after the start bit or after the stop bit.

16.12.6.2 Address Mark Wakeup (WAKE = 1)

When WAKE = 1, an address mark clears the RWU bit and wakes up the receiver. An address mark is a 1 in the most significant data bit position. The receiver interprets the data as address data. When using address mark wakeup, the MSB of all non-address data must be 0. User code must compare the address data to the receiver’s address and, if the

addresses match, the receiver processes the frames that follow. If the addresses do not match, user code must put the receiver back to sleep by setting the RWU bit. The RWU bit remains set and the receiver remains on standby until another address frame appears on the RXD pin.

The address mark clears the RWU bit before the stop bit is received and sets the RDRF flag.

Address mark wakeup allows messages to contain idle frames but requires that the most significant byte (MSB) be reserved for address data.

NOTE: *With the WAKE bit clear, setting the RWU bit after the RXD pin has been idle can cause the receiver to wake up immediately.*

16.13 Single-Wire Operation

Normally, the SCI uses the TXD pin for transmitting and the RXD pin for receiving (LOOPS = 0, RSRC = X). In single-wire mode, the RXD pin is disconnected from the SCI and is available as a general-purpose I/O pin. The SCI uses the TXD pin for both receiving and transmitting.

In single-wire mode (LOOPS = 1, RXRC = 1), setting the data direction bit for the TXD pin configures TXD as the output for transmitted data. Clearing the data direction bit configures TXD as the input for received data.

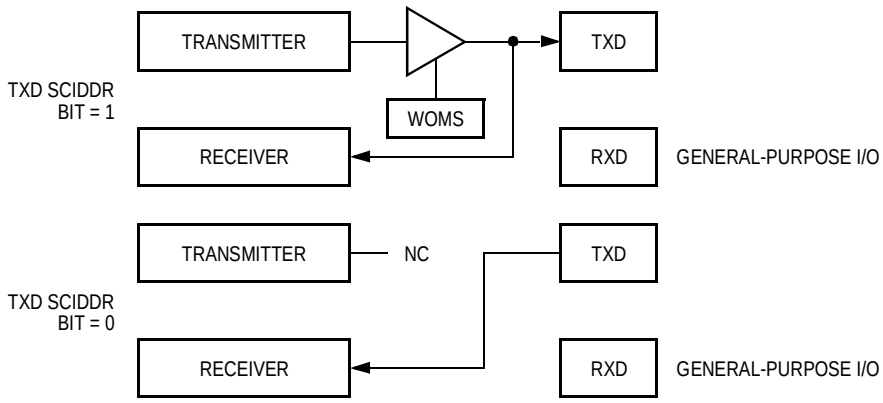

Figure 16-25. Single-Wire Operation (LOOPS = 1, RSRC = 1)

Section 17. Serial Peripheral Interface Module (SPI)

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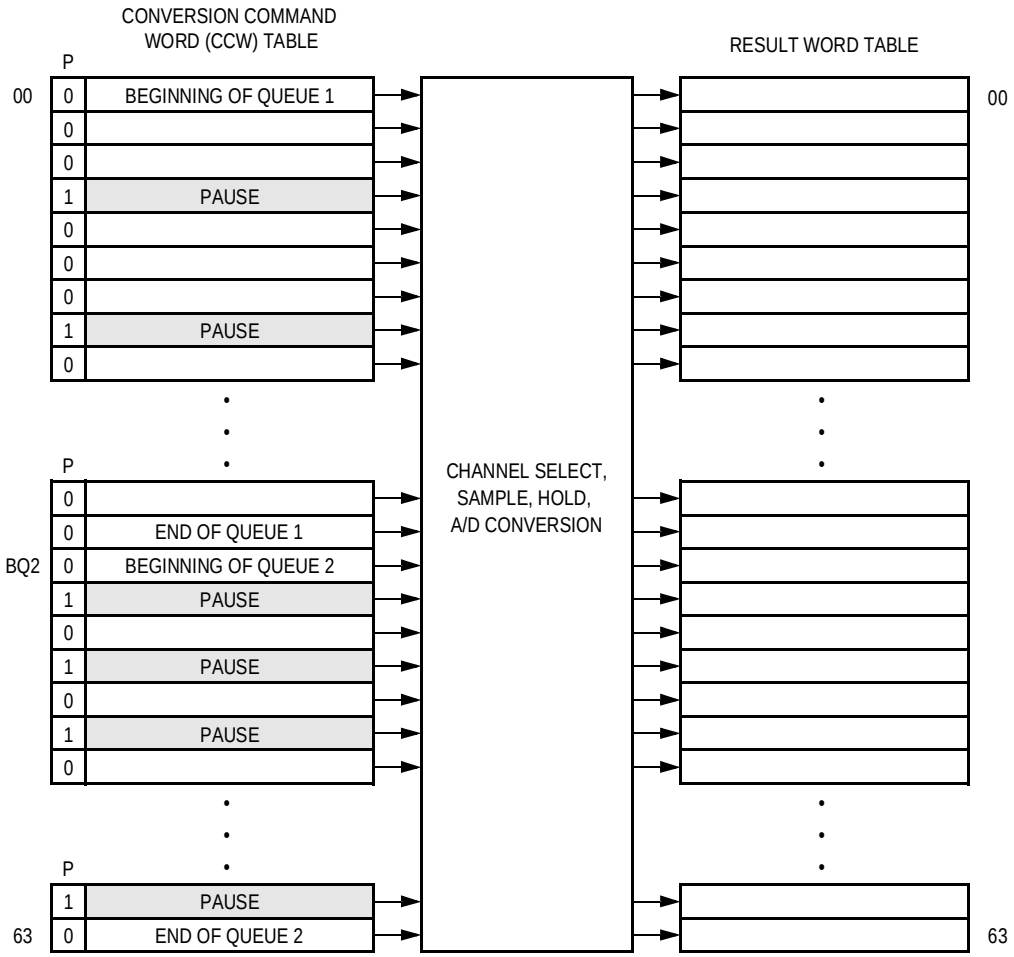

Figure 18-22. QADC Queue Operation with Pause

The queue operating mode selected for queue 1 determines what type of trigger event causes the execution of each of the subqueues within queue 1. Similarly, the queue operating mode for queue 2 determines the type of trigger event required to execute each of the subqueues within queue 2.

For example, when the external trigger rising edge continuous-scan mode is selected for queue 1, and there are six subqueues within queue 1, a separate rising edge is required on the external trigger pin after every pause to begin the execution of each subqueue (refer to **Figure 18-22**).

The choice of single-scan or continuous-scan applies to the full queue, and is not applied to each subqueue. Once a subqueue is initiated, each

Situation S3 (**Figure 18-25**) shows that when the pause feature is in use, the trigger overrun error status bit is set the same way, and that queue execution continues unchanged.

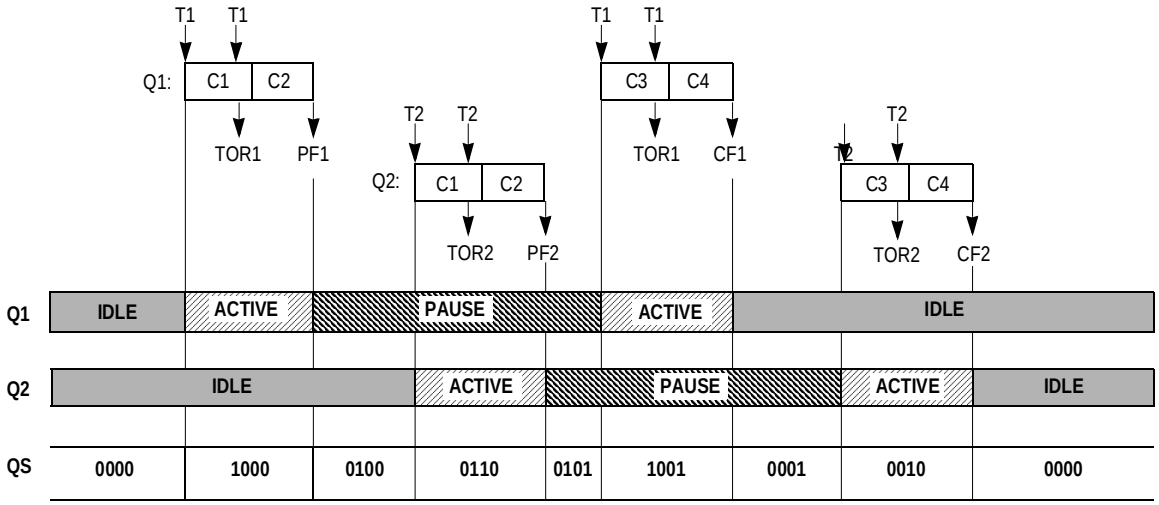

Figure 18-25. CCW Priority Situation 3

The next two situations consider trigger events that occur for the lower priority queue 2, while queue 1 is actively being serviced.

Situation S4 (**Figure 18-26**) shows that a queue 2 trigger event that is recognized while queue 1 is active is saved, and as soon as queue 1 is finished, queue 2 servicing begins.

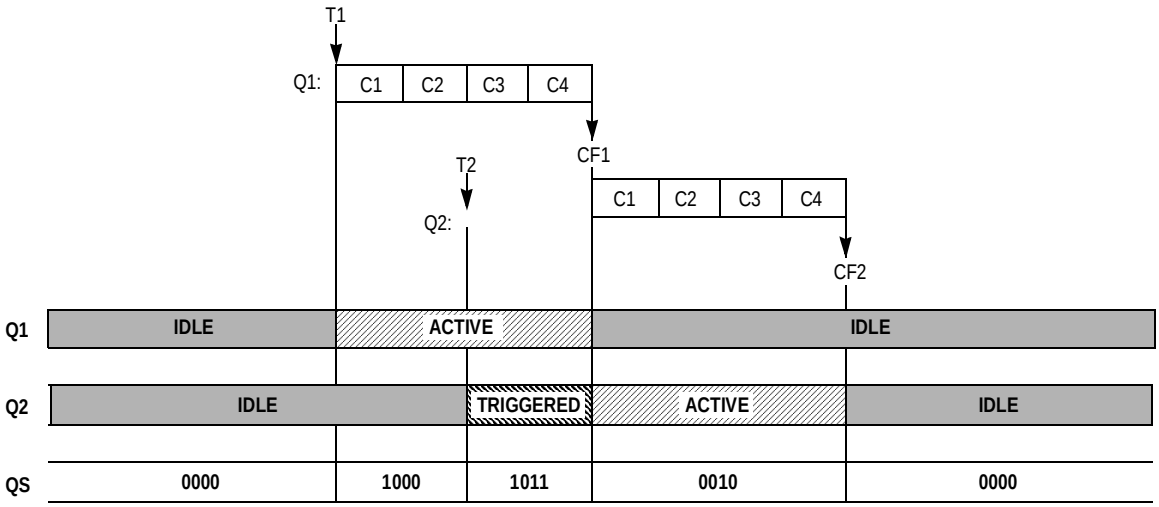

Figure 18-26. CCW Priority Situation 4

19.7.1 Read Cycles

During a read cycle, the EBI receives data from an external memory or peripheral device. During external read cycles, the $\overline{OE}$ pin is asserted regardless of operand size. See **Figure 19-1**.

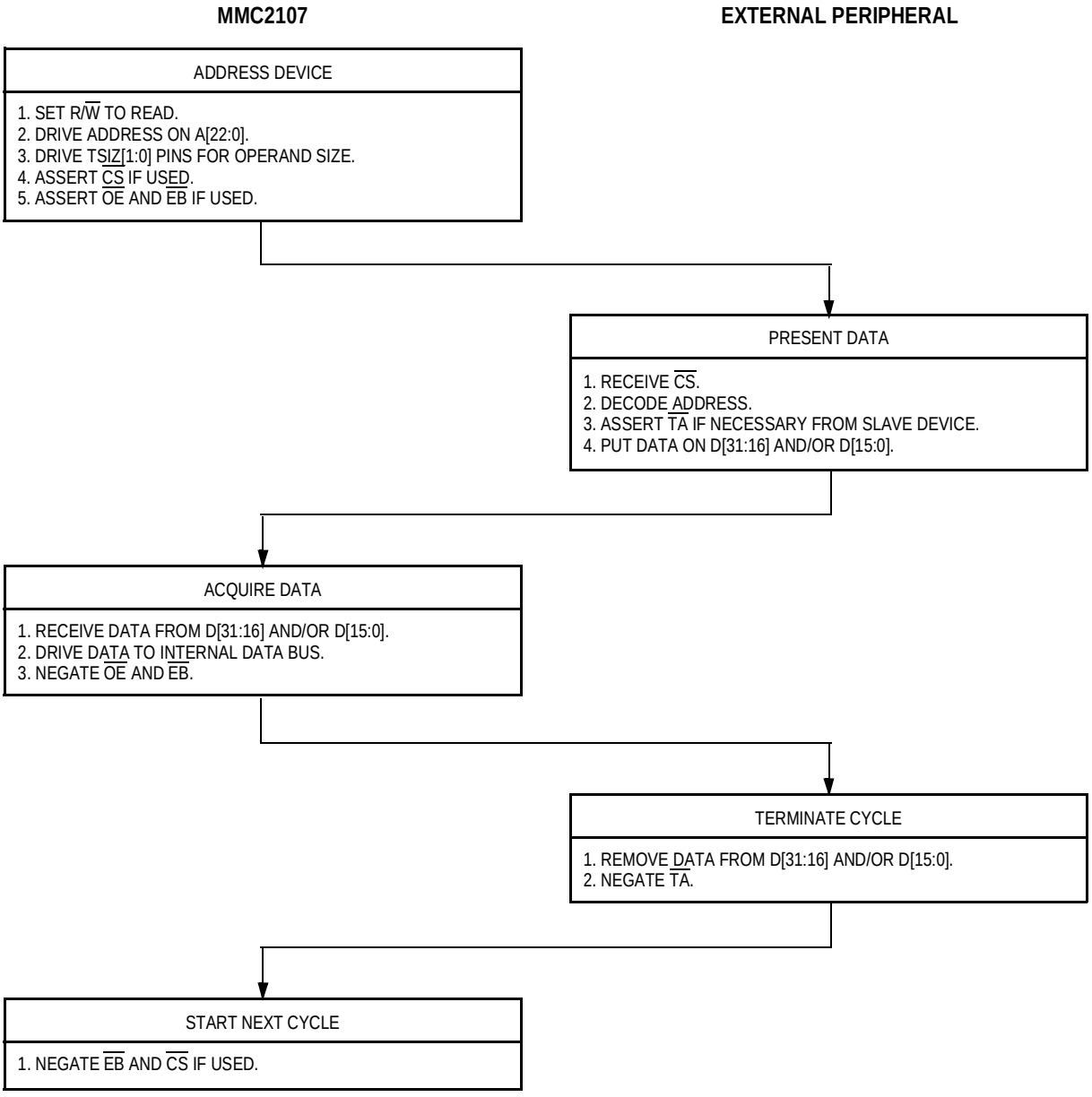

Figure 19-1. Read Cycle Flowchart

20.6.2 Registers

The chip programming model consists of four chip select control registers (CSCR0–CSCR3), one for each chip select (CS[3:0]). CSCR0–CSCR3 are read/write always and define the conditions for asserting the chip select signals.

All the chip select control registers are the same except for the reset states of the CSEN and PS bits in CSCR0 and the CSEN bit in CSCR1. This allows CS0 to be enabled at reset with either a 16-bit or 32-bit port size for selecting an external boot device and allows CS1 to be used to emulate internal memory.

Address: 0x00c2_0000 and 0x00c2_0001

	Bit 15	14	13	12	11	10	9	Bit 8
Read: / Write:	SO	RO	PS	WWS	WE	WS2	WS1	WS0
Reset:	0	0	See note	1	1	1	1	1
	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	0	TAEN	CSEN
Write:								
Reset:	0	0	0	0	0	0	1	See note

= Writes have no effect and the access terminates without a transfer error exception.

Note: Reset state determined during reset configuration.

Figure 20-2. Chip Select Control Register 0 (CSCR0)

21.14.3.2 CPU Debug Request (DBGRQ)

The DBGRQ signal is asserted by the OnCE control logic to request the CPU to enter the debug state. It may be asserted for a number of different conditions. Assertion of this signal causes the CPU to finish the current instruction being executed, save the instruction pipeline information, enter debug mode, and wait for further commands. Asserting DBGRQ causes the device to exit stop, doze, or wait mode.

21.14.3.3 CPU Debug Acknowledge (DBGACK)

The CPU asserts the DBGACK signal upon entering the debug state. This signal is part of the handshake mechanism between the OnCE control logic and the CPU.

21.14.3.4 CPU Breakpoint Request (BRKRQ)

The BRKRQ signal is asserted by the OnCE control logic to signal that a breakpoint condition has occurred for the current CPU bus access.

21.14.3.5 CPU Address, Attributes (ADDR, ATTR)

The CPU address and attribute information may be used in the memory breakpoint logic to qualify memory breakpoints with access address and cycle type information.

21.14.3.6 CPU Status (PSTAT)

The trace logic uses the PSTAT signals to qualify trace count decrements with specific CPU activity.

21.14.3.7 OnCE Debug Output (DEBUG)

The DEBUG signal is used to indicate to on-chip resources that a debug session is in progress. Peripherals and other units may use this signal to modify normal operation for the duration of a debug session. This may involve the CPU executing a sequence of instructions solely for the purpose of visibility/system control. These instructions are not part of the normal instruction stream that the CPU would have executed had it not been placed in debug mode.

22.13 SPI Timing Characteristics

Table 22-13. SPI Timing Characteristics
(V_{DD} = 2.7 to 3.6 V, V_{SS} = 0 V, T_A = T_L to T_H)

No.	Function	Symbol	Min	Max	Unit
1	Operating frequency Master Slave	f_{op}	DC DC	1/2 x f_{sys} 1/2 x f_{sys}	System frequency
2	SCK period Master Slave	t_{SCK}	2 2	2048 —	t_{cyc} t_{cyc}
3	Enable lead time Master Slave	t_{Lead}	1/2 1	— —	t_{sck} t_{cyc}
4	Enable lag time Master Slave	t_{Lag}	1/2 1	— —	t_{sck} t_{cyc}
5	Clock (SCK) high or low time Master Slave	t_{WSCK}	t_{cyc} – 30 t_{cyc} – 30	1024 t_{cyc} —	ns
6	Data setup time, inputs Master Slave	t_{SU}	25 25	— —	ns
7	Data hold time, inputs Master Slave	t_{High}	0 25	— —	ns
8	Slave access time	t_A	—	1	t_{cyc}
9	Slave MISO disable time	t_{DIS}	—	1	t_{cyc}
10	Data valid after SCK edge Master Slave	t_V	— —	25 25	ns
11	Data hold time, outputs Master Slave	t_{Hold}	0 0	— —	ns
12	Rise time Input Output	t_{RI} t_{RO}	— —	t_{cyc} – 25 25	ns
13	Fall time Input Output	t_{FI} t_{FO}	— —	t_{cyc} – 25 25	ns