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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M210
Core Size	16/32-Bit
Speed	33MHz
Connectivity	EBI/EMI, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	72
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mmc2107cfcpu33

  - Queue pointers indicate current location for each queue
  - Automated queue modes initiated by:
    - External edge trigger and gated trigger
    - Periodic/interval timer, within queued analog-to-digital converter (QADC) module {queue1 and queue2}
    - Software command
  - Single-scan or continuous-scan of queues
  - Output data readable in three formats:
    - Right-justified unsigned
    - Left-justified signed
    - Left-justified unsigned
  - Unused analog channels can be used as digital input/output (I/O)
  - Minimum pin set configuration implemented

- Interrupt controller:
  - Up to 40 interrupt sources
  - 32 unique programmable priority levels for each interrupt source
  - Independent enable/disable of pending interrupts based on priority level
  - Select normal or fast interrupt request for each priority level
  - Fast interrupt requests always have priority over normal interrupts.
  - Ability to mask interrupts at and below a defined priority level
  - Ability to select between autovectored or vectored interrupt requests
  - Vectored interrupts generated based on priority level
  - Ability to generate a separate vector number for normal and fast interrupts
  - Ability for software to self-schedule interrupts
  - Software visibility of pending interrupts and interrupt signals to core
  - Asynchronous operation to support wakeup from low-power modes

System Memory Map

Address	Register Name		Bit Number							
			Bit 15	14	13	12	11	10	9	Bit 8
0x00ca_0012 0x00ca_0013	QADC Status Register 1 (QASR1) See page 436.	Read:	0	0	CWPQ15	CWPQ14	CWPQ13	CWPQ12	CWPQ11	CWPQ10
		Write:								
		Reset:	0	0	1	1	1	1	1	1
			Bit 7	6	5	4	3	2	1	Bit 0
		Read:	0	0	CWPQ25	CWPQ24	CWPQ23	CWPQ22	CWPQ21	CWPQ20
		Write:								
		Reset:	0	0	1	1	1	1	1	1
			Bit 7	6	5	4	3	2	1	Bit 0
0x00ca_0014 ↓ 0x00ca_01ff	Reserved		Writes have no effect, reads return 0s, and the access terminates without a transfer error exception.							
			Bit 15	14	13	12	11	10	9	Bit 8
0x00ca_0200 0x00ca_027e	Conversion Command Word Register (CCW) See page 437.	Read:	0	0	0	0	0	0	P	BYP
		Write:								
		Reset:	0	0	0	0	0	0	U	U
			Bit 7	6	5	4	3	2	1	Bit 0
		Read:	IST1	IST0	CHAN5	CHAN4	CHAN3	CHAN2	CHAN1	CHAN0
		Write:								
		Reset:	U	U	U	U	U	U	U	U
			Bit 15	14	13	12	11	10	9	Bit 8
0x00ca_0280 0x00ca_02fe	Right-Justified Unsigned Result Register (RJURR) See page 441.	Read:	0	0	0	0	0	0	RESULT	
		Write:								
		Reset:	0	0	0	0	0	0		
			Bit 7	6	5	4	3	2	1	Bit 0
		Read:	RESULT							
		Write:								
		Reset:								

P = Current pin state U = Unaffected = Writes have no effect and the access terminates without a transfer error exception.

Figure 2-2. Register Summary (Sheet 23 of 34)

3.4.1 Master Mode

In master mode, the internal central processor unit (CPU) can access external memories and peripherals. Full master mode functionality requires the bonding out of the optional pins. The external bus consists of a 32-bit data bus and 23 address lines. Available bus control signals include R/$\overline{W}$, TC[2:0], TSIZ[1:0], $\overline{TA}$, $\overline{TEA}$, $\overline{OE}$, and $\overline{EB}$[3:0]. Up to four chip selects can be programmed to select and control external devices and to provide bus cycle termination. When interfacing to 16-bit ports, the ports C and D pins and $\overline{EB}$[3:2] can be configured as general-purpose input/output (I/O).

3.4.2 Single-Chip Mode

In single-chip mode, all memory is internal to the chip. External bus pins are configured as digital I/O.

3.4.3 Emulation Mode

Emulation mode supports external port replacement logic. All ports are emulated and all primary pin functions are enabled. Since the full external bus must be visible to support the external port replacement logic, the emulation mode pin configuration resembles master mode. Full emulation mode functionality requires bonding out the optional pins. Emulation mode chip selects are provided to give additional information about the bus cycle. Also, the signal $\overline{SHS}$ is provided as a strobe for capturing addresses and data during show cycles.

3.4.4 Factory Access Slave Test (FAST) Mode

FAST mode is for factory test only.

3.7 Memory Map and Registers

This subsection provides a description of the memory map and registers.

3.7.1 Programming Model

The CCM programming model consists of these registers:

- The chip configuration register (CCR) controls the main chip configuration.
- The reset configuration register (RCON) indicates the default chip configuration.
- The chip identification register (CIR) contains a unique part number.
- The chip test register (CTR) contains chip-specific test functions.

Some control register bits are implemented as write-once bits. These bits are always readable, but once the bit has been written, additional writes have no effect, except during debug mode and test operations.

Some write-once bits and test bits can be read and written while in debug mode or test mode. When debug or test mode is exited, the chip configuration module resumes operation based on the current register values. If a write to a write-once register bit occurs while in debug or test mode, the register bit remains writable on exit from debug or test mode. Table 3-2 shows the accessibility of write-once bits.

Table 3-2. Write-Once Bits Read/Write Accessibility

Configuration	Read/Write Access
All configurations	Read-always
Debug operation (all modes)	Write-always
Test operation (all modes)	Write-always
Master mode	Write-once
Single-chip mode	Write-once
FAST mode	Write-once
Emulation mode	Write-once

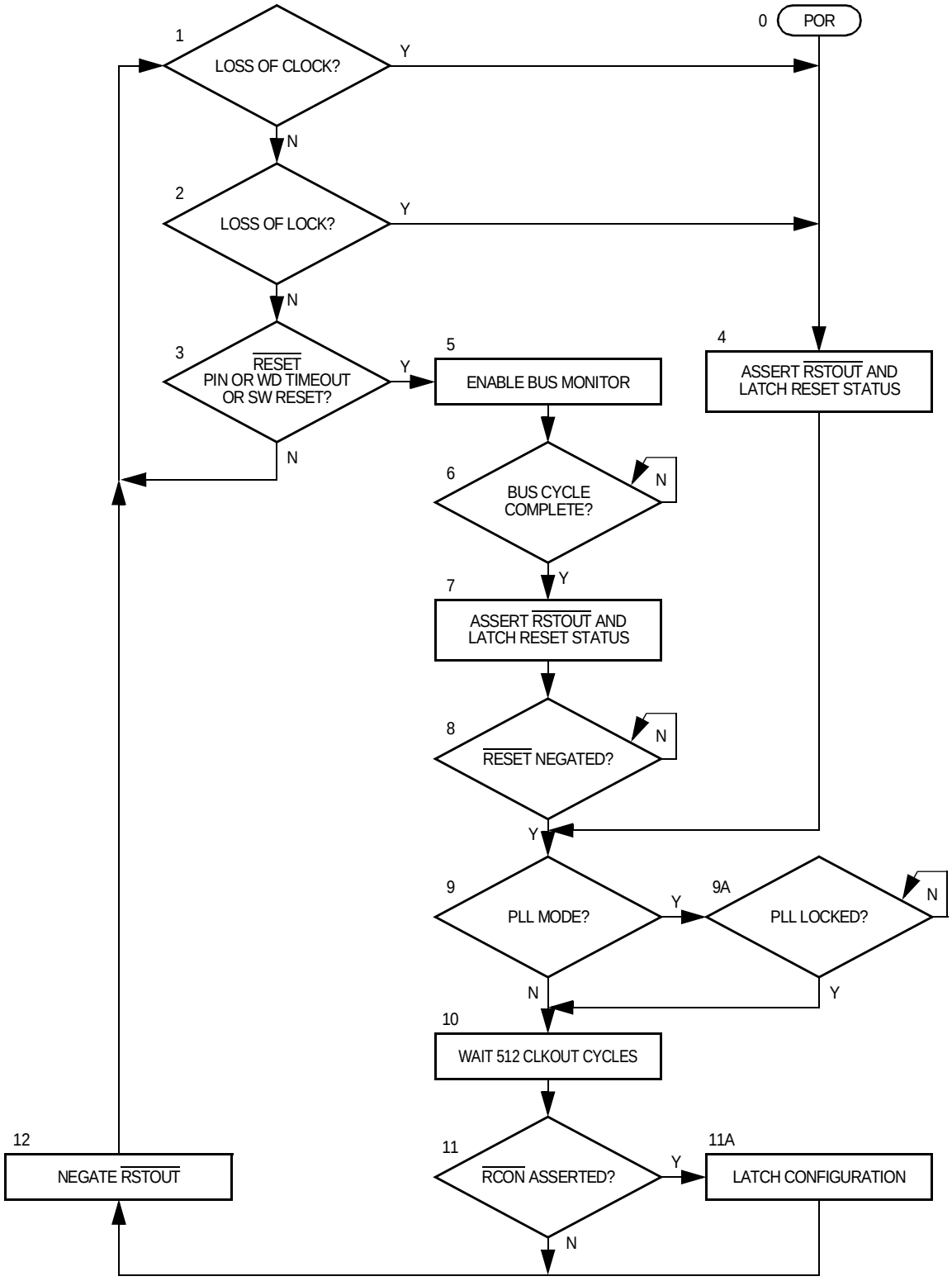

Figure 5-5. Reset Control Flow

7.7.2.4 Interrupt Pending Register

The 32-bit, read-only interrupt pending register (IPR) reflects any currently pending interrupts which are assigned to each priority level. Writes to this register have no effect and are terminated normally.

Address: 0x00c5_000c through 0x00c5_000f

	Bit 31	30	29	28	27	26	25	Bit 24
Read:	IP31	IP30	IP29	IP28	IP27	IP26	IP25	IP24
Write:								
Reset:	0	0	0	0	0	0	0	0

	Bit 23	22	21	20	19	18	17	Bit 16
Read:	IP23	IP22	IP21	IP20	IP19	IP18	IP17	IP16
Write:								
Reset:	0	0	0	0	0	0	0	0

	Bit 15	14	13	12	11	10	9	Bit 8
Read:	IP15	IP14	IP13	IP12	IP11	IP10	IP9	IP8
Write:								
Reset:	0	0	0	0	0	0	0	0

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 7-6. Interrupt Pending Register (IPR)

IP[31:0] — Interrupt Pending Field

A read-only IPx bit is set when at least one interrupt request is asserted at priority level x. Reset clears IP[31:0].

1 = At least one interrupt request asserted at priority level x
0 = All interrupt requests at level x negated

CAUTION: *Never stop or alter the system clock frequency during a program or erase operation. Changing the clock frequency during program or erase results in inaccurate pulse widths and variations in the charge pump output.*

The default reset state of SCLKR[2:0] is 000, giving a clock scaling of 1, and the program or erase pulse is not terminated until EHV is cleared by a software write.

CLKPE[1:0] — Clock Period Exponent Field

The read/write CLKPE[1:0] field selects the clock period exponent for program/erase pulse timing. The second term of the timing control is the clock multiplier, 2^N. The program pulse number (pulse), clock period exponent bits (CLKPE[1:0]), and ERASE define the exponent in the 2^N multiply of the clock period. The exponent, N, is defined by the equation:

$$N = 5 + CLKPE[1:0] + [(ERASE) \times 10]$$

All of the exponents are shown in **Table 9-5**.

NOTE: *The CLKPE[1:0] bits are not write protected by the SES bit. Unless the PAWS[2] bit is set, writes to CLKPE[1:0] in software should not be changed if SES = 1.*

The default reset state of CLKPE[1:0] is 00.

Table 9-5. Clock Period Exponent and Pulse Width Range

ERASE	CLKPE[1:0]	Exponent (N)	Pulse Width Range for all System Clock Frequencies from 8.0 MHz to 33.0 MHz	
			Minimum $2^N \times 1.25E-7$	Maximum[1] $2^N \times 128 \times 8.33E-8$
0	00	5	4.00 µs	0.34 ms
	01	6	8.00 µs	0.68 ms
	10	7	16.00 µs	1.36 ms
	11	8	32.0 µs	2.73 ms
1	00	15	4.096 ms	349.5 ms
	01	16	8.192 ms	699.0 ms
	10	17	16.39 ms	1.398 s
	11	18	32.77 ms	2.796 s

1. The maximum system clock frequency is 33 MHz.

BLOCK[7:0] — Block Program and Erase Field

The read/write BLOCK[7:0] field selects array blocks for program or erase operation. BLOCK[7:0] is writable when the SES bit is clear. If SES is written in the same cycle with BLOCK[7:0] bits, the write permission to BLOCK[7:0] bits depends on the previous value of SES. Up to eight blocks at once can be selected for program operation. Array blocks that correspond to 1s in BLOCK[7:0] are selected for program or erase operation. The BLOCK[7:0] default state is $00, not selected for program or erase.

1 = Array block selected for program or erase
0 = Array block not selected for program or erase

RSVD6 — Reserved

Reserved for test purposes. Writing to this read/write bit updates the values and could affect functionality if set to 1.

ERASE — Program or Erase Select Bit

The read-always ERASE bit selects program or erase operations. ERASE is writable when the SES bit is clear. If SES and ERASE are written in the same cycle, the write permission to ERASE bit depends on the previous value of SES.

When ERASE = 0, the array is configured for programming, and if SES = 1 the SIE bit is write locked. When ERASE = 1, the array is configured for erasing, and SES does not write lock the SIE bit.

1 = Erase operation
0 = Program operation

SES — Start/End Sequence Bit

The read-always SES bit signals the start and end of a program or erase sequence. SES is writable when the HVS and EHV bits are clear. If SES and EHV are written in the same cycle, the write permission to SES depends on the previous value of EHV. At the start of a program or erase sequence, SES is set, locking PROTECT[7:0], BLOCK[7:0], and ERASE.

1 = CMFR configured for program or erase operation
0 = CMFR not configured for program or erase operation

NOTE: *SES does not lock the SCLKR[2:0], CLKPE[1:0], and CLKPM[6:0] bits. Do not change these bits in software when SES = 1 unless PAWS[2] = 1.*

Section 11. Ports Module

11.1 Contents

15.7.10 Timer Interrupt Enable Register

Address: TIM1 — 0x00ce_000c
TIM2 — 0x00cf_000c

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	C3I	C2I	C1I	C0I
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 15-13. Timer Interrupt Enable Register (TIMIE)

Read: Anytime

Write: Anytime

C[3:0]I — Channel Interrupt Enable Bits

C[3:0]I enable the C[3:0]F flags in timer flag register 1 to generate interrupt requests.

1 = Corresponding channel interrupt requests enabled
0 = Corresponding channel interrupt requests disabled

15.7.12 Timer Flag Register 1

Address: TIM1 — 0x00ce_000e
TIM2 — 0x00cf_000e

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	C3F	C2F	C1F	C0F
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 15-15. Timer Flag Register 1 (TIMFLG1)

Read: Anytime

Write: Anytime; writing 1 clears flag; writing 0 has no effect

C[3:0]F — Channel Flags

A channel flag is set when an input capture or output compare event occurs. Clear a channel flag by writing a 1 to it.

NOTE: *When the fast flag clear all bit, TFFCA, is set, an input capture read or an output compare write clears the corresponding channel flag. TFFCA is in timer system control register 1 (TIMSCR1).*

When a channel flag is set, it does not inhibit subsequent output compares or input captures.

16.7.6 SCI Data Registers

Address: SCI1 — 0x00cc_0006
SCI2 — 0x00cd_0006

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	R8	T8	0	0	0	0	0	0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 16-8. SCI Data Register High (SCIDRH)

Address: SCI1 — 0x00cc_0007
SCI2 — 0x00cd_0007

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	R7	R6	R5	R4	R3	R2	R1	R0
Write:	T7	T6	T5	T4	T3	T2	T1	T0
Reset:	0	0	0	0	0	0	0	0

Figure 16-9. SCI Data Register Low (SCIDRL)

Read: Anytime

Write: Anytime; writing to R8 has no effect

R8 — Receive Bit 8

The R8 bit is the ninth received data bit when using the 9-bit data format (M = 1). Reset clears R8.

T8 — Transmit Bit 8

The T8 bit is the ninth transmitted data bit when using the 9-bit data format (M = 1). Reset clears T8.

R[7:0] — Receive Bits [7:0]

The R[7:0] bits are receive bits [7:0] when using the 9-bit or 8-bit data format. Reset clears R[7:0].

T[7:0] — Transmit Bits [7:0]

The T[7:0] bits are transmit bits [7:0] when using the 9-bit or 8-bit data format. Reset clears T[7:0].

Section 18. Queued Analog-to-Digital Converter (QADC)

18.1 Contents

19.7.1 Read Cycles

During a read cycle, the EBI receives data from an external memory or peripheral device. During external read cycles, the $\overline{OE}$ pin is asserted regardless of operand size. See **Figure 19-1**.

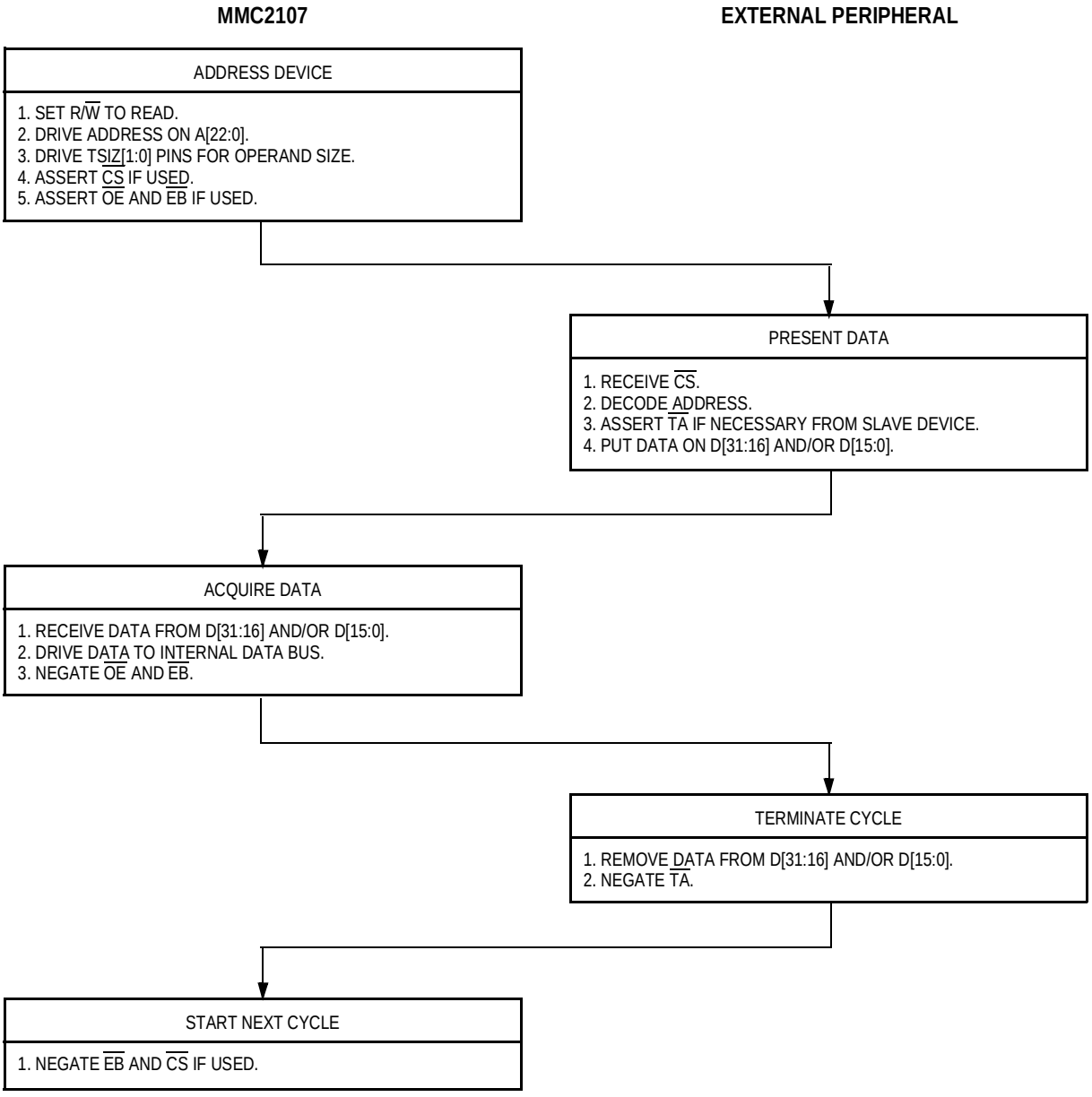

Figure 19-1. Read Cycle Flowchart

pin is asserted before the chip select logic asserts the internal cycle termination signal, then the bus cycle is terminated early.

If internal address bit 31 is 0, then the access is internal. If internal address bit 31 is 1, then the access is external.

NOTE: *Chip select logic does not decode internal address bits A[30:25].*

Table 20-4. Chip Select Address Range Encoding

Chip Select	Block Size	Address Bits Compared (A[31:23])(1)
$\overline{CS0}$	8 MB	1XXX_XXX0_0
$\overline{CS1}$	8 MB	1XXX_XXX0_1(2)
$\overline{CS2}$	8 MB	1XXX_XXX1_0
$\overline{CS3}$	8 MB	1XXX_XXX1_1

1. The chip selects do not decode A[30:25]. Thus, the total 32-Mbyte block size is repeated/mirrored in external memory space.
2. If the EMINT bit in the chip configuration module CCR is set, then $\overline{CS1}$ matches only internal accesses to the 8-MB block starting at address 0 to support emulation of internal memory. Thus, A[31:23] match 0xxx_xxx0_0.

20.8 Interrupts

The chip select module does not generate interrupt requests.

21.12 Low-Level TAP (OnCE) Module

The low-level TAP (OnCE, on-chip emulation) circuitry provides a simple, inexpensive debugging interface that allows external access to the processor's internal registers and to memory/peripherals. OnCE capabilities are controlled through a serial interface, mapped onto a JTAG test access port (TAP) protocol.

Refer to **Figure 21-4** for a block diagram of the OnCE.

NOTE: *The interface to the OnCE controller and its resources is based on the TAP defined for JTAG in the IEEE 1149.1 standard.*

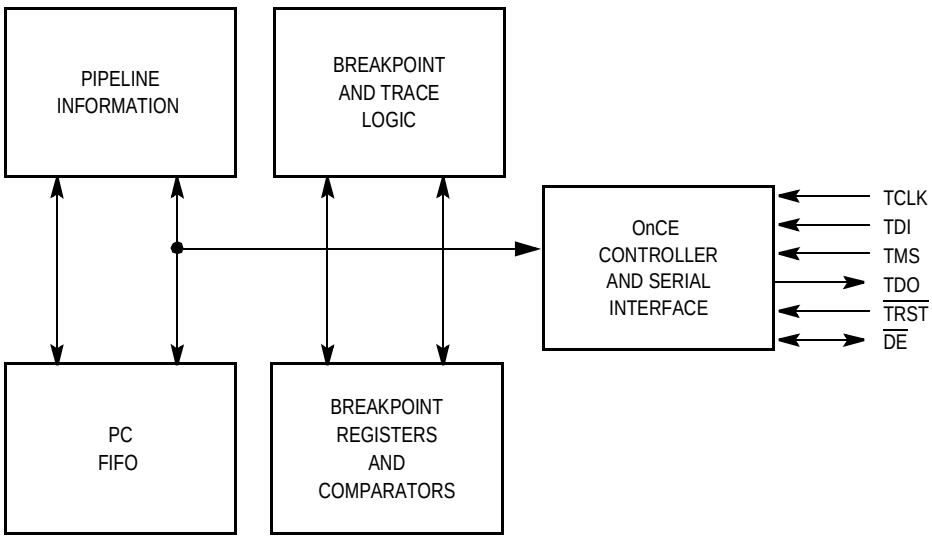

Figure 21-4. OnCE Block Diagram

Figure 21-5 shows the OnCE (low-level TAP module) data registers in the MMC2107.

Table 21-4. OnCE Register Addressing

RS4–RS0	Register Selected
00000	Reserved
00001	Reserved
00010	Reserved
00011	OTC — OnCE trace counter
00100	MBCA — memory breakpoint counter A
00101	MBCB — memory breakpoint counter B
00110	PC FIFO — program counter FIFO and increment counter
00111	BABA — breakpoint address base register A
01000	BABB — breakpoint address base register B
01001	BAMA — breakpoint address mask register A
01010	BAMB — breakpoint address mask register B
01011	CPUSCR — CPU scan chain register
01100	Bypass — no register selected
01101	OCR — OnCE control register
01110	OSR — OnCE status register
01111	Reserved (factory test control register — do not access)
10000	Reserved (MEM_BIST — do not access)
10001–10110	Reserved (bypass, do not access)
10111	Reserved (LSRL, do not access)
11000–11110	Reserved (bypass, do not access)
11111	Bypass

21.14.4.2 OnCE Control Register

The 32-bit OnCE control register (OCR) selects the events that put the device in debug mode and enables or disables sections of the OnCE logic.

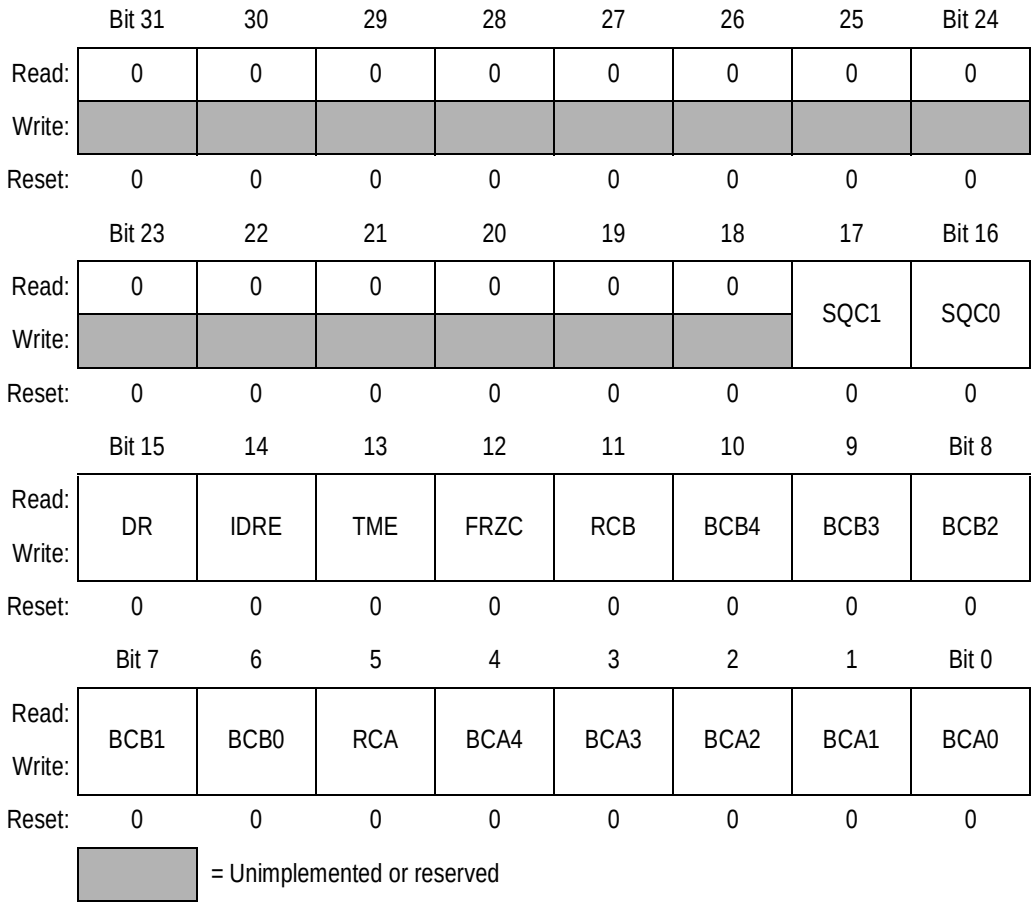

Figure 21-9. OnCE Control Register (OCR)

SQC1 and SQC0 — Sequential Control Field

The SQC field allows memory breakpoint B and trace occurrences to be suspended until a qualifying event occurs. Test logic reset clears the SQC field. See **Table 21-5**.

Table 21-6. Memory Breakpoint Control Field Settings

BCB4–BCB0 BCA4–BCA0	Description
00000	Breakpoint disabled
00001	Qualify match with any access
00010	Qualify match with any instruction access
00011	Qualify match with any data access
00100	Qualify match with any change of flow instruction access
00101	Qualify match with any data write
00110	Qualify match with any data read
00111	Reserved
01XXX	Reserved
10000	Reserved
10001	Qualify match with any user access
10010	Qualify match with any user instruction access
10011	Qualify match with any user data access
10100	Qualify match with any user change of flow access
10101	Qualify match with any user data write
10110	Qualify match with any user data read
10111	Reserved
11000	Reserved
11001	Qualify match with any supervisor access
11010	Qualify match with any supervisor instruction access
11011	Qualify match with any supervisor data access
11100	Qualify match with any supervisor change of flow access
11101	Qualify match with any supervisor data write
11110	Qualify match with any supervisor data read
11111	Reserved