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Details	
Product Status	Obsolete
Core Processor	M210
Core Size	16/32-Bit
Speed	33MHz
Connectivity	EBI/EMI, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	72
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mmc2107cfcpv33

Section 12. Edge Port Module (EPORT)

Section 13. Watchdog Timer Module

Address	Register Name		Bit Number							
Edge Port (EPORT)										
			Bit 15	14	13	12	11	10	9	Bit 8
0x00c6_0000 0x00c6_0001	EPORT Pin Assignment Register (EPPAR) See page 264.	Read: Write:	EPPA7		EPPA6		EPPA5		EPPA4	
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
		Read: Write:	EPPA3		EPPA2		EPPA1		EPPA0	
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c6_0002	EPORT Data Direction Register (EPDDR) See page 266.	Read: Write:	EPDD7	EPDD6	EPDD5	EPDD4	EPDD3	EPDD2	EPDD1	EPDD0
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c6_0003	EPORT Port Interrupt Enable Register (EPIER) See page 267.	Read: Write:	EPIE7	EPIE6	EPIE5	EPIE4	EPIE3	EPIE2	EPIE1	EPIE0
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c6_0004	EPORT Port Data Register (EPDR) See page 268.	Read: Write:	EPD7	EPD6	EPD5	EPD4	EPD3	EPD2	EPD1	EPD0
		Reset:	1	1	1	1	1	1	1	1
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c6_0005	EPORT Port Pin Data Register (EPPDR) See page 268.	Read:	EPPD7	EPPD6	EPPD5	EPPD4	EPPD3	EPPD2	EPPD1	EPPD0
		Write:								
		Reset:	P	P	P	P	P	P	P	P
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c6_0006	EPORT Port Flag Regiser (EPFR) See page 269.	Read: Write:	EPF7	EPF6	EPF5	EPF4	EPF3	EPF2	EPF1	EPF0
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c6_0007	Reserved		Writes have no effect, reads return 0s, and the access terminates without a transfer error exception.							

P = Current pin state U = Unaffected = Writes have no effect and the access terminates without a transfer error exception.

Figure 2-2. Register Summary (Sheet 17 of 34)

Address	Register Name		Bit Number							
Timer 1 (TIM1) and Timer 2 (TIM2)										
Note: Addresses for TIM1 are at 0x00ce_#### and addresses for TIM2 are at 0x00cf_####.										
			Bit 7	6	5	4	3	2	1	Bit 0
0x00ce_0000 0x00cf_0000	Timer Input Capture/ Output Compare Select Register (TIMIOS) See page 300.	Read:	0	0	0	0	IOS3	IOS2	IOS1	IOS0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00ce_0001 0x00cf_0001	Timer Compare Force Register (TIMCFORC) See page 301.	Read:	0	0	0	0	0	0	0	0
		Write:					FOC3	FOC2	FOC1	FOC0
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00ce_0002 0x00cf_0002	Timer Output Compare 3 Mask Register (TIMOC3M) See page 302.	Read:	0	0	0	0	OC3M3	OC3M2	OC3M1	OC3M0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00ce_0003 0x00cf_0003	Timer Output Compare 3 Data Register (TIMOC3D) See page 303.	Read:	0	0	0	0	OC3D3	OC3D2	OC3D1	OC3D0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00ce_0004 0x00cf_0004	Timer Counter Register High (TIMCNTH) See page 304.	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00ce_0005 0x00cf_0005	Timer Counter Register Low (TIMCNTL) See page 304.	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00ce_0006 0x00cf_0006	Timer System Control Register 1 (TIMSCR1) See page 305.	Read:	TIMEN	0	0	TFFCA	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0

P = Current pin state U = Unaffected = Writes have no effect and the access terminates without a transfer error exception.

Figure 2-2. Register Summary (Sheet 28 of 34)

LOAD — Pad Driver Load Bit

The LOAD bit selects full or default drive strength for selected pad output drivers. For maximum capacitive load, set the LOAD bit to select full drive strength. For reduced power consumption, clear the LOAD bit to select default drive strength.

1 = Full drive strength
0 = Default drive strength

Table 3-2 shows the read/write accessibility of this write-once bit.

SHEN — Show Cycle Enable Bit

The SHEN bit enables the external memory interface to drive the external bus during internal transfer operations.

1 = Show cycles enabled
0 = Show cycles disabled

In emulation mode, the SHEN bit is read-only. In all other modes, it is a read/write bit.

EMINT — Emulate Internal Address Space Bit

The EMINT bit enables chip select 1 (CS1) to decode the internal memory address space.

1 = CS1 decodes internal memory address space.
0 = CS1 decodes external memory address space.

The EMINT bit is read-always but can be written only in emulation mode.

MODE[2:0] — Chip Configuration Mode Field

This read-only field reflects the chip configuration mode, as shown in Table 3-4.

Table 3-4. Chip Configuration Mode Selection

MODE[2:0]	Chip Configuration Mode
111	Master mode
110	Single-chip mode
10X	FAST mode
0XX	Emulation mode

4.5.2 Phase-Lock Loop (PLL) and Clock Signals

These signals are used to support the on-chip clock generation circuitry.

4.5.2.1 External Clock In (EXTAL)

This input signal is always driven by an external clock input except when used as a connection to the external crystal when the internal oscillator circuit is used. The clock source is configured during reset.

4.5.2.2 Crystal (XTAL)

This output signal is used as a connection to the external crystal when the internal oscillator circuit is used. XTAL should be grounded when using an external clock input.

4.5.2.3 Clock Out (CLKOUT)

This output signal reflects the internal system clock.

4.5.2.4 Synthesizer Power (V_{DDSYN} and V_{SSSYN})

These are dedicated quiet power and ground supply signals for the frequency synthesizer circuit.

4.5.3 External Memory Interface Signals

In addition to the function stated here, these signals can be configured as discrete I/O signals also.

4.5.3.1 Data Bus (D[31:0])

These three-state bidirectional signals provide the general-purpose data path between the microcontroller unit (MCU) and all other devices.

RSVD24 — Reserved

Writing to this read/write bit updates the value but has no effect on functionality.

SUPV[7:0] — Supervisor Space Field

The read-always SUPV[7:0] field controls supervisor/unrestricted address space assignment of array blocks. The field is writable when the LOCKCTL bit is clear.

Array blocks that correspond to 1s in SUPV[7:0] are selected for data address space.

Each array block can be mapped into supervisor or unrestricted address space. When an array block is mapped into supervisor address space (SUPV[M] = 1) only supervisor accesses are allowed. A user access to a location in supervisor address space causes a data error exception. When an array block is mapped into unrestricted address space (SUPV[M] = 0) both supervisor and user accesses are allowed.

The default reset state of SUPV[7:0] bits are supervisor address space (SUPV[M] = 1).

1 = Array block in supervisor address space
0 = Array block in unrestricted address space

DATA[7:0] — Data Space Field

The read-always DATA[7:0] field controls data/program address space assignment of array blocks. When LOCKCTL = 1, the DATA[7:0] field is write-protected, and writing to it has no effect.

Array blocks that correspond to 1s in DATA[7:0] are selected for data address space.

Each array block can be mapped into data address space or both data and program address space. When an array block is mapped into data address space (DATA[M] = 1) only data accesses are allowed. A program access to a location in data address space causes a data error exception. When an array block is mapped into both data and program address space (DATA[M] = 0) both data and program accesses are allowed.

The default reset state of DATA[7:0] bits are data and program address space (DATA[M] = 0).

1 = Array block in data address space
0 = Array block is both data and program address space

After lock is detected, the lock circuit continues to monitor the reference and feedback frequencies using the alternate count and compare process. If the counters do not match at any comparison time, then the LOCK flag is cleared to indicate that the PLL has lost lock. At this point, the lock criteria is tightened and the lock detect process is repeated.

The alternate count sequences prevent false lock detects due to frequency aliasing while the PLL tries to lock. Alternating between tight and relaxed lock criteria prevents the lock detect function from randomly toggling between locked and non-locked status due to phase sensitivities. **Figure 10-6** shows the sequence for detecting locked and non-locked conditions.

In external clock mode, the PLL is disabled and cannot lock.

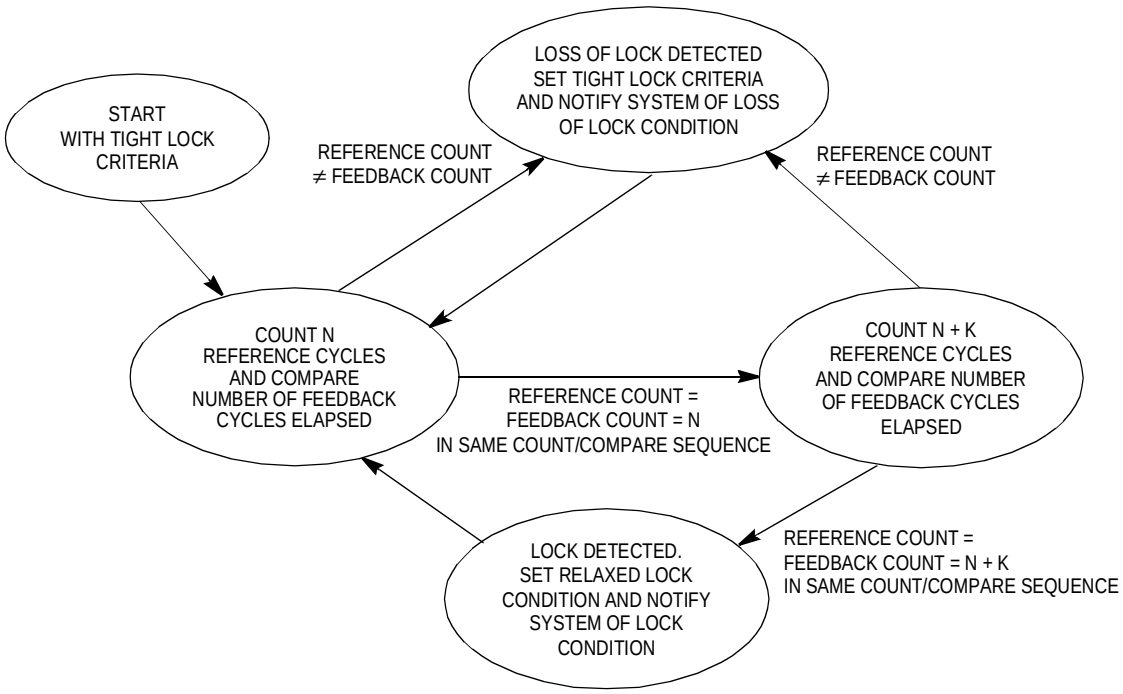

Figure 10-6. Lock Detect Sequence

Table 10-8. Stop Mode Operation (Sheet 1 of 3)

MODE In	LOCEN	LOCRE	LOLRE	PLL	OSC	FWKUP	Expected PLL Action at Stop	PLL Action During Stop	MODE Out	LOCKS	LOCK	LOCS	Comments
EXT	X	X	X	X	X	X	—	—	EXT	0	0	0	
								Lose reference clock	Stuck	—	—	—	
NRM	0	0	0	Off	Off	0	Lose lock, f.b. clock, reference clock	Regain	NRM	‘LK	1	‘LC	
								No regain	Stuck	—	—	—	
NRM	X	0	0	Off	Off	1	Lose lock, f.b. clock, reference clock	Regain clocks, but don’t regain lock	SCM–> unstable NRM	0–>‘LK	0–>1	1–>‘LC	Block LOCS and LOCKS until clock and lock respectively regain; enter SCM regardless of LOCEN bit until reference regained
								No reference clock regain	SCM–>	0–>	0–>	1–>	Block LOCS and LOCKS until clock and lock respectively regain; enter SCM regardless of LOCEN bit
								No f.b. clock regain	Stuck	—	—	—	
NRM	0	0	0	Off	On	0	Lose lock	Regain	NRM	‘LK	1	‘LC	Block LOCKS from being cleared
								Lose reference clock or no lock regain	Stuck	—	—	—	
								Lose reference clock, regain	NRM	‘LK	1	‘LC	Block LOCKS from being cleared
NRM	0	0	0	Off	On	1	Lose lock	No lock regain	Unstable NRM	0–>‘LK	0–>1	‘LC	Block LOCKS until lock regained
								Lose reference clock or no f.b. clock regain	Stuck	—	—	—	
								Lose reference clock, regain	Unstable NRM	0–>‘LK	0–>1	‘LC	LOCS not set because LOCEN = 0
NRM	0	0	0	On	On	0	—	—	NRM	‘LK	1	‘LC	
								Lose lock or clock	Stuck	—	—	—	
								Lose lock, regain	NRM	0	1	‘LC	
								Lose clock and lock, regain	NRM	0	1	‘LC	LOCS not set because LOCEN = 0
NRM	0	0	0	On	On	1	—	—	NRM	‘LK	1	‘LC	
								Lose lock	Unstable NRM	0	0–>1	‘LC	
								Lose lock, regain	NRM	0	1	‘LC	
								Lose clock	Stuck	—	—	—	
								Lose clock, regain without lock	Unstable NRM	0	0–>1	‘LC	
								Lose clock, regain with lock	NRM	0	1	‘LC	

12.5.2.2 EPORT Data Direction Register

Address: 0x00c6_0002

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	EPDD7	EPDD6	EPDD5	EPDD4	EPDD3	EPDD2	EPDD1	EPDD0
Reset:	0	0	0	0	0	0	0	0

Figure 12-3. EPORT Data Direction Register (EPDDR)

EPDD[7:0] — Edge Port Data Direction Bits

Setting any bit in the EPDDR configures the corresponding pin as an output. Clearing any bit in EPDDR configures the corresponding pin as an input. Pin direction is independent of the level/edge detection configuration. Reset clears EPDD[7:0].

To use an EPORT pin as an external interrupt request source, its corresponding bit in EPDDR must be clear. Software can generate interrupt requests by programming the EPORT data register when the EPDDR selects output.

1 = Corresponding EPORT pin configured as output
0 = Corresponding EPORT pin configured as input

12.5.2.6 Edge Port Flag Register

Address: 0x00c6_0006

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	EPF7	EPF6	EPF5	EPF4	EPF3	EPF2	EPF1	EPF0
Reset:	0	0	0	0	0	0	0	0

Figure 12-7. EPORT Port Flag Register (EPFR)

EPF[7:0] — Edge Port Flag Bits

When an EPORT pin is configured for edge triggering, its corresponding read/write bit in EPFR indicates that the selected edge has been detected. Reset clears EPF[7:0].

1 = Selected edge for INTx pin has been detected.
0 = Selected edge for INTx pin has not been detected.

Bits in this register are set when the selected edge is detected on the corresponding pin. A bit remains set until cleared by writing a 1 to it. Writing 0 has no effect. If a pin is configured as level-sensitive (EPPARx = 00), pin transitions do not affect this register.

Section 14. Programmable Interrupt Timer Modules (PIT1 and PIT2)

14.1 Contents

16.7.2 SCI Control Register 1

Address: SCI1 — 0x00cc_0002
SCI2 — 0x00cd_0002

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	LOOPS	WOMS	RSRC	M	WAKE	ILT	PE	PT
Reset:	0	0	0	0	0	0	0	0

Figure 16-4. SCI Control Register 1 (SCICR1)

Read: Anytime

Write: Anytime

LOOPS — Loop Select Bit

This read/write control bit switches the SCI between normal mode and loop mode. Reset clears LOOPS.

1 = Loop mode SCI operation
0 = Normal mode SCI operation

The SCI operates normally (LOOPS = 0, RSRC = X) when the output of its transmitter is connected to the TXD pin, and the input of its receiver is connected to the RXD pin.

In loop mode (LOOPS =1, RSRC = 0), the input to the SCI receiver is internally disconnected from the RXD pin logic and instead connected to the output of the SCI transmitter. The behavior of TXD is governed by the DDRSC1 bit in SCIDDR. If DDRSC1 = 1, the TXD pin is driven with the output of the SCI transmitter. If DDRSC1 = 0, the TXD pin idles high. See **16.14 Loop Operation** for additional information.

For either loop mode or single-wire mode to function, both the SCI receiver and transmitter must be enabled by setting the RE and TE bits in SCIxCR2.

NOTE: *The RXD pin becomes general-purpose I/O when LOOPS = 1, regardless of the state of the RSRC bit. DDRSC0 in SCIDDR is the data direction bit for the RXD pin.*

Table 16-3 shows how the LOOPS, RSRC, and DDRSC0 bits affect SCI operation and the configuration of the RXD and TXD pins.

16.10 Baud Rate Generation

A 13-bit modulus counter in the baud rate generator derives the baud rate for both the receiver and the transmitter. The value from 0 to 8191 written to SCIBDH and SCIBDL determines the system clock divisor. The baud rate clock is synchronized with the bus clock and drives the receiver. The baud rate clock divided by 16 drives the transmitter. The receiver acquisition rate is 16 samples per bit time.

Baud rate generation is subject to two sources of error:

1. Integer division of the module clock may not give the exact target frequency.
2. Synchronization with the bus clock can cause phase shift.

Table 16-4. Example Baud Rates (System Clock = 33 MHz)

SBR[12:0]	Receiver Clock (Hz)	Transmitter Clock (Hz)	Target Baud Rate	Percent Error
0x0012	1,833,333.3	114,583.3	115,200	0.54
0x0024	916,666.7	57,291.7	57,600	0.54
0x0036	611,111.1	38,194.4	38,400	0.54
0x003d	540,983.6	33,811.4	33,600	0.63
0x0048	458,333.3	28,645.8	28,800	0.54
0x006b	308,411.2	19,275.7	19,200	0.39
0x0008f	230,769.2	14,423.1	14,400	0.16
0x00d7	153,488.4	95,93.0	9,600	0.07
0x01ae	76,744.2	4,796.5	4,800	0.07
0x035b	38,416.8	2,401.0	2,400	0.04
0x06b7	19,197.2	1,199.8	1,200	0.01
0x0d6d	9,601.4	600.1	600	0.01
0x1adb	4,800.0	300.0	300	0

16.11.1 Frame Length

The transmitter can generate either 10-bit or 11-bit frames. In SCICR1, the M bit selects frame length, and the PE bit enables the parity function. One data bit may be an address mark or an extra stop bit. All frames begin with a start bit and end with one or two stop bits. When transmitting 9-bit data, bit T8 in SCI data register high (SCIDRH) is the ninth bit (bit 8).

Table 16-5. Example 10-Bit and 11-Bit Frames

M Bit	Frame Length	Start Bit	Data Bits	Parity Bit	Address Mark[1]	Stop Bit(s)
0	10 bits	1	8	No	No	1
		1	7	No	No	2
		1	7	No	Yes	1
		1	7	Yes	No	1
1	11 bits	1	9	No	No	1
		1	8	No	No	2
		1	8	No	Yes	1
		1	8	Yes	No	1
		1	7	No	Yes	2
		1	7	Yes	No	2

1. When implementing a multidrop network using the SCI, the address mark bit is used to designate subsequent data frames as a network address and not device data.

17.7.1 SPI Control Register 1

Address: 0x00cb_0000

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	SPIE	SPE	SWOM	MSTR	CPOL	CPHA	SSOE	LSBFE
Reset:	0	0	0	0	0	1	0	0

Figure 17-2. SPI Control Register 1 (SPICR1)

Read: Anytime

Write: Anytime

SPIE — SPI Interrupt Enable Bit

The SPIE bit enables the SPIF and MODF flags to generate interrupt requests. Reset clears SPIE.

1 = SPIF and MODF interrupt requests enabled
0 = SPIF and MODF interrupt requests disabled

SPE — SPI System Enable Bit

The SPE bit enables the SPI and dedicates SPI port pins [3:0] to SPI functions. When SPE is clear, the SPI system is initialized but in a low-power disabled state. Reset clears SPE.

1 = SPI enabled
0 = SPI disabled

SWOM — SPI Wired-OR Mode Bit

The SWOM bit configures the output buffers of SPI port pins [3:0] as open-drain outputs. SWOM controls SPI port pins [3:0] whether they are SPI outputs or general-purpose outputs. Reset clears SWOM.

1 = Output buffers of SPI port pins [3:0] open-drain
0 = Output buffers of SPI port pins [3:0] CMOS drive

17.8 Functional Description

The SPI module allows full-duplex, synchronous, serial communication between the MCU and peripheral devices. Software can poll the SPI status flags or SPI operation can be interrupt driven.

Setting the SPE bit in SPICR1 enables the SPI and dedicates four SPI port pins to SPI functions:

- Slave select ($\overline{SS}$)
- Serial clock (SCK)
- Master out/slave in (MOSI)
- Master in/slave out (MISO)

When the SPE bit is clear, the $\overline{SS}$, SCK, MOSI, and MISO pins are general-purpose I/O pins controlled by SPIDDR.

The 8-bit shift register in a master SPI is linked by the MOSI and MISO pins to the 8-bit shift register in the slave. The linked shift registers form a distributed 16-bit register. In an SPI transmission, the SCK clock from the master shifts the data in the 16-bit register eight bit positions, and the master and slave exchange data. Data written to the master SPIDR register is the output data to the slave. After the exchange, data read from the master SPIDR is the input data from the slave.

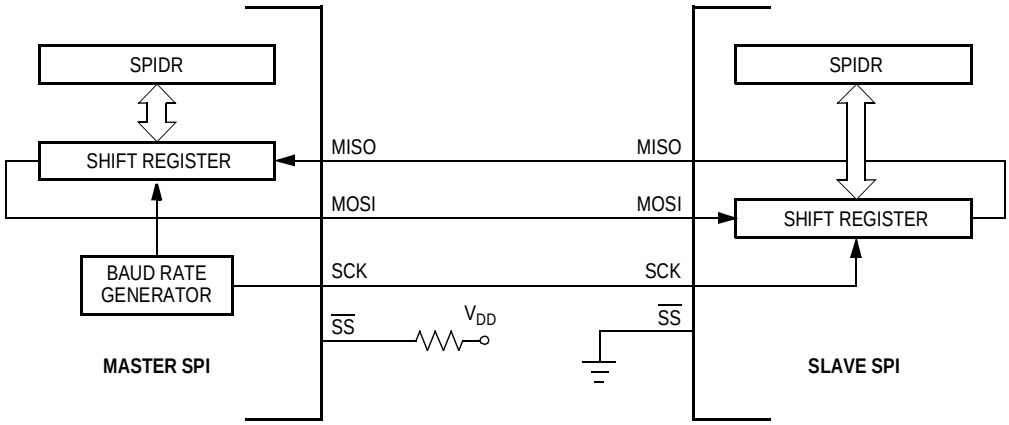

Figure 17-10. Full-Duplex Operation

- Output data readable in three formats:
  - Right-justified unsigned
  - Left-justified signed
  - Left-justified unsigned
- Unused analog channels can be used as digital ports

18.4 Block Diagram

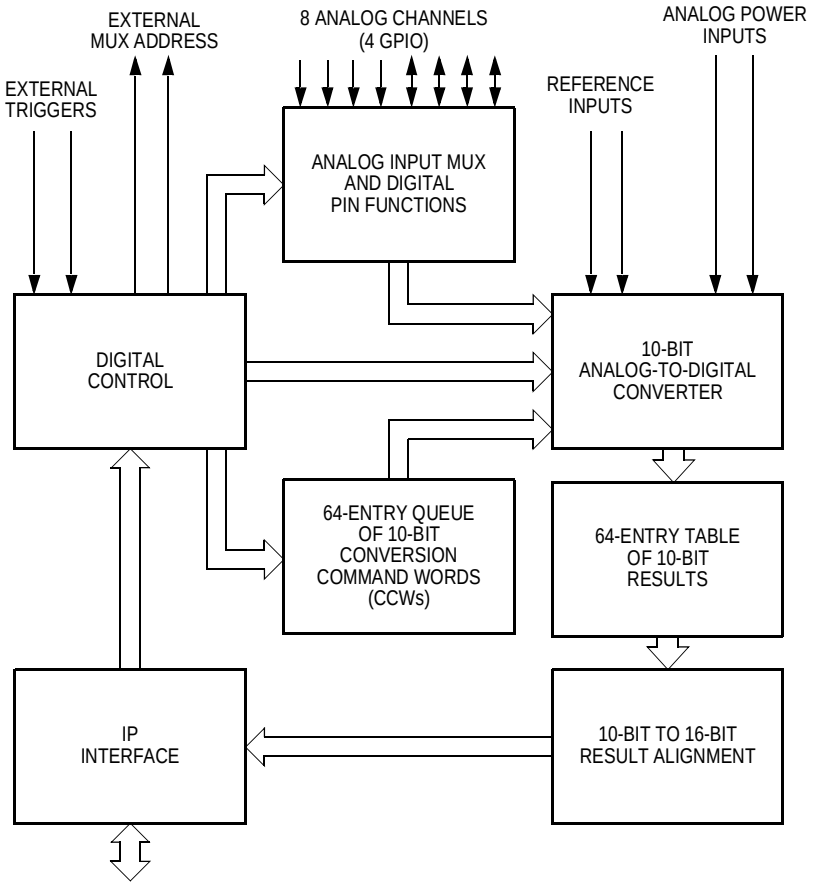

Figure 18-1. QADC Block Diagram

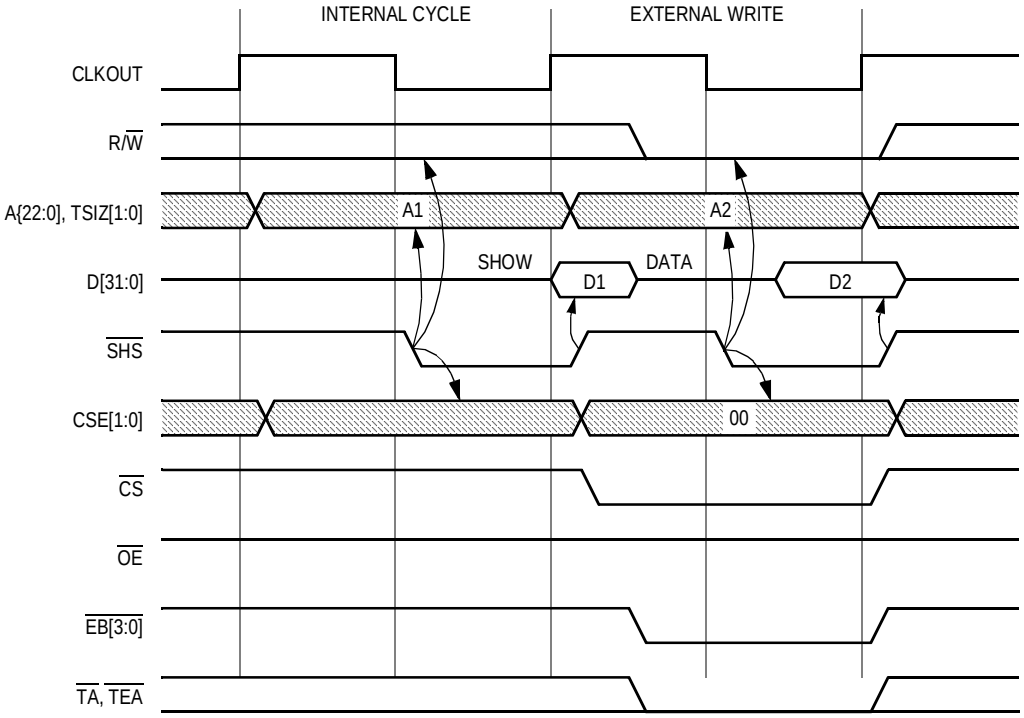

Figure 19-6. Internal (Show) Cycle Followed by External 1-Clock Write

19.10 Bus Monitor

The bus monitor can be set detects excessively long bus access termination response times. Whenever an undecoded address is accessed or a peripheral is inoperative, the access is not terminated and the bus is potentially locked up while it waits for the required response.

The bus monitor monitors the cycle termination response times during a bus cycle. If the cycle termination response time exceeds a programmed count, the bus monitor asserts an internal bus error.

The bus monitor monitors the cycle termination response time (in system clock cycles) by using a programmable maximum allowable response period. There are four selectable response time periods for the bus monitor, selectable among 8, 16, 32, and 64 system clock cycles. The periods are selectable with the BMT[1:0] field in the chip configuration module CCR. The programmability of the timeout allows for varying external peripheral response times. The monitor is cleared and restarted