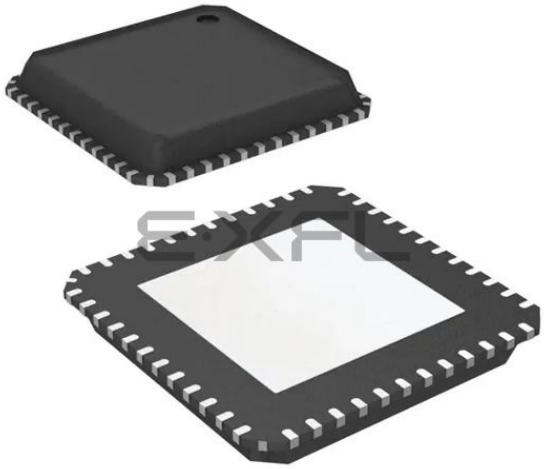

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Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Automotive
Core Processor	XC800
Program Memory Type	FLASH (64kB)
Controller Series	-
RAM Size	3.25K x 8
Interface	LIN, SSI, UART
Number of I/O	11
Voltage - Supply	3V ~ 27V
Operating Temperature	-40°C ~ 150°C (TJ)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-48-29
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tle9834qxxuma1

Edition 2012-03-08

Published by
Infineon Technologies AG
81726 Munich, Germany

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Table of Contents

1 Summary of Features

- High performance XC800 core
  - compatible to standard 8051 core
  - up to 40 MHz clock frequency
  - two clocks per machine cycle architecture
  - two data pointers
- On-chip memory
  - 60 kByte + 4 kByte Flash for program code and data (4 kByte EEPROM emulation built-in)
  - 512 Byte One Time Programmable Memory (OTP)
  - 512 Byte 100 Time Programmable Memory (100TP)
  - 256 Byte RAM, 3 kByte XRAM
  - BootROM for startup firmware and Flash routines
- Core logic supply at 1.5 V
- On-chip OSC and PLL for clock generation
  - Loss of clock detection with fail safe mode for power switches
- Watchdog timer (WDT) with programmable window feature for refresh operation and warning prior to overflow
- General-purpose I/O Port (GPIO) with wake-up capability
- Multiplication/division unit (MDU) for arithmetic calculation
- Software libraries to support floating point and MDU calculations
- Five 16-Bit timers - Timer 0, Timer 1, Timer 2, Timer 21 and Timer 3
- Capture/compare unit for PWM signal generation (CCU6) with Timer 12 and Timer 13
- Full duplex serial interface (UART) with LIN support
- Synchronous serial channel (SSC)
- On-chip debug support via 2-wire Device Access Port (DAP)
- LIN Bootstrap loader (LIN BSL)
- LIN transceiver compliant to LIN 1.3, LIN 2.0 and LIN 2.1
- 2 x Low Side Switches with clamping capability incl. PWM functionality, e.g. as relay driver
- 2 x High Side Switches with cyclic sense option and PWM functionality, e.g. for LED or powering of switches
- 5 x High Voltage Monitor Input pins for wake-up and with cyclic sense and analog measurement option
- Measurement unit with 10 channels, 8-Bit A/D Converter (ADC2) and data post processing
- 8 channels, 10-Bit A/D Converter (including battery voltage and supply voltage measurement) (ADC1)
- Single power supply from 3.0 V to 27 V
- Low-dropout voltage regulators (LDO)
- Dedicated 5 V voltage regulator for external loads (e.g. hall sensor)
- Programmable window watchdog (WDT1) with independent on-chip clock source
- Power saving modes
  - MCU slow-down mode
  - Stop Mode
  - Sleep Mode
  - Cyclic wake-up and cyclic sense during Stop Mode and Sleep Mode
- Power-on and undervoltage/brownout reset generator
- Overtemperature protection
- Overcurrent protection with shutdown
- Supported by a full range of development tools including C compilers, macro assembler packages, emulators, evaluation boards, HLL debugger, programming tools, software packages
- Temperature Range T_J: -40 °C up to 150 °C
- Package VQFN-48-29
- Green package (RoHS compliant)

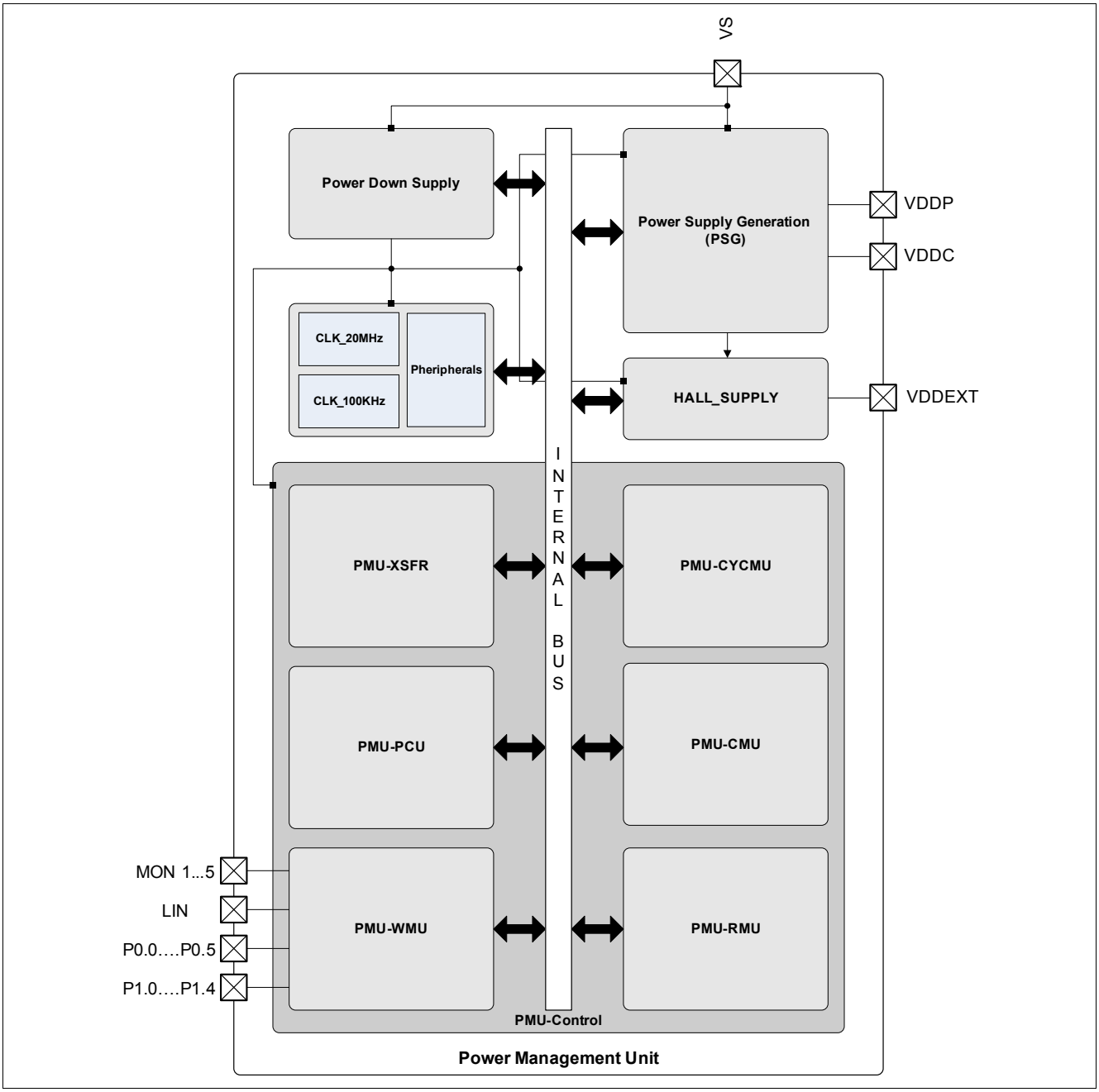

Figure 5 Power Management Unit Block Diagram

3.1.2 Voltage Regulator 1.5V (VDDC)

This module represents the 1.5 V voltage regulator, which serves as core supply for the 8-bit µC and other chip internal analog 1.5 V functions (e.g. 8 Bit ADC). To further reduce the current consumption of the 8-bit MCU during Stop Mode the output voltage is optionally reduced to 0.9 V.

Features

- 1.5 V low-drop voltage regulator
- Optional 0.9 V in Stop Mode
- Current limitation
- Overcurrent monitoring and shutdown with MCU signalling (interrupt)
- Overvoltage monitoring with MCU signalling (interrupt)
- Undervoltage monitoring with MCU signalling (interrupt)
- Pull-down current source at the output for Sleep Mode (100 µA)

The output capacitor C_{VDDC} is mandatory to ensure a proper regulator functionality.

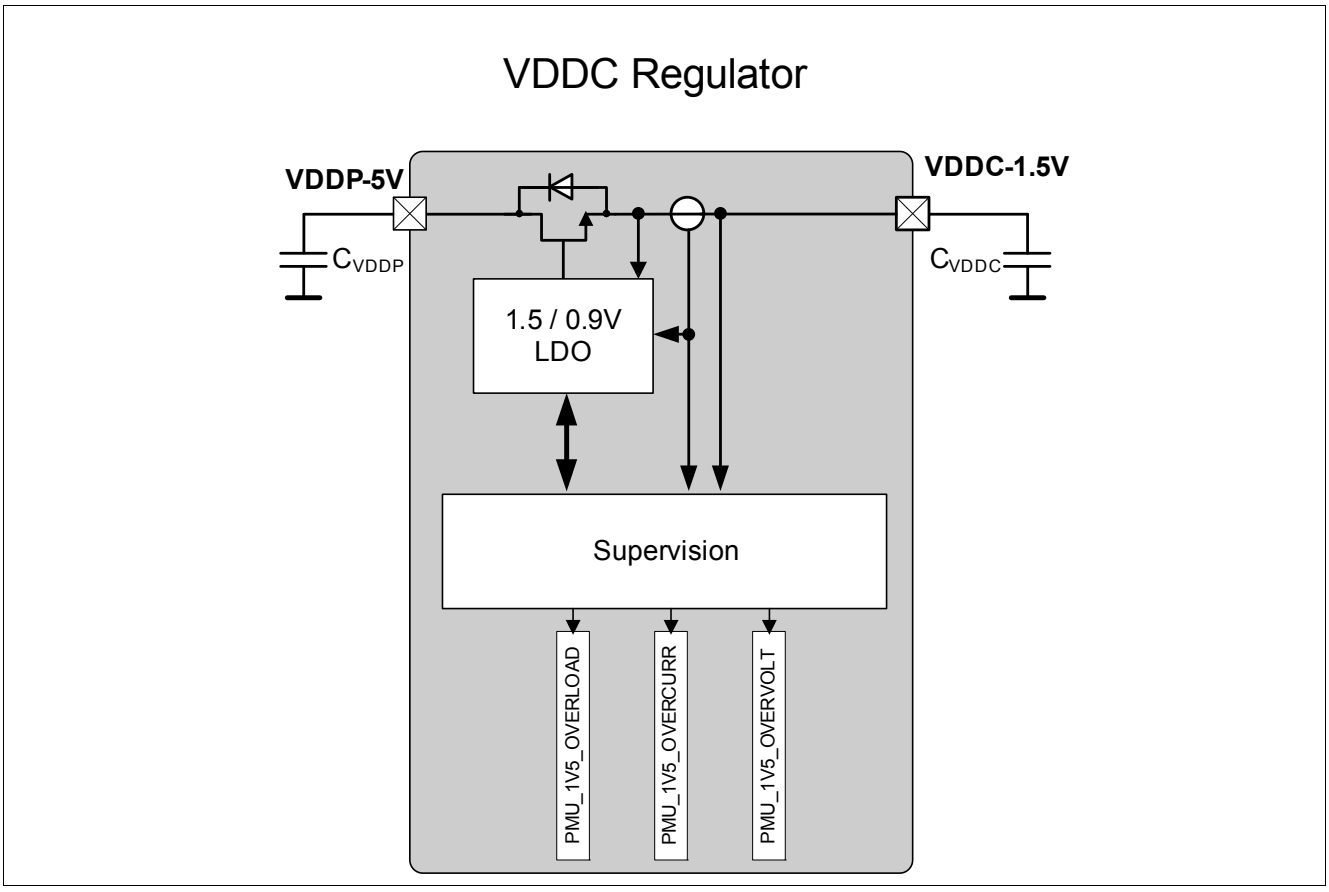

Figure 7 Module Block Diagram of VDDC Voltage Regulator

3.1.3 External Voltage Regulator 5.0V (VDDEXT)

The external voltage regulator provides 5 V output voltage in order to supply external circuitry like LEDs, hall sensors or potentiometers.

Features

- Switchable +5 V, 20 mA low-drop voltage regulator
- Switch-on overcurrent blanking time in order to drive small capacitive loads
- Short circuit robust
- Overvoltage monitoring with MCU interrupt signalling
- Undervoltage monitoring with MCU interrupt signalling
- Selectable switch-on slew-rate 0.95 V/µs max. @10 mA supply current, 10 nF capacitive load
- Pull-down current source at the output for Sleep Mode and off mode (100 µA)
- Cyclic sense option together with GPIOs

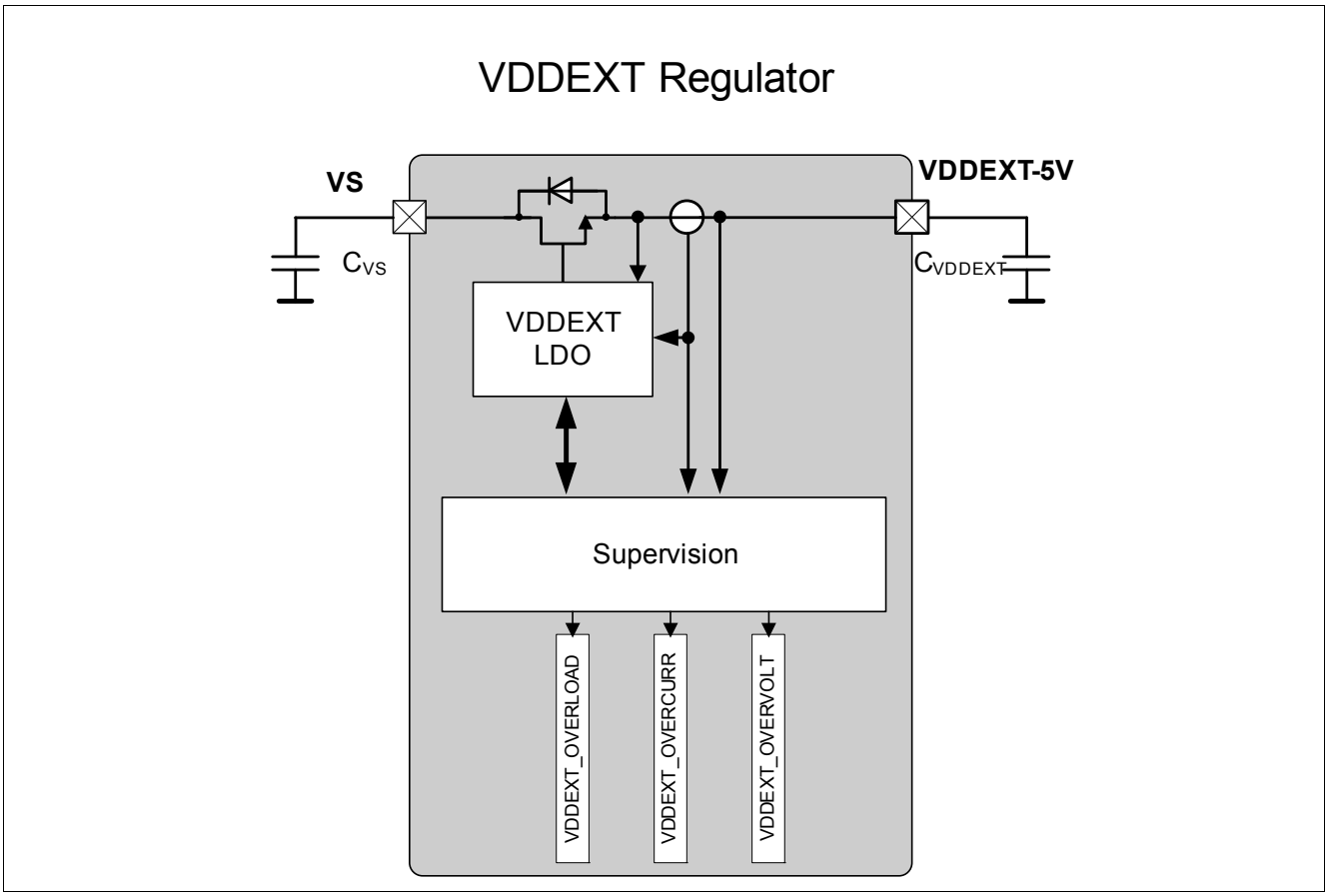

Figure 8 Module Block Diagram

3.8 Interrupt System

The TLE9834QX supports 14 interrupt vectors with four priority levels. Eleven of these interrupt vectors are assigned to the on-chip peripherals: Timer 0, Timer 1, UART, SSC and A/D Converter are each assigned to one dedicated interrupt vector; while Timer2, Timer21, MDU, LIN and the Capture/Compare Unit share six interrupt vectors.

Two interrupt vectors are assigned to the external interrupts. External interrupts 0 to 1 are each assigned to one dedicated interrupt vector, external interrupt 2 shares on interrupt vector with Timer21 and the MDU.

One interrupt vector is dedicated to the XINT interrupt events whose interrupt flags are also located in registers in XSFR area.

A non-maskable interrupt (NMI) with the highest priority is shared by the following:

- Watchdog Timer, warning before overflow
- MI_CLK Watchdog Timer overflow event
- PLL, loss of lock
- Flash, on operation complete, e.g. erase.
- OCDS, on user IRAM event
- Oscillator watchdog detection for too low oscillation of f_{OSC}
- Flash map error
- Uncorrectable ECC error on Flash, XRAM and IRAM
- VSUP supply pre warning when any supply voltage drops below or exceeds any threshold.

Figure 14, **Figure 15**, **Figure 16**, **Figure 17** and **Figure 18** give a general overview of the interrupt sources and nodes, and their corresponding control and status flags. **Figure 19** gives the corresponding overview for the NMI sources.

Figure 21 shows the structure of an input-only port pin. Each P2 pin can only function in input mode. Register P2_DIR is provided to enable or disable the input driver. When the input driver is enabled, the actual voltage level present at the port pin is translated into a logic 0 or 1 via a Schmitt-Trigger device and can be read via register. Each pin can also be programmed to activate an internal weak pull-up or pull-down device. The analog input (Analog In) bypasses the digital circuitry and Schmitt-Trigger device for direct feed-through to the ADC1 input channel.

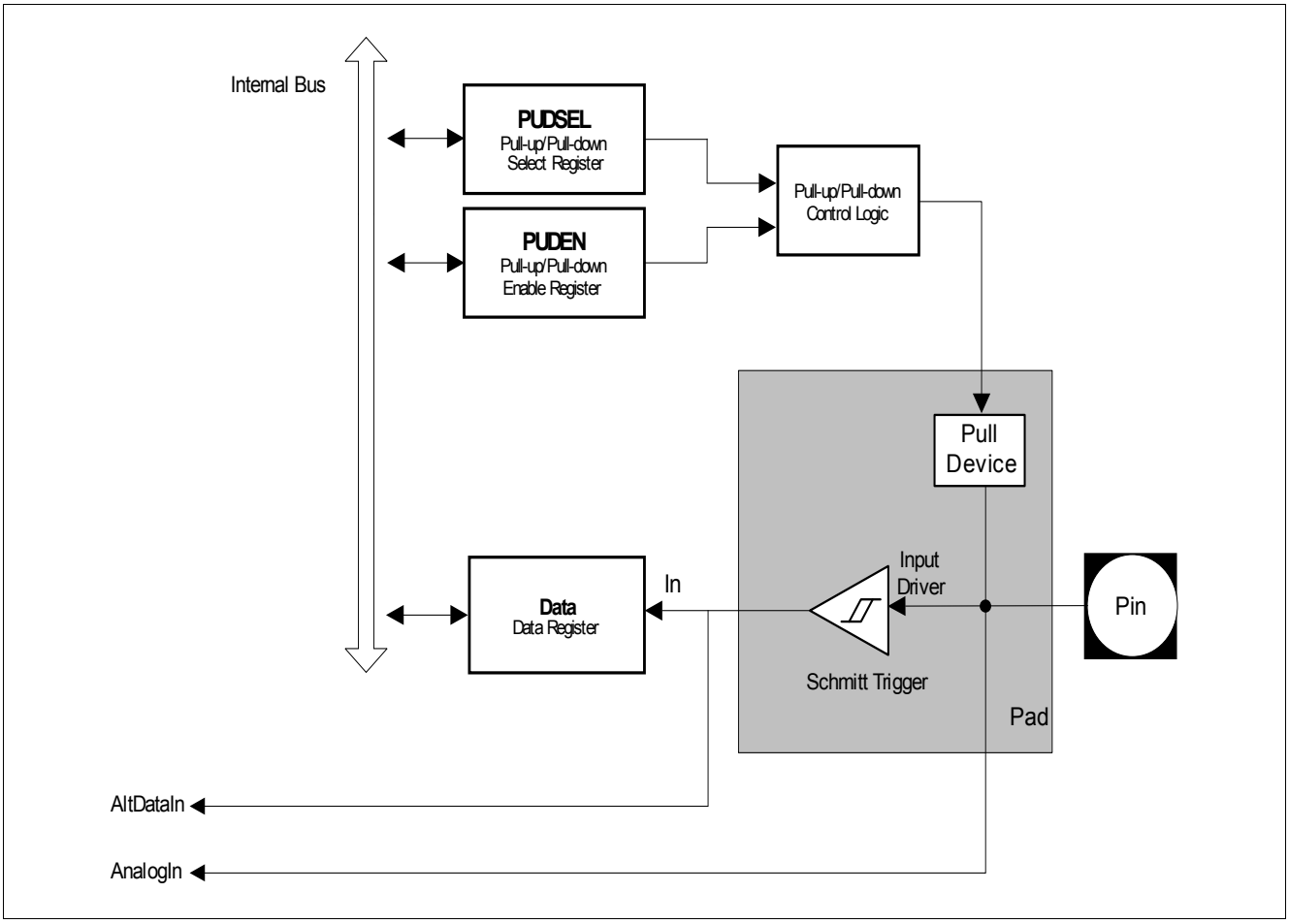

Figure 21 General Structure of an Input Port Pin

  - Programmable number of data Bits: 2 to 8 Bits
  - Programmable shift direction: LSB or MSB shift first
  - Programmable clock polarity: idle low or high state for the shift clock
  - Programmable clock/data phase: data shift with leading or trailing edge of the shift clock
- Variable baud rate
- Compatible with Serial Peripheral Interface (SPI)
- Interrupt generation
  - On a transmitter empty condition
  - On a receiver full condition
  - On an error condition (receive, phase, baud rate, transmit error)

Data is transmitted or received on lines TXD and RXD, which are normally connected to the pins MTSR (Master Transmit/Slave Receive) and MRST (Master Receive/Slave Transmit). The clock signal is output via line MS_CLK (Master Serial Shift Clock) or input via line SS_CLK (Slave Serial Shift Clock). Both lines are normally connected to the pin SCLK. Transmission and reception of data are double-buffered.

Figure 24 shows all functional relevant interfaces associated with the SSC Kernel.

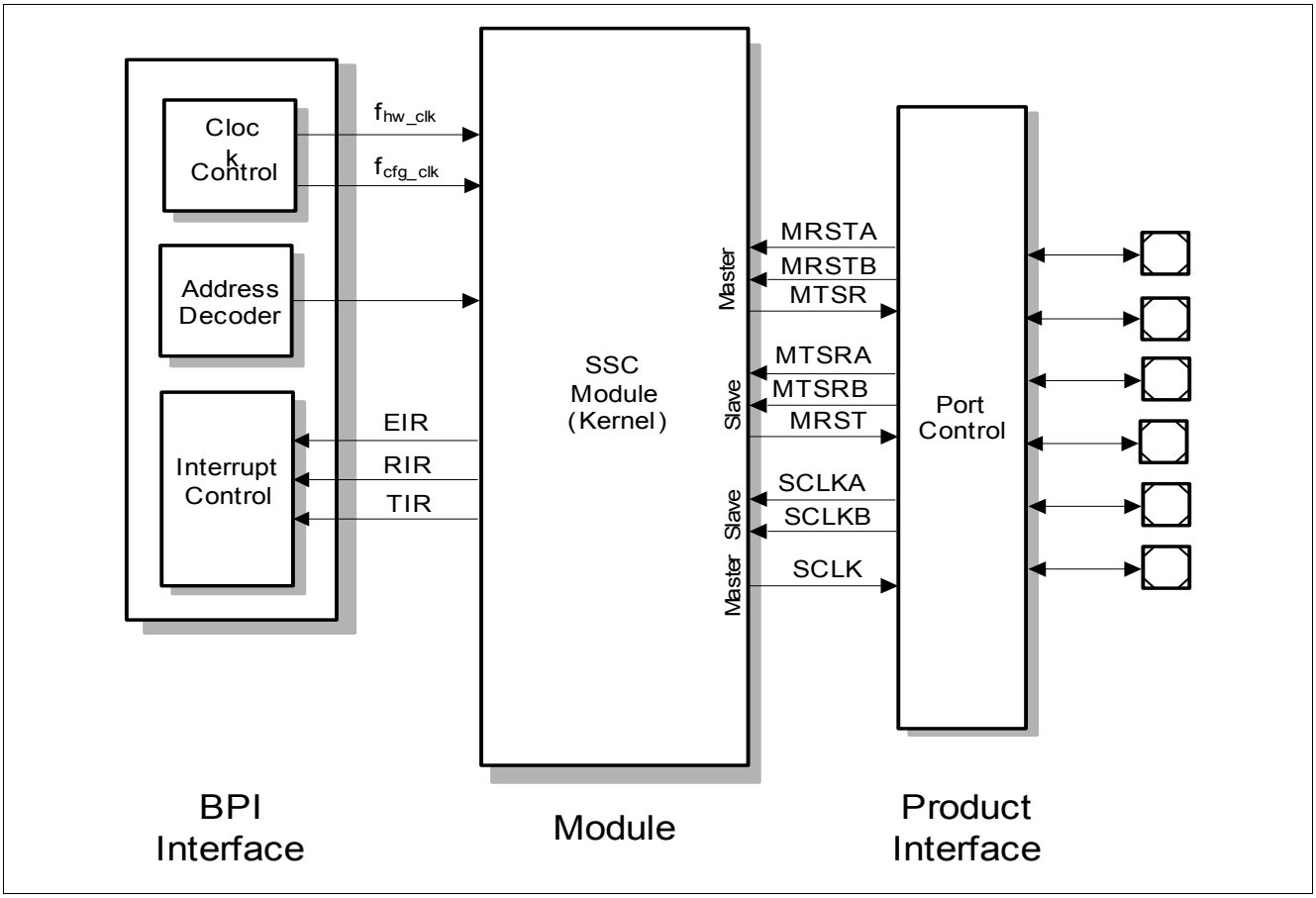

Figure 24 SSC Interface Diagram

4 Application Information

4.1 Electric Drive Application

Figure 31 shows the TLE9834QX in an electric drive application setup controlling a DC-brush motor. The two Low Side Switches are controlling a relay each. An external FET allows to control the window lift motor with a PWM signal as generated with the CCU6 module of the microcontroller.

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

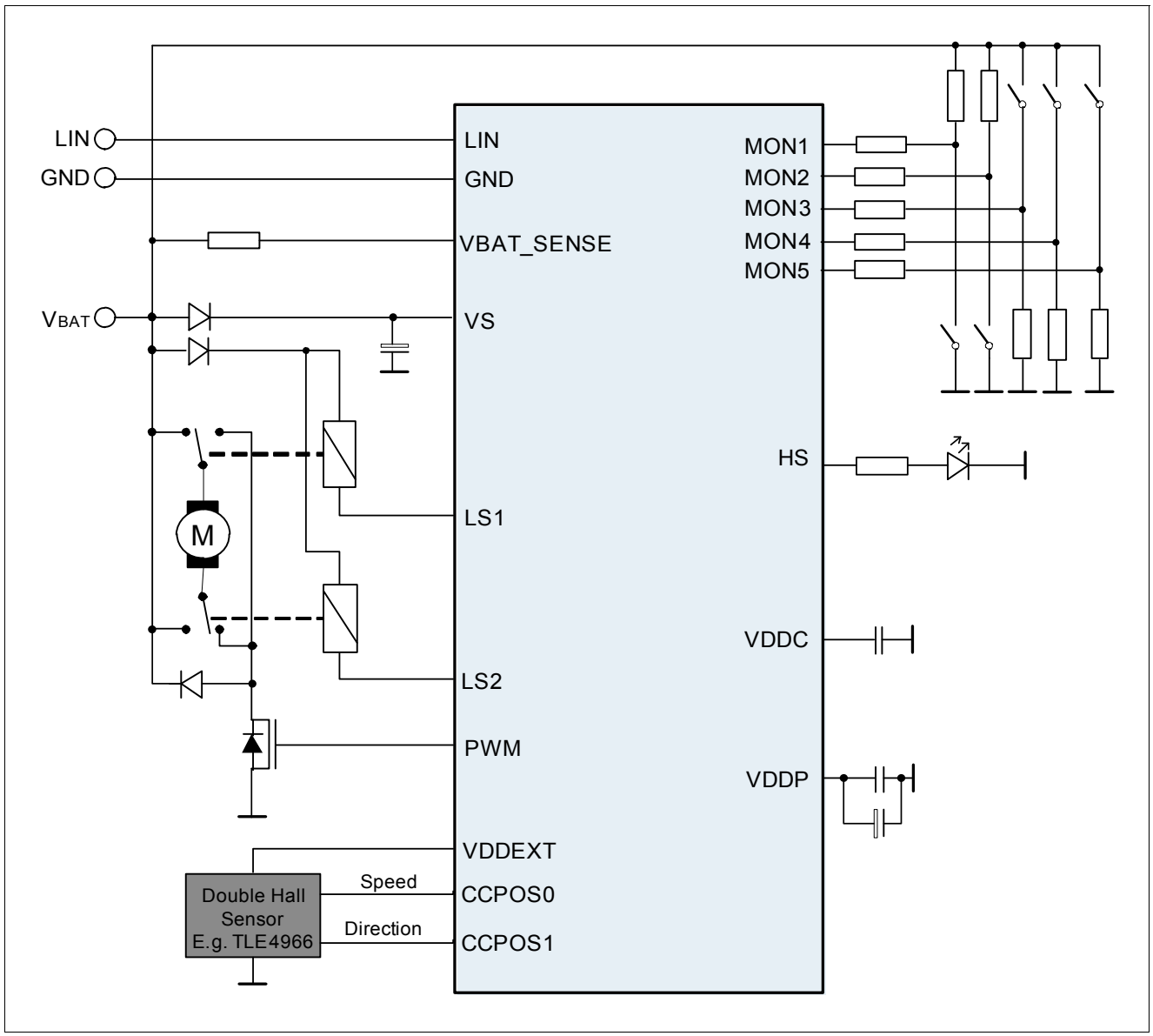

Figure 31 Simplified Application Diagram

4.2 Connection of N.C. Pins

It is recommended to connect N.C. pins to GND unless otherwise specified. Since pins 10 and 46 are located next to high voltage pins (VS, MON5, LS1) these 2 N.C. pins can be also left unconnected in order to avoid huge current flow and damage of the system in case of short-circuit.

4.3 Connection of ADCGND Pin

The ADCGND pin is chip-internal connected to reference ground. In order to provide full offset compensation and achieve full accuracy of ADC1 the ADCGND pin must not be connected to board ground. ADCGND pin should be connected with a capacitor (100 nF) to VAREF only.

4.4 Connection of Exposed Pad

It is recommended to connect the exposed pad to GND.

4.5 Voltage Regulators-Blocking Capacitors

Table 11 External Component Recommendation

Symbol	Function	Comment
C_{VS}	blocking capacitor at VS pin	> 20 µF Elco + 100 nF Ceramic, ESR < 1 Ω
C_{VDDP}	blocking capacitor at VDDP pin	1 µF typ. + 100 nF Ceramic, ESR < 1 Ω
C_{VDDEXT}	blocking capacitor at VDDEXT pin	100 nF typ., ESR < 1 Ω
C_{VDDC}	blocking capacitor at VDDC pin	> 330 nF + 100 nF Ceramic, ESR < 1 Ω
C_{VAREF}	blocking capacitor at VAREF pin	> 100 nF, ESR < 1 Ω

4.6 Additional External Components

Table 12 External Component Recommendation

Symbol	Function	Comment
C_{HSx}	HF blocking capacitor at HSx pin	6.8 nF
R_{MONx}	resistor at MONx pin	1 kΩ
$R_{VBAT\_}$	resistor at VBAT_SENSE pin	1 kΩ

5.1.3 Current Consumption

Table 16 Electrical Characteristics [1)]

V_s = 5.5V to 18V, T_J = -40°C to 85°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Current Consumption @VS pin							
Current Consumption in Active Mode	I_{Active}	–	30	40	mA	fsys = 40 MHz no loads on pins, LIN in recessive state, LS1, LS2, HS1 and HS2 off	P_5.1.25
Current consumption in Stop Mode	$I_{Powerdown}$	–	85	95	µA	microcontroller in Stop Mode, LIN recessive state, MON1-5 disabled, GPIOs open (no loads)	P_5.1.26
Current consumption in Stop Mode with cyclic sense enabled	$I_{Powerdown2}$	–	–	110	µA	microcontroller in Stop Mode, LIN recessive state, GPIOs open (no loads)	P_5.1.27
Current consumption in Sleep Mode	I_{Sleep}	–	–	25	µA	system in Sleep Mode, microcontroller not powered, LIN recessive state, MON1-5 disabled and GPIOs open (no loads)	P_5.1.28

1) Not subject to production test, specified by design.

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

5.1.4 Thermal Resistance

Table 17 Thermal Resistance

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Junction to Ambient	R_{thJA}	–	23.9	–	K/W	1)	P_5.1.29

1) EIA/JESD 52_2, FR4, 76.2 x 114.3 x 1.5 mm; 35µ Cu, 5µ Sn; 300 mm^2

5.2 Power Management Unit (PMU)

This chapter includes all electrical characteristics of the Power Management Unit

5.2.1 PMU I/O Supply Parameters VDDP

Table 19 Electrical Characteristics

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Specified Output Current	I_{VDDP}	0	–	60	mA	1)	P_5.2.1
Required Output Capacitance	C_{VDDP}	0.1	–	10	µF	1) ESR < 1Ω	P_5.2.2
Output Voltage including line regulation	V_{DDPOUT}	4.9	5.0	5.1	V	I_{load} < 90mA;Vs > 5.5V	P_5.2.3
Output Drop	$Vs_{V\ DDPout}$	–	–	+400	mV	I_{load} < 70mA; 3V < V_s < 5.5V	P_5.2.4
Dynamic Load Regulation	$V_{VDDPLOR}$	-50	–	50	mV	1) 2 ... 70mA; C=470nF; dI/dt=100mA/µs	P_5.2.5
Dynamic Line Regulation	$V_{VDDPLIR}$	-25	–	25	mV	1) V_s= 5.5 ... 20V; dV/dt=5V/µs	P_5.2.6
Power Supply Ripple Rejection	$P_{SSRVDDP}$	50	–	–	dB	1) V_s= 13.5V; f=0 ... 1KHz; Vr=2Vpp	P_5.2.7
Over Voltage Detection	V_{DDPOV}	5.05	–	5.4	V	V_s > 5.5V; Overvoltage leads to SUPPLY_NMI	P_5.2.8
Under Voltage Reset	V_{DDPUV}	2.4	–	2.7	V	V_s > 5.5V	P_5.2.9
Over Current Shutdown	I_{VDDPOC}	90	–	180	mA	–	P_5.2.10

1) Not subject to production test, specified by design

5.3 System Clocks

5.3.1 Oscillators and PLL

Table 22 Electrical Characteristics

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
PMU Oscillators (Power Management Unit)							
Frequency of LP_CLK	f_{LP_CLK1}	14	18	22	MHz	this clock is used at startup and can be used in case the PLL fails	P_5.3.1
Frequency of LP_CLK2	f_{LP_CLK2}	70	100	130	kHz	this clock is used for cyclic wake and cyclic sense	P_5.3.2
CGU Oscillator (Clock Generation Unit Microcontroller)							
Short term frequency deviation	f_{TRIMST}	-1.5%	5	+1.5%	MHz	[1] with respect to nominal configured system frequency within one LIN message (< 10ms ... 100ms)	P_5.3.3
Long term frequency deviation	f_{TRIMLT}	-3.0%	5	+3.0%	MHz	with respect to nominal configured system frequency over lifetime and temperature	P_5.3.4
CGU-OSC Start-up time	T_{OSC}	–	–	10	µs	startup time OSC from Sleep Mode and Stop Mode, power supply stable	P_5.3.5
PLL (Clock Generation Unit Microcontroller)							
VCO frequency range Mode 0	f_{VCO-0}	48	–	112	MHz	VCOSEL =”0”	P_5.3.6
VCO frequency range Mode 1	f_{VCO-1}	96	–	160	MHz	VCOSEL =”1”	P_5.3.7
Input frequency range	f_{OSC}	4	–	16	MHz	–	P_5.3.8
XTAL1 input freq. range	f_{OSC}	4	–	16	MHz	–	P_5.3.9
Output freq. range	f_{PLL}	0.04687	–	80	MHz	–	P_5.3.10
Free-running frequency Mode 0	$f_{VCOfree\_0}$	–	–	38	MHz	VCOSEL =”0”	P_5.3.11
Free-running frequency Mode 1	$f_{VCOfree\_1}$	–	–	76	MHz	VCOSEL =”1”	P_5.3.12
Input clock high/low time	$t_{high/low}$	10	–	–	ns	–	P_5.3.13
Peak period jitter	t_{jp}	-500	–	500	ps	for K=1	P_5.3.14

5.4 Flash Parameters

This chapter includes the parameters for the 64 kByte embedded flash module.

Table 24 Flash Characteristics [1)]

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Programming time per 128 Byte page	t_{PR}	–	[2)]3	3.5	ms	–	P_5.4.1
Erase time per sector/page	t_{ER}	–	[2)]4	4.5	ms	–	P_5.4.2
Data retention time	t_{RET}	20	–	–	years	1,000 erase / program cycles	P_5.4.3
Flash erase endurance for user sectors	N_{ER}	30	–	–	kcycles	Data retention time 5 years	P_5.4.4

1) Not subject for production test, specified by design

2) Programming and erase times depend on the internal Flash clock source. The control state machine needs a few system clock cycles. This requirement is only relevant for extremely low system frequencies.

Table 26 DC Characteristics

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input leakage current (all other)	I_{OZ2}	-15	–	+15	µA	T_J ≤ 150°C, 0.45 V < V_{IN} < V_{DDP}	P_5.5.12
Pull level keep current	I_{PLK}	-240	–	+240	µA	6) V_{PIN} ≥ V_{IH} (up) V_{PIN} ≤ V_{IL} (dn)	P_5.5.13
Pull level force current	I_{PLF}	-1.5	–	+1.5	mA	6) V_{PIN} ≤ V_{IL} (up) V_{PIN} ≥ V_{IH} (dn)	P_5.5.14
Pin capacitance (digital inputs/outputs)	C_{IO}	–	–	10	pF	–	P_5.5.15

1) Not subject to production test, specified by design.

2) The maximum deliverable output current of a port driver depends on the selected output driver mode. The limit for pin groups must be respected.

3) As a rule, with decreasing output current the output levels approach the respective supply level (V_{OL}→GND, V_{OH}→V_{DDP}). However, only the levels for nominal output currents are verified.

4) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage is determined by the external circuit.

5) The given values are worst-case values. In production test, this leakage current is only tested at 125°C; other values are ensured by correlation. For derating, please refer to the following descriptions:
Leakage derating depending on temperature (T_J = junction temperature [°C]):
I_{OZ} = 0.05 × $e^{(1.5 + 0.028 \times TJ)}$ [µA]. For example, at a temperature of 95°C the resulting leakage current is 3.2 µA.
Leakage derating depending on voltage level (ΔV = V_{DDP} - V_{PIN} [V]):
I_{OZ} = $I_{OZtempmax}$ - (1.6 × ΔV) [µA]
This voltage derating formula is an approximation which applies for maximum temperature.

6) Keep current: Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level: V_{PIN} ≥ V_{IH} for a pull-up; V_{PIN} ≤ V_{IL} for a pull-down.
Force current: Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device: V_{PIN} ≤ V_{IL} for a pull-up; V_{PIN}≥ V_{IH} for a pull-down.
These values apply to the fixed pull-devices in dedicated pins and to the user-selectable pull-devices in general purpose IO pins.

Table 41 Electrical Characteristics (cont'd)

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Turn OFF Delay time, PWM mode	$t_{dOff,f\text{-}LS}$	–	–	2	µs	LS_ON=0 to 0.1*Vs V_S=13.5V, R_L =270Ω	P_5.12.12
Turn OFF Rise time, PWM mode	$t_{OFFR,PWM}$	–	1	1.25	µs	V_{LS} 0.1*Vs to 0.9*Vs; V_S=13.5V, R_L =270Ω	P_5.12.13
Turn OFF Rise time, slow mode	$t_{OFFR,Slow}$	–	100	150	µs	1) V_{LS} 0.9*Vs to 0.9*Vs; V_S=13.5V, R_L =270Ω	P_5.12.14
Minimum Duty Cycle Pulse Width variation	ton_{MIN}	1.5	2	3.5	µs	ton(dig) = 2µs2)	P_5.12.15
Typical (systematic) Pulse Width increase LS_ON to VLS	$d\ ton_{TYP}$	–	1.25	–	µs	ton(dig) = 2µs2)	P_5.12.16
Zener Clamp Voltage	V_{AZ}	–	50	–	V	values are valid at T_j = 25°C	P_5.12.17
Clamping Energy (repetitive)	E_{clamp}	–	–	2	mJ	2) 1.000.000 cycles	P_5.12.18
Clamping Energy	E_{clamp}	–	–	14	mJ	2) Tstart = 25°C	P_5.12.19
Clamping Energy (single), hot	E_{clamp}	–	–	7	mJ	2) 10 cycles, Tstart = 85°C	P_5.12.20

1) Static ON mode (no PWM)

2) Not subject to production test, specified by design

6 Package Outlines

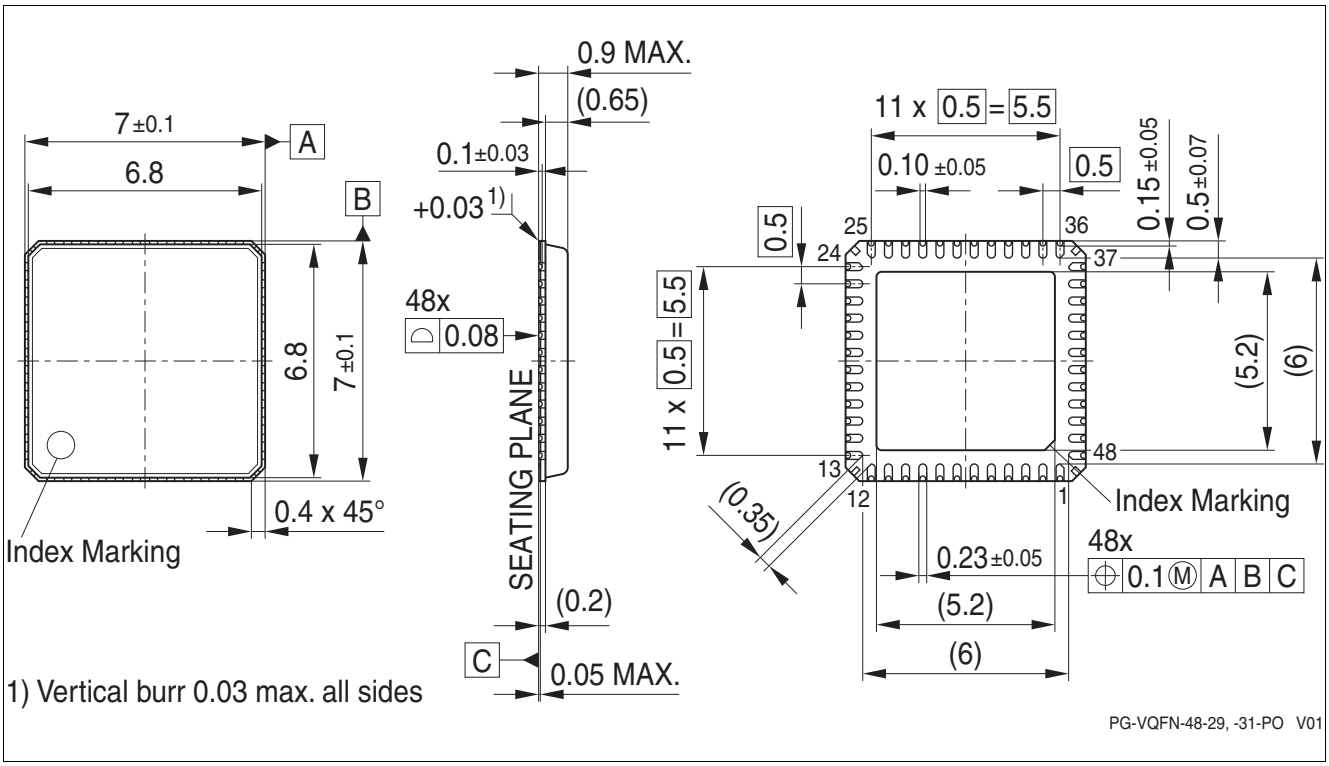

Figure 33 Package outline VQFN-48-29

Notes

1. *You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.*
2. *Dimensions in mm.*

Revision	Date	Changes
1.1	2012-03-08	**Table 14**: - Renamed Parameter “Output voltage VDDP” to “Voltage VDDP” (2x) - Renamed Parameter “Output voltage VDDC” to “Voltage VDDC”
1.1	2012-03-08	**Table 28**: Added value LIN input capacity C_{LIN_IN}

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