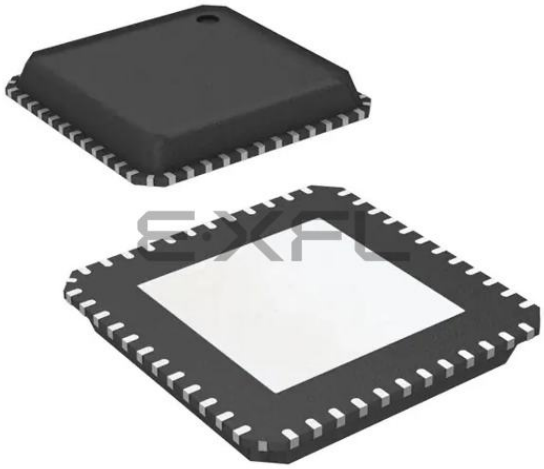

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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Automotive
Core Processor	XC800
Program Memory Type	FLASH (64kB)
Controller Series	-
RAM Size	3.25K x 8
Interface	LIN, SSI, UART
Number of I/O	11
Voltage - Supply	3V ~ 27V
Operating Temperature	-40°C ~ 150°C (TJ)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-48-29
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tle9834qxxuma2

1.2 Abbreviations

The following acronyms and terms are used within this document. List see in Table 2.

Table 2 Acronyms

Acronyms	Name
ALU	Arithmetic Logic Unit
CCU6	Capture Compare Unit 6
CGU	Clock Generation Unit
CMU	Cyclic Management Unit
DAP	Device Access Port
DPP	Data Post Processing
ECC	Error Correction Code
EEPROM	Electrically Erasable Programmable Read Only Memory
GPIO	General Purpose Input Output
FSR	Full Scale Range
ICU	Interrupt Control Unit
IRAM	Internal Random Access Memory - Internal Data Memory
LDO	Low DropOut voltage regulator
LIN	Local Interconnect Network
LSB	Least Significant Bit
MCU	Micro Controller Unit
MDU	Multiplication Division Unit
MMC	Monitor Mode Control
MSB	Most Significant Bit
NMI	Non Maskable Interrupt
OCDS	On Chip Debug Support
OTP	One Time Programmable
OSC	Oscillator
PC	Program Counter
PCU	Power Control Unit
PD	Pull Down
PGU	Power supply Generation Unit
PLL	Phase Locked Loop
PMU	Power Management Unit
PSW	Program Status Word
PU	Pull Up
PWM	Pulse Width Modulation
RAM	Random Access Memory
RCU	Reset Control Unit
RMU	Reset Management Unit

Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Type	Reset State	Function	
P2.3	36	I	I	AN3 CCPOS1_0 EXINT0_2 CTRAP_1 CC60_1	ADC1 analog input channel 3 CCU6 hall input 1 External interrupt input 0 CCU6 trap input CCU6 capture/compare channel 0 input
P2.4	32	I	I	AN4 T0_2	ADC1 analog input channel 4 Timer 0 input
P2.5	31	I	I	AN5 T1_2	ADC1 analog input channel 5 Timer 1 input
P2.7	35	I	I	AN7 CCPOS2_0 EXINT2_0 T13HR_1 CC62_1	ADC1 analog input channel 7 CCU6 hall input 2 External interrupt input 2 CCU6 timer 13 hardware run input CCU6 capture/compare channel 2 input
Power Supply					
VS	47	P	–	Battery supply input	
VDDP	44	P	–	I/O port supply (5.0 V). Do not connect external loads. For buffer and bypass capacitors.	
VDDC	42	P	–	Core supply (1.5 V during Active Mode, 0.9 V during Stop Mode). Do not connect external loads. For buffer/bypass capacitor.	
VDDEXT	45	P	–	External voltage supply output (5.0 V, 20 mA)	
LSGND	13	P	–	Low Side ground LS1, LS2	
GND	30, 43, 19, 38	P	–	Core supply ground; analog supply ground	
ADCGND	33	P	–	Analog supply ground for ADC1	
LINGND	2	P	–	LIN ground	
Monitor Inputs					
MON1	5	I	I	High Voltage Monitor Input 1	
MON2	6	I	I	High Voltage Monitor Input 2	
MON3	7	I	I	High Voltage Monitor Input 3	
MON4	8	I	I	High Voltage Monitor Input 4	
MON5	9	I	I	High Voltage Monitor Input 5	
High Side Switch / Low Side Switch Outputs					
LS1	11	O	Hi-Z	Low Side Switch output 1	
LS2	12	O	Hi-Z	Low Side Switch output 2	
HS1	3	O	Hi-Z	High Side Switch output 1	
HS2	4	O	Hi-Z	High Side Switch output 2	
LIN Interface					
LIN	1	I/O	PU	LIN bus interface input/output	

3 Functional Description

This highly integrated circuit contains analog and digital functional blocks. For system and interface control an embedded 8-Bit state-of-the-art microcontroller, compatible to the standard 8051 core with On-Chip Debug Support (OCDS), is available. For internal and external power supply purposes, on-chip low drop-out regulators are existent. An internal oscillator provides a cost effective and suitable clock in particular for LIN slave nodes. As communication interface, a LIN transceiver and several High Voltage Monitor Inputs with adjustable threshold and filters are available. Furthermore two High Side Switches (e.g. for driving LEDs or cyclic powering of switches), two Low Side Switches (e.g. for relays) and several general purpose input/outputs (GPIO) with pulse-width modulation (PWM) capabilities are available.

The Micro Controller Unit (MCU) supervision and system protection including reset feature is controlled by a programmable window watchdog. A cyclic wake-up circuit, supply voltage supervision and integrated temperature sensors are available on-chip.

All relevant modules offer power saving modes in order to support terminal 30 connected automotive applications. A wake-up from the power saving mode is possible via a LIN bus message, via the monitoring inputs, via the GPIO ports or repetitive with a programmable time period (cyclic wake-up).

The integrated circuit is available in a VQFN-48-29 package with 0.5 mm pitch and is designed to withstand the severe conditions of automotive applications.

Block Diagram

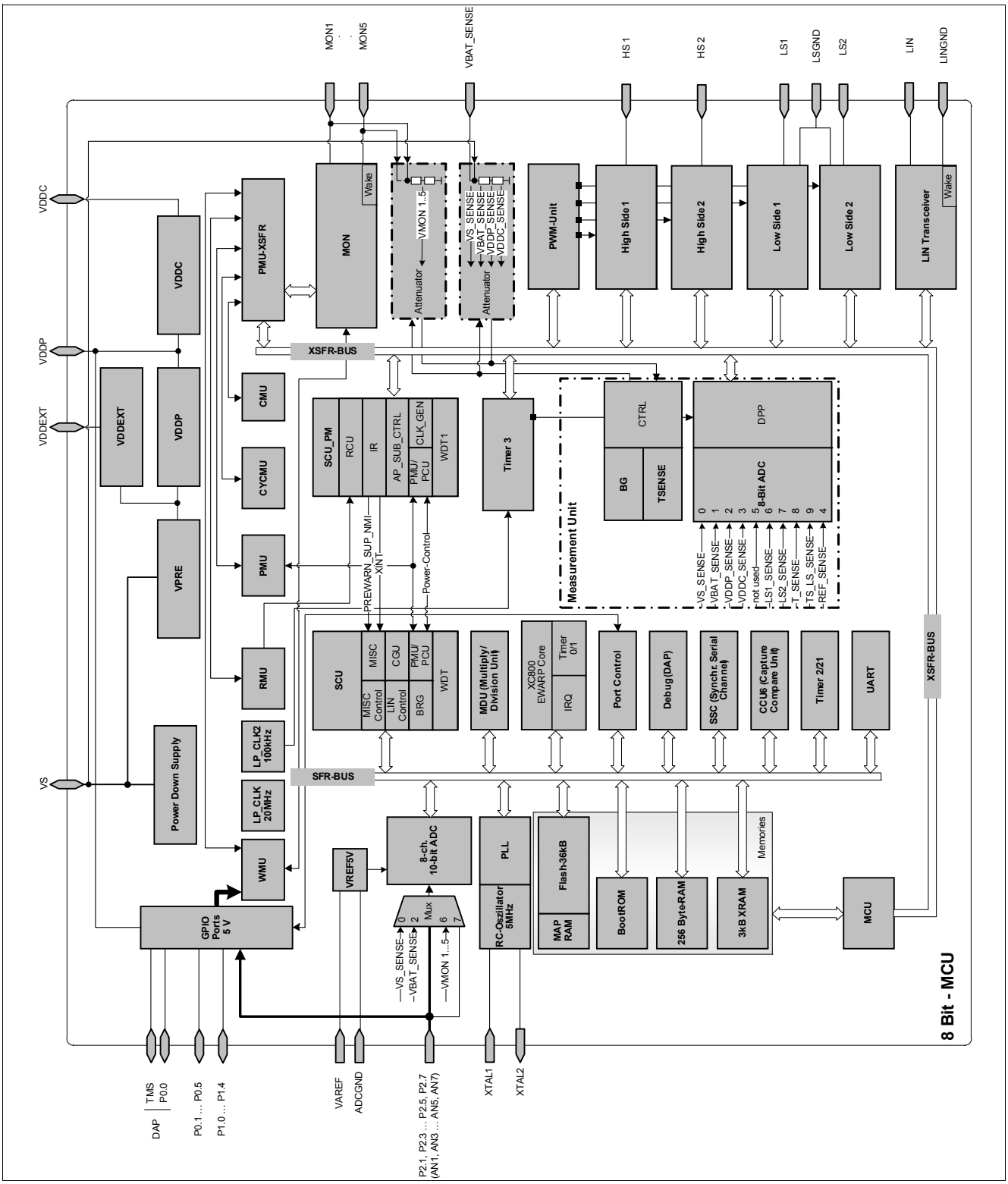


Figure 2 Block Diagram

The TLE9834QX has several operational modes mainly to support low power consumption requirements. The low power modes and state transitions are depicted in **Figure 3** below.

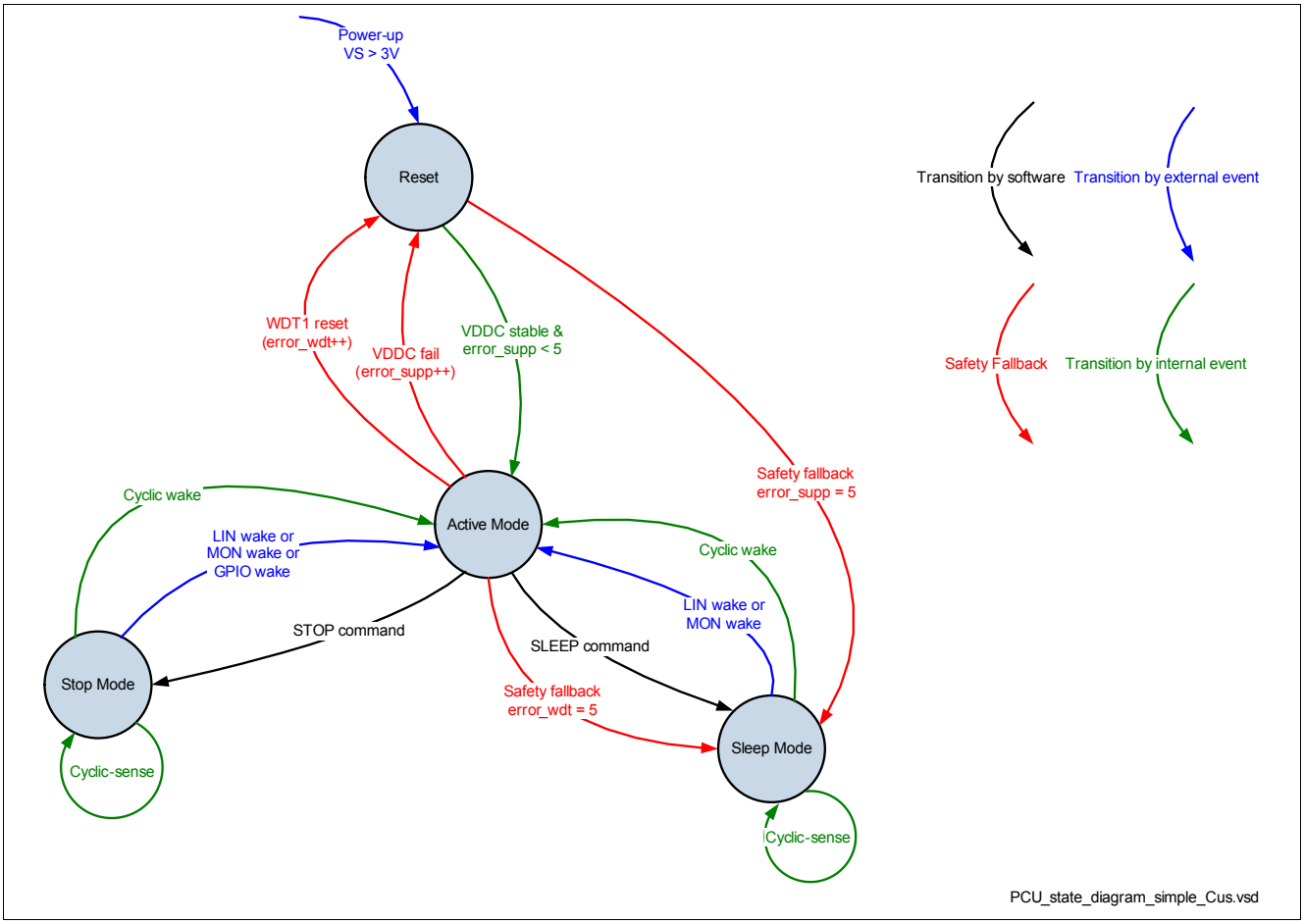


Figure 3 Power Control State Diagram

Reset Mode

The Reset Mode is a transition mode e.g. during power-up of the device after a power-on reset. In this mode the on-chip power supplies are enabled and all other modules are initialized. Once the core supply VDDC is stable, the Active Mode is entered. In case the watchdog timer WDT1 fails for more than four times, a fail-safe transition to the Sleep Mode is done.

Active Mode

In Active Mode all modules are activated and the TLE9834QX is fully operational.

Stop Mode

The Stop Mode is one out of two low power modes. The transition to the low power modes is done by setting the respective Bits in the mode control register. In Stop Mode the embedded microcontroller is still powered allowing faster wake-up reaction times. A wake-up from this mode is possible by LIN bus activity, the High Voltage Monitor Input pins or the respective 5V GPIOs.

Sleep Mode

The Sleep Mode is the second low-power mode. The transition to the low-power modes is done by setting the respective Bits in the MCU mode control register. In Sleep Mode the embedded microcontroller power supply is deactivated allowing the lowest system power consumption, but the wake-up time is longer compared to the Stop Mode. A wake-up from this mode is possible by LIN bus activity or the High Voltage Monitor Input pins. A wake-up from Sleep Mode behaves similar to a power-on reset.

Table 5 Description of PMU Submodules

Mod. Name	Modules	Functions
Power Down Supply	Independent Supply Voltage Generation for PMU	This supply is only dedicated to the PMU to ensure a independent operation of generated power supplies (VDDP, VDDC).
LP_CLK (= 20 MHz)	- Clock Source for all PMU submodules - Backup Clock Source for System - Clock Source for WDT1	This ultra low power oscillator generates the clock for the PMU. This clock is also used as backup clock for the system in case of PLL clock failure and as independent clock source for WDT1
LP_CLK2 (= 100 kHz)	Clock Source for PMU	This ultra low power oscillator generates the clock for the PMU mainly in Stop Mode and in the cyclic modes.
Peripherals	Peripheral blocks of PMU	This blocks includes all relevant peripherals to ensure a stable and fail safe PMU startup and operation
Power Supply Generation Unit (PGU)	Voltage regulators for VDDP and VDDC	This block includes the voltage regulators for the pad supply (VDDP) and the core supply (VDDC) including all diagnosis and safety features
VDDEXT (Hall Sensor Supply)	Voltage regulator for VDDEXT to supply external modules (e.g. Hall Sensors)	This voltage regulator is a dedicated supply for external modules and can also be used for cyclic sense operations (e.g. with hall sensor)
PMU-XSFR	All PMU relevant Extended Special Function Registers	This module contains all PMU relevant registers, which are needed to control and monitor the PMU.
PMU-PCU	Power Control Unit of the PMU	This block is responsible for controlling all power related actions within the PGU Module.
PMU-WMU	Wake-up Management Unit of the PMU	This block is responsible for controlling all wake-up related actions within the PMU Module.
PMU-CYCMU	Cyclic Management Unit of the PMU	This block is responsible for controlling all actions within cyclic mode.
PMU-CMU	Clock Management Unit of the PMU	This block is responsible for controlling all clocking actions within the PMU.
PMU-RMU	Reset Management Unit of the PMU	This block is responsible for generating all system required resets.

3.1.2 Voltage Regulator 1.5V (VDDC)

This module represents the 1.5 V voltage regulator, which serves as core supply for the 8-bit µC and other chip internal analog 1.5 V functions (e.g. 8 Bit ADC). To further reduce the current consumption of the 8-bit MCU during Stop Mode the output voltage is optionally reduced to 0.9 V.

Features

- 1.5 V low-drop voltage regulator
- Optional 0.9 V in Stop Mode
- Current limitation
- Overcurrent monitoring and shutdown with MCU signalling (interrupt)
- Overvoltage monitoring with MCU signalling (interrupt)
- Undervoltage monitoring with MCU signalling (interrupt)
- Pull-down current source at the output for Sleep Mode (100 µA)

The output capacitor C_{VDDC} is mandatory to ensure a proper regulator functionality.

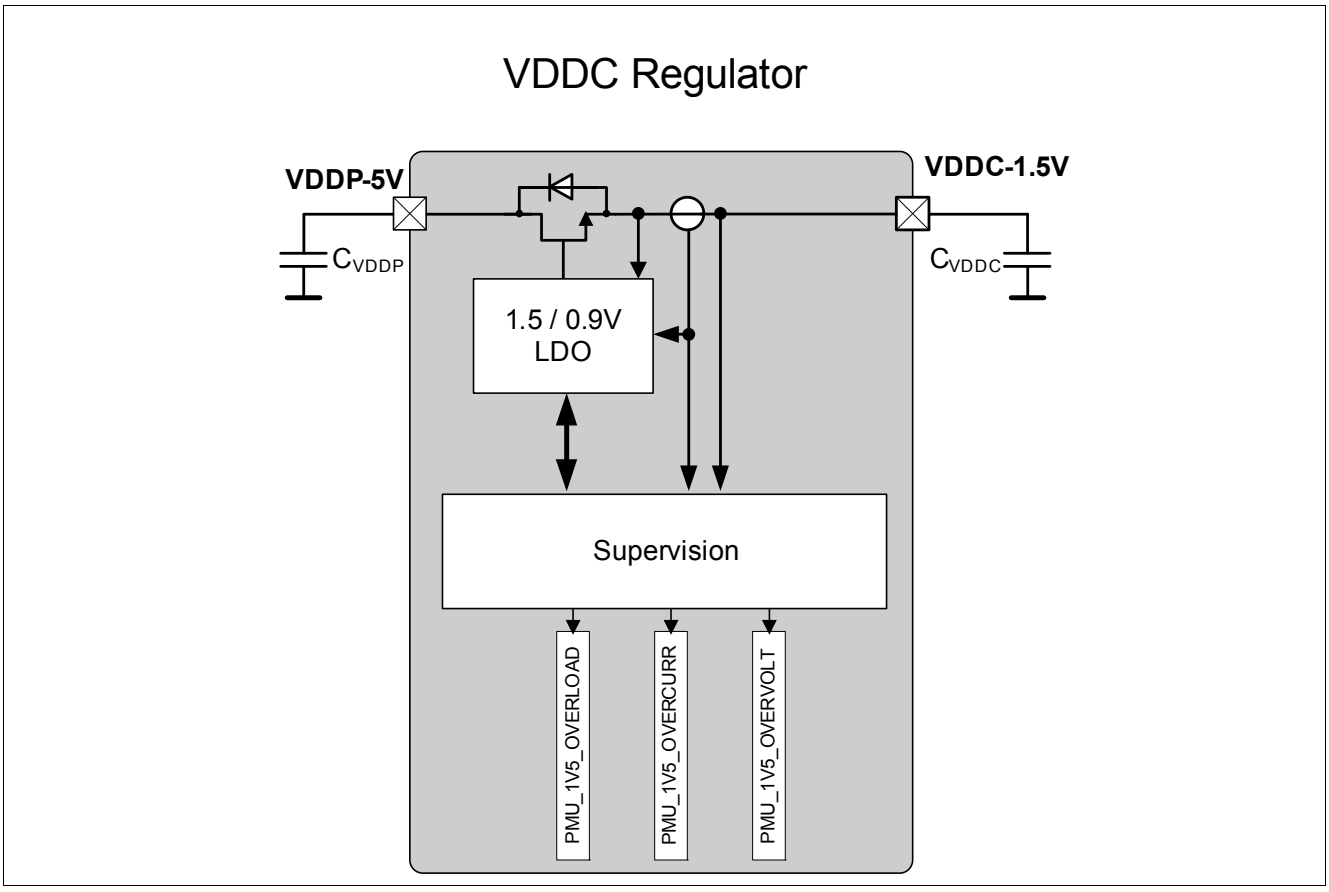


Figure 7 Module Block Diagram of VDDC Voltage Regulator

3.1.3 External Voltage Regulator 5.0V (VDDEXT)

The external voltage regulator provides 5 V output voltage in order to supply external circuitry like LEDs, hall sensors or potentiometers.

Features

- Switchable +5 V, 20 mA low-drop voltage regulator
- Switch-on overcurrent blanking time in order to drive small capacitive loads
- Short circuit robust
- Overvoltage monitoring with MCU interrupt signalling
- Undervoltage monitoring with MCU interrupt signalling
- Selectable switch-on slew-rate 0.95 V/µs max. @10 mA supply current, 10 nF capacitive load
- Pull-down current source at the output for Sleep Mode and off mode (100 µA)
- Cyclic sense option together with GPIOs

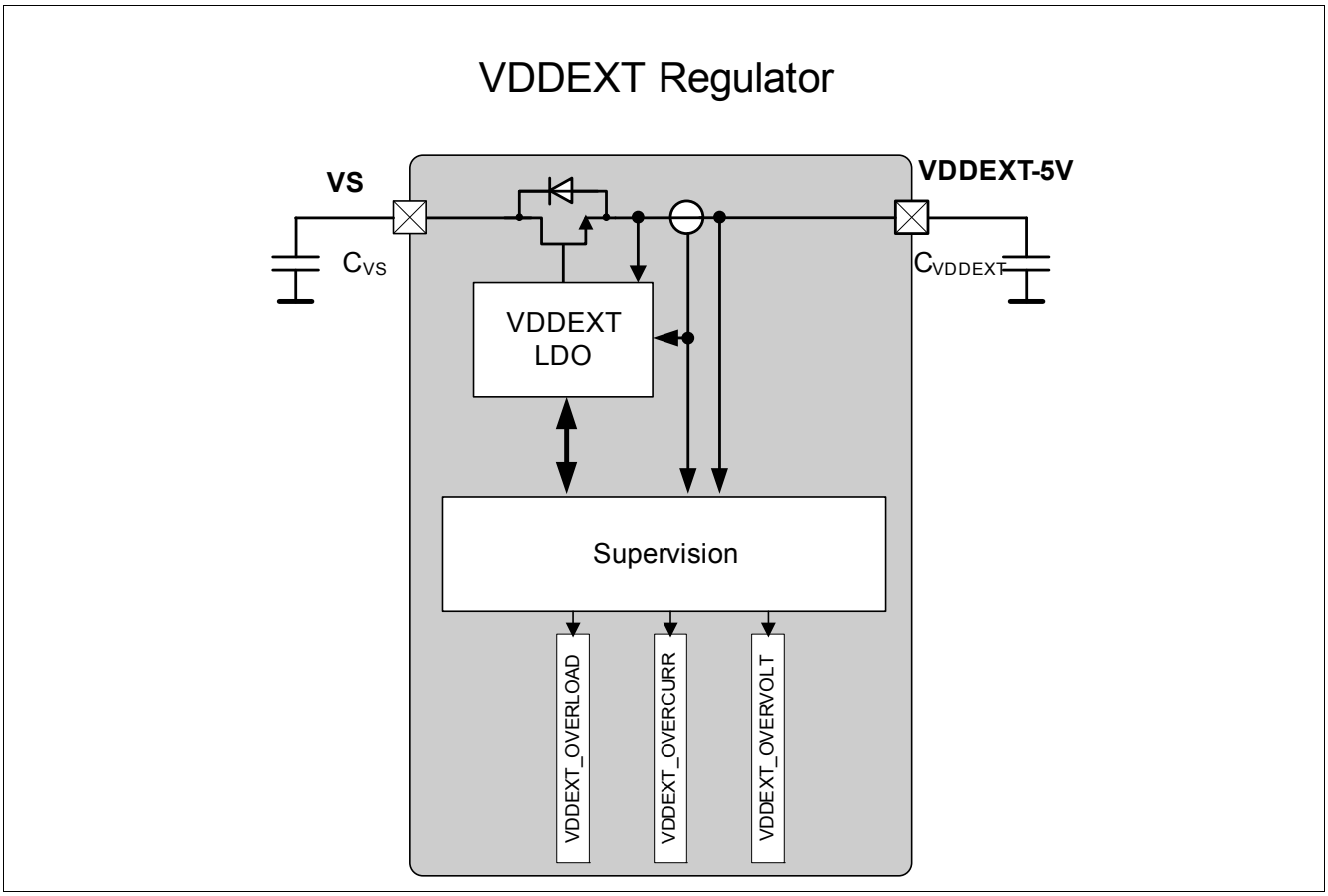


Figure 8 Module Block Diagram

Figure 10 shows the functional blocks of the XC800 Core. The XC800 Core consists mainly of the instruction decoder, the arithmetic section, the program control section, the access control section, and the interrupt controller.

The instruction decoder decodes each instruction and accordingly generates the internal signals required to control the functions of the individual units within the core. These internal signals have an effect on the source and destination of data transfers and control the ALU processing.

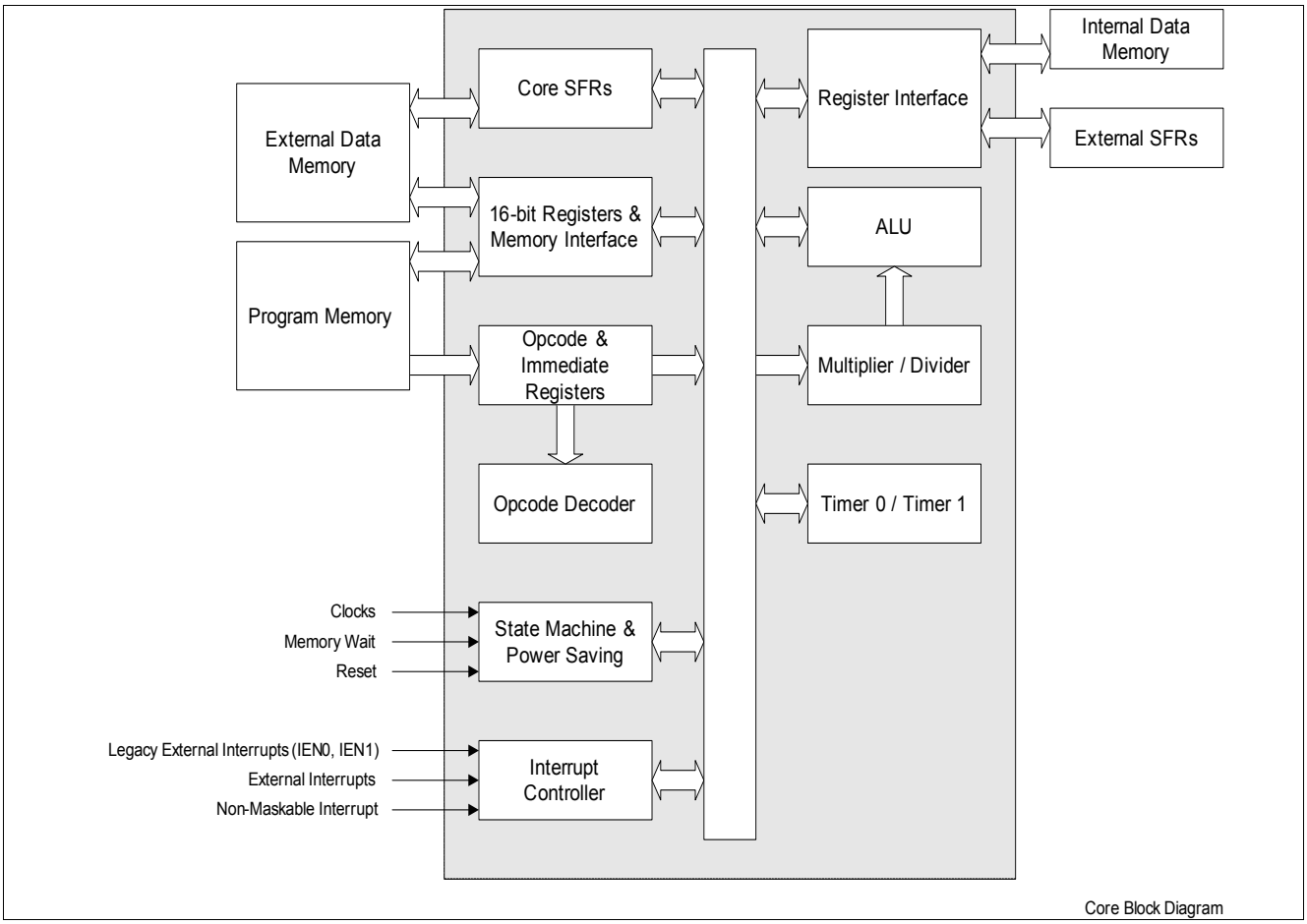


Figure 10 XC800 Core Block Diagram

The arithmetic section of the processor performs extensive data manipulation and consists of the arithmetic/logic unit (ALU), A register, B register and PSW register. The ALU accepts 8-Bit data words from one or two sources and generates an 8-Bit result under the control of the instruction decoder. The ALU performs both arithmetic and logic operations. Arithmetic operations include add, subtract, multiply, divide, increment, decrement, BCD-decimal-add-adjust and compare. Logic operations include AND, OR, Exclusive OR, complement and rotate (right, left or swap nibble (left four)). Also included is a Boolean unit performing the Bit operations as set, clear, complement, jump-if-set, jump-if-not-set, jump-if-set-and-clear and move to/from carry. The ALU can perform the Bit operations of logical AND or logical OR between any addressable Bit (or its complement) and the carry flag, and place the new result in the carry flag.

The program control section controls the sequence in which the instructions stored in program memory are executed. The 16-Bit program counter (PC) holds the address of the next instruction to be executed. The conditional branch logic enables internal and external events to the processor to cause a change in the program execution sequence.

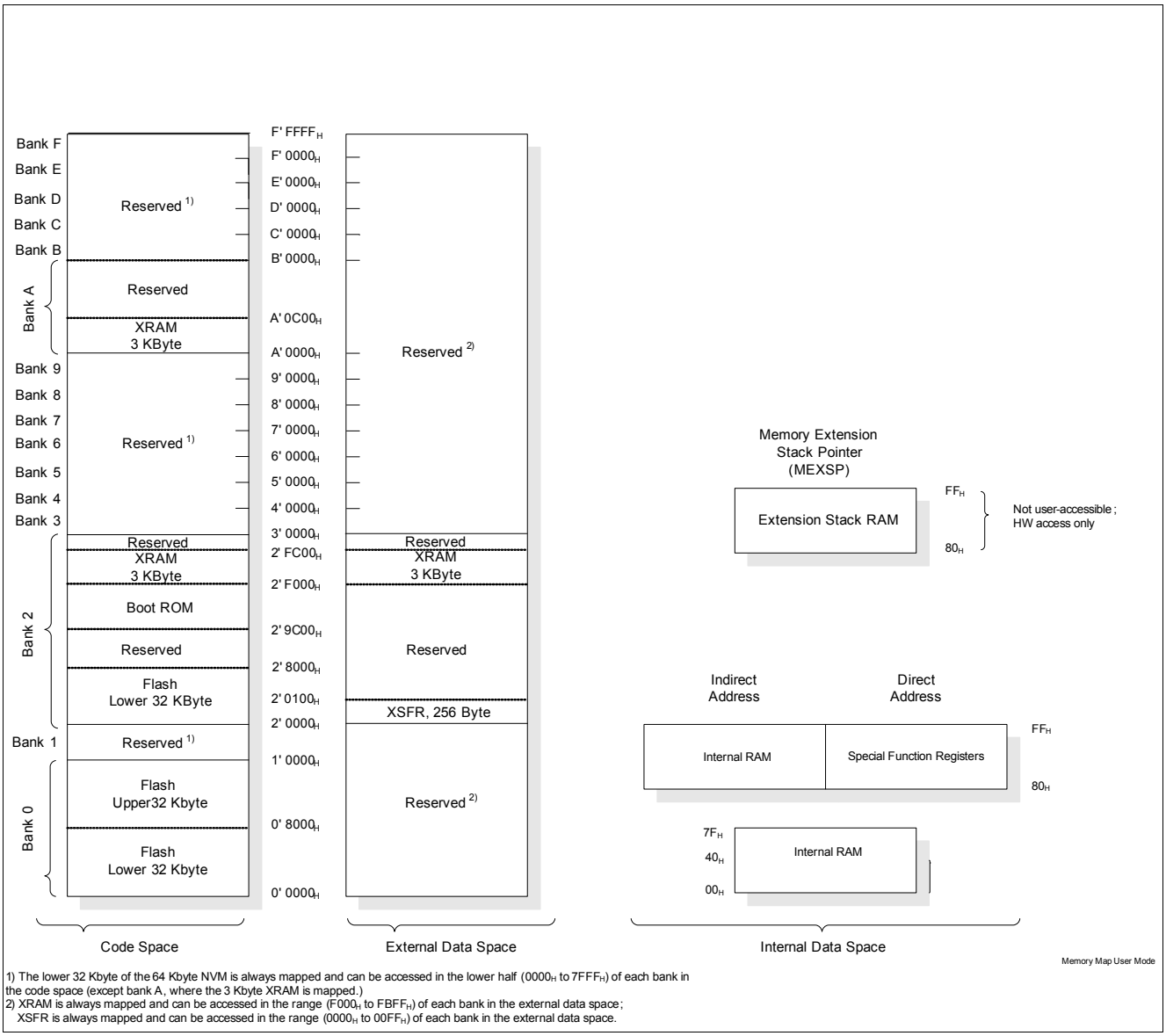
The access control unit is responsible for the selection of the on-chip memory resources. The interrupt requests from the peripheral units are handled by the interrupt controller unit.

3.4 Memory Architecture

The TLE9834QX CPU manipulates operands in the following memory spaces:

- 64 kByte of Flash memory in code space
- BootROM memory in code space
- 256 Byte of internal RAM data memory in internal data space
- 3 kByte of XRAM memory in code space and external data space (XRAM can be read/written as program memory or external data memory)
- 128 Byte of special function registers SFR in internal data space
- 256 Byte of special function registers XSFR in external data space.

Figure 11 illustrates the memory address spaces of the TLE9834QX.



1) The lower 32 Kbyte of the 64 Kbyte NVM is always mapped and can be accessed in the lower half (0000_H to $7FFF_H$) of each bank in the code space (except bank A, where the 3 Kbyte XRAM is mapped.)
2) XRAM is always mapped and can be accessed in the range ($F000_H$ to $FBFF_H$) of each bank in the external data space; XSFR is always mapped and can be accessed in the range (0000_H to $00FF_H$) of each bank in the external data space.

Figure 11 TLE9834QX Memory Map

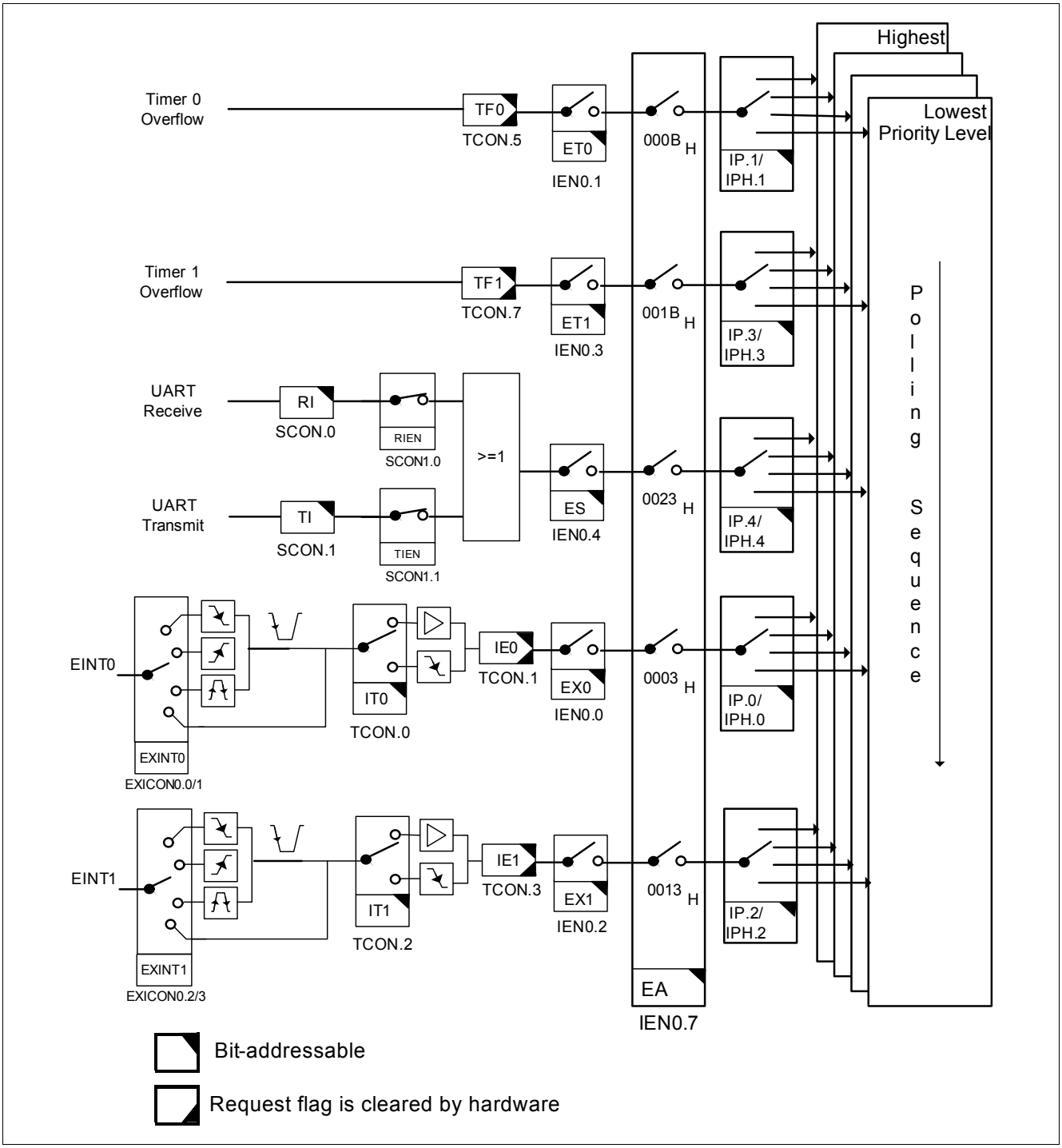


Figure 14 Interrupt Request Sources (Part 1)

3.16 LIN Transceiver

The LIN module is a transceiver for the Local Interconnect Network (LIN) compliant to the standards LIN 1.3, LIN 2.0 and LIN 2.1. It operates as a bus driver between the protocol controller and the physical network. The LIN bus is a single wire, bi-directional bus typically used for in-vehicle networks, using baud rates between 2.4 kbps and 20 kbps. Additionally baud rates up to 40 kBaud are implemented.

The LIN module offers several different operation modes, including a Sleep Mode and the normal operation mode. The integrated slope control allows to use several data transmission rates with optimized EMC performance. For data transfer at the end of line, a Flash Mode up to 115 kBaud is also implemented.

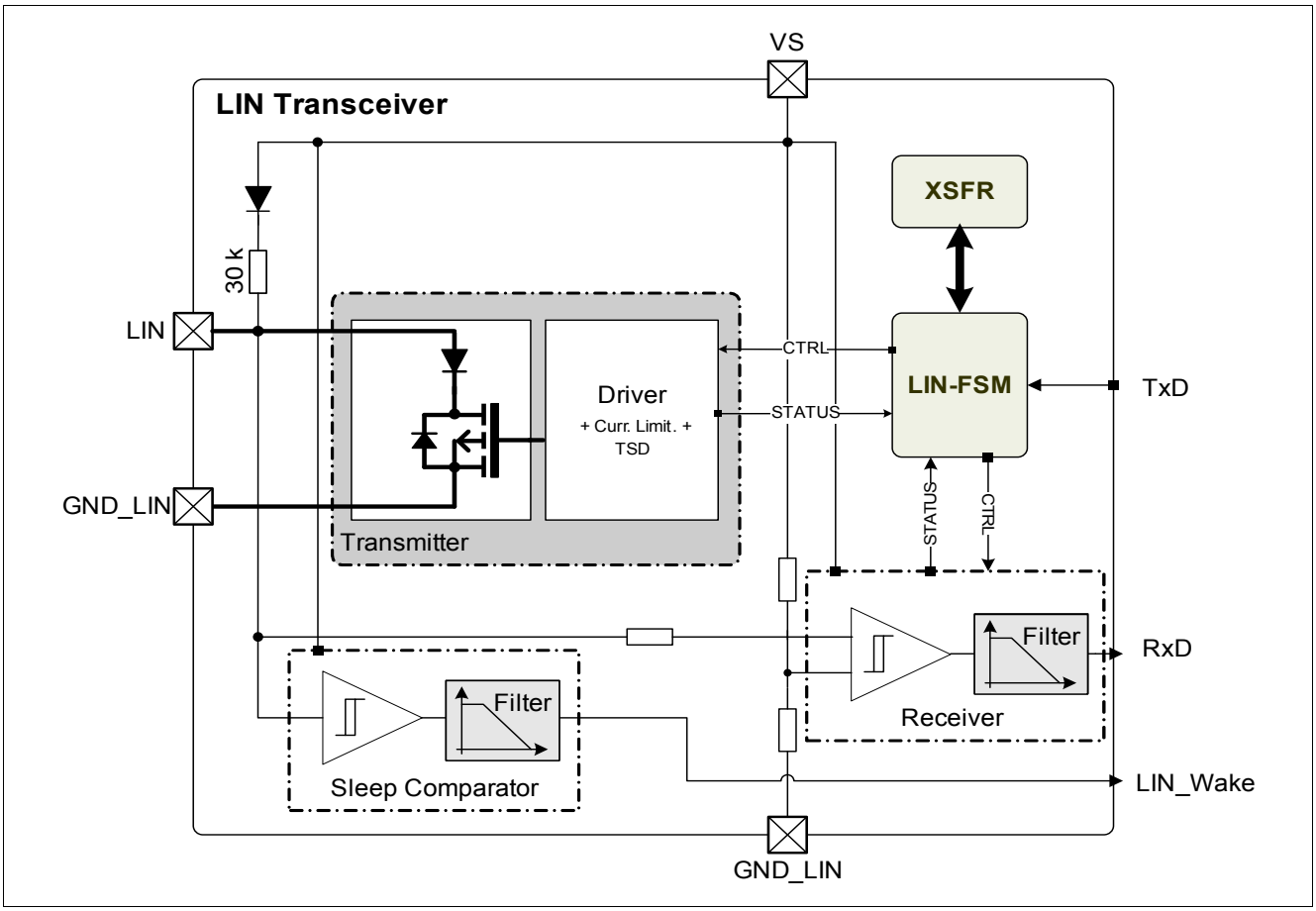


Figure 23 LIN Transceiver Block Diagram

3.17 High-Speed Synchronous Serial Interface

The High-Speed Synchronous Serial Interface (SSC) supports full-duplex and half-duplex synchronous communication. The serial clock signal can be generated by the SSC internally (master mode), using its own 16-Bit baud-rate generator, or can be received from an external master (slave mode). Data width, shift direction, clock polarity and phase are programmable. This allows communication with SPI-compatible devices or devices using other synchronous serial interfaces.

Features

- Master and slave mode operation
  - Full-duplex or half-duplex operation
- Transmit and receive buffered
- Flexible data format

  - Programmable number of data Bits: 2 to 8 Bits
  - Programmable shift direction: LSB or MSB shift first
  - Programmable clock polarity: idle low or high state for the shift clock
  - Programmable clock/data phase: data shift with leading or trailing edge of the shift clock
- Variable baud rate
- Compatible with Serial Peripheral Interface (SPI)
- Interrupt generation
  - On a transmitter empty condition
  - On a receiver full condition
  - On an error condition (receive, phase, baud rate, transmit error)

Data is transmitted or received on lines TXD and RXD, which are normally connected to the pins MTSR (Master Transmit/Slave Receive) and MRST (Master Receive/Slave Transmit). The clock signal is output via line MS_CLK (Master Serial Shift Clock) or input via line SS_CLK (Slave Serial Shift Clock). Both lines are normally connected to the pin SCLK. Transmission and reception of data are double-buffered.

Figure 24 shows all functional relevant interfaces associated with the SSC Kernel.

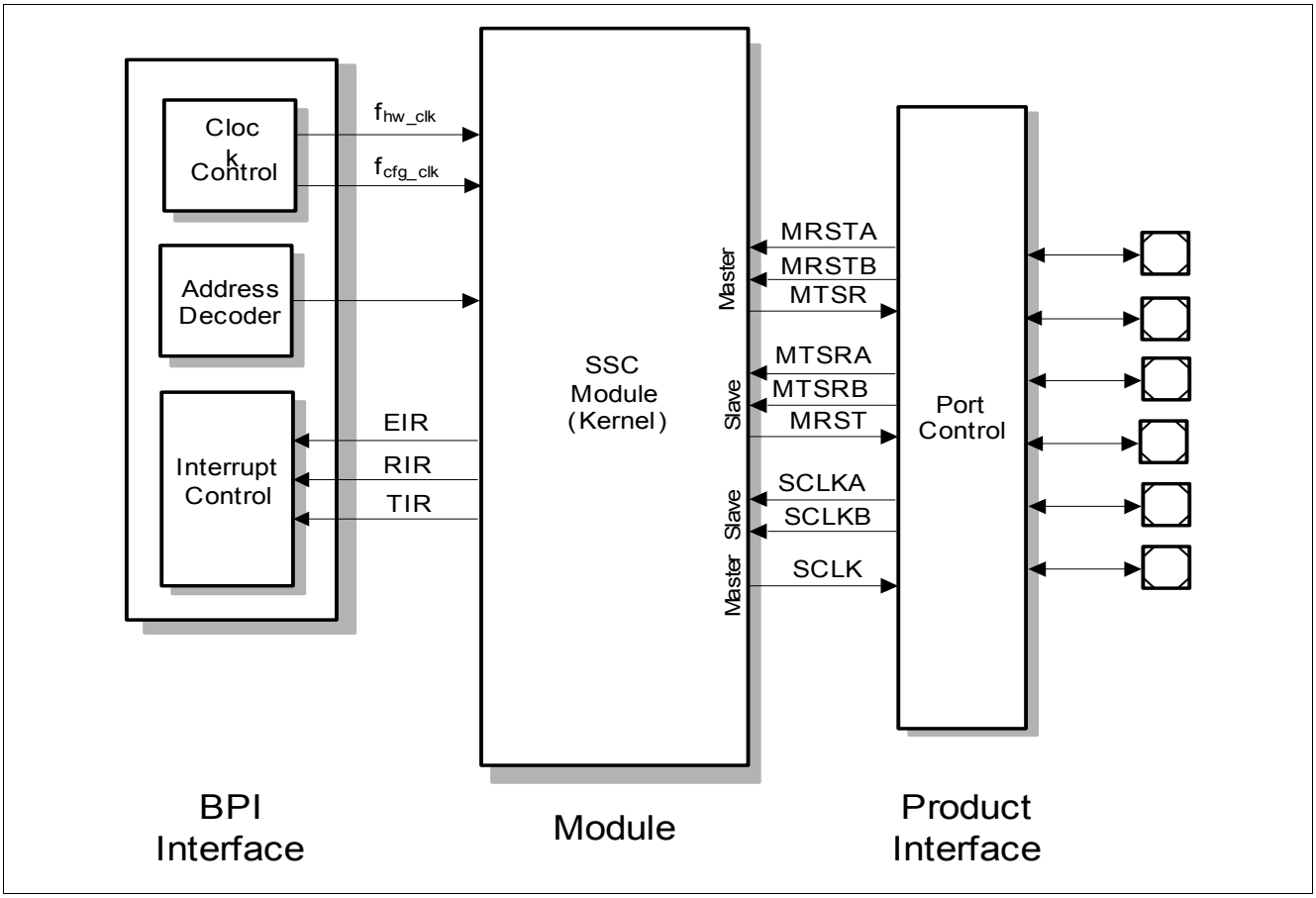


Figure 24 SSC Interface Diagram

5.2.2 PMU Core Supply Parameters VDDC

Table 20 Electrical Characteristics

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Specified Output Current	I_{VDDC}	0	–	30	mA	1) only used as internal core supply	P_5.2.11
Required Output Capacitance	C_{VDDC}	0.1	–	10	µF	2) ESR < 1Ω	P_5.2.12
Output Voltage including line regulation @ Active Mode	V_{DDCOUT}	1.44	1.5	1.56	V	I_{load} < 40mA	P_5.2.13
Output Voltage including line regulation @ Stop Mode	V_{DDCOUT}	0.89	0.95	1.15	V	I_{load} < 200µA	P_5.2.14
Dynamic Load Regulation	V_{DDCLOR}	-50	–	50	mV	2) 2 ... 30mA; C=330nF; dI/dt=100mA/µs	P_5.2.15
Dynamic Line Regulation	V_{DDCLIR}	-25	–	25	mV	2) V_{DDP}= 2.5 ... 5.5V; dV/dt=5V/µs	P_5.2.16
Over Voltage Detection	V_{DDCOV}	1.61	–	1.68	V	Overvoltage leads to SUPPLY_NMI	P_5.2.17
Under Voltage Reset	V_{DDVUV}	1.10	–	1.19	V	–	P_5.2.18
Over Current Shutdown	I_{VDDCOC}	35	–	80	mA	–	P_5.2.19

1) VDDC is not intended to be used as external voltage regulator

2) Not subject to production test, specified by design

5.2.3 VDDEXT Voltage Regulator 5.0V

Table 21 Electrical Characteristics

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Output Current	I_{VDDEXT}	0	–	20	mA	1)	P_5.2.20
Output Capacitance	C_{VDDEXT}	10	–	1000	nF	1) ESR < 1 Ω	P_5.2.21
Output Voltage including line regulation	V_{DDEXT}	4.9	5.0	5.1	V	I_{load} < 20mA;Vs > 5.5V	P_5.2.22
Output Drop	V_s-V_{DDEXT}		–	+400	mV	1) I_{load} < 20mA; 3V < V_s < 5.5V	P_5.2.23
Dynamic Load Regulation	$V_{DDEXTLOR}$	-50	–	50	mV	1) 2 ... 20mA; C=10nF; dI/dt=10mA/µs	P_5.2.24
Dynamic Line Regulation	$V_{VDDEXTLIR}$	-25	–	25	mV	V_s= 5.5 ... 20V; dV/dt=5V/µs	P_5.2.25
Power Supply Ripple Rejection1)	$P_{SSRVDDEXT}$	50	–	–	dB	V_s= 13.5V; f=0 ... 1KHz; V_r=2Vpp	P_5.2.26
Over Voltage Detection	$V_{VDDEXTOV}$	5.05	–	5.4	V	V_s > 5.5V	P_5.2.27
Under Voltage Detection	$V_{VDDEXTUV}$	2.6	–	2.9	V	2)V_s > 3.0V	P_5.2.28
Over Current Diagnostic	$I_{VDDEXTOC}$	25	–	70	mA	–	P_5.2.29

1) Not subject to production test, specified by design

2) When the condition is met, the Bit VDDEXT_CTRL.VDDEXT_SHORT will be set

5.3 System Clocks

5.3.1 Oscillators and PLL

Table 22 Electrical Characteristics

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
PMU Oscillators (Power Management Unit)							
Frequency of LP_CLK	f_{LP_CLK1}	14	18	22	MHz	this clock is used at startup and can be used in case the PLL fails	P_5.3.1
Frequency of LP_CLK2	f_{LP_CLK2}	70	100	130	kHz	this clock is used for cyclic wake and cyclic sense	P_5.3.2
CGU Oscillator (Clock Generation Unit Microcontroller)							
Short term frequency deviation	f_{TRIMST}	-1.5%	5	+1.5%	MHz	[1] with respect to nominal configured system frequency within one LIN message (< 10ms ... 100ms)	P_5.3.3
Long term frequency deviation	f_{TRIMLT}	-3.0%	5	+3.0%	MHz	with respect to nominal configured system frequency over lifetime and temperature	P_5.3.4
CGU-OSC Start-up time	T_{OSC}	–	–	10	µs	startup time OSC from Sleep Mode and Stop Mode, power supply stable	P_5.3.5
PLL (Clock Generation Unit Microcontroller)							
VCO frequency range Mode 0	f_{VCO-0}	48	–	112	MHz	VCOSEL =”0”	P_5.3.6
VCO frequency range Mode 1	f_{VCO-1}	96	–	160	MHz	VCOSEL =”1”	P_5.3.7
Input frequency range	f_{OSC}	4	–	16	MHz	–	P_5.3.8
XTAL1 input freq. range	f_{OSC}	4	–	16	MHz	–	P_5.3.9
Output freq. range	f_{PLL}	0.04687	–	80	MHz	–	P_5.3.10
Free-running frequency Mode 0	$f_{VCOfree\_0}$	–	–	38	MHz	VCOSEL =”0”	P_5.3.11
Free-running frequency Mode 1	$f_{VCOfree\_1}$	–	–	76	MHz	VCOSEL =”1”	P_5.3.12
Input clock high/low time	$t_{high/low}$	10	–	–	ns	–	P_5.3.13
Peak period jitter	t_{jp}	-500	–	500	ps	for K=1	P_5.3.14

Table 27 Current Limits for Port Output Drivers[1)]

Port Output Driver Mode	Maximum Output Current (I_{OLmax} , - I_{OHmax})		Nominal Output Current (I_{OLnom} , - I_{OHnom})		Number
	VDDP ≥ 4.5V	VDDP < 4.5V	VDDP ≥ 4.5V	VDDP < 4.5V	
Strong Driver	7.5 mA	7.5 mA	2.5 mA	2.5 mA	P_5.5.16
Medium Driver	4 mA	2.5 mA	1.0 mA	1.0 mA	P_5.5.17
Weak Driver	0.5 mA	0.5 mA	0.1 mA	0.1 mA	P_5.5.18

1) Not subject to production test, specified by design.

Note: Stresses above the values listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for an extended time may affect device reliability.
During absolute maximum rating overload conditions (V_{IN} > V_{DDP} or V_{IN} < GND) the voltage on V_{DDP} pins with respect to ground (GND) must not exceed the values defined by the absolute maximum ratings.

5.9.2 Analog/Digital Converter Parameters

These parameters describe the conditions for optimum ADC performance.

Note: Operating Conditions apply.

Table 36 A/D Converter Characteristics

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Analog reference supply	V_{AREFSR}	V_{AGND} + 1.0	–	V_{DDPA} + 0.05	V	1)	P_5.9.7
Analog reference ground	V_{AGNDSR}	GND - 0.05	–	1.5	V	2)	P_5.9.8
Analog input voltage range	V_{AIN}	V_{AGND}	–	V_{AREF}	V	3)	P_5.9.9
Analog clock frequency	f_{ADCI}	0.5	–	20	MHz	4)	P_5.9.10
Conversion time for 10-bit result[5]	t_{C10}	(13 + STC) × t_{ADCI} + 2 x t_{SYS}	(13 + STC) × t_{ADCI} + 2 x t_{SYS}	(13 + STC) × t_{ADCI} + 2 x t_{SYS}	–	–	P_5.9.11
Conversion time for 8-bit result	t_{C8}	(11 + STC) × t_{ADCI} + 2 × t_{SYS}	(11 + STC) × t_{ADCI} + 2 × t_{SYS}	(11 + STC) × t_{ADCI} + 2 × t_{SYS}	–	–	P_5.9.12
Wake-up time from analog Stop Mode, fast mode	t_{WAF}	–	–	4	µs	6)	P_5.9.13
Wake-up time from analog Stop Mode, slow mode	t_{WAS}	–	–	15	µs	6)	P_5.9.14
Total unadjusted error[7]	TUE	-15	–	+ 15	LSB	1) V_{AREF} = 5.0 V±1%	P_5.9.15
DNL error	EA_{DNL}EA	-2	–	+ 2	LSB	–	P_5.9.16
INL error	EA_{INL}EA	-5	–	+ 5	LSB	–	P_5.9.17
Gain error	EA_{GAIN}EA	-10	–	+ 10	LSB	–	P_5.9.18
Offset error	EA_{OFF}EA	-2	–	+ 2	LSB	–	P_5.9.19
Total capacitance of an analog input	C_{AINT}	–	–	10	pF	6)8)	P_5.9.20
Switched capacitance of an analog input	C_{AINS}	–	–	4	pF	6)8)	P_5.9.21
Resistance of the analog input path	R_{AIN}	–	–	2	kΩ	6)8)	P_5.9.22
Total capacitance of the reference input	C_{AREFT}	–	–	15	pF	6)8)	P_5.9.23
Switched capacitance of the reference input	C_{AREFS}	–	–	7	pF	6)8)	P_5.9.24
Resistance of the reference input path	R_{AREF}	–	–	2	kΩ	6)8)	P_5.9.25

Revision	Date	Changes
1.1	2012-03-08	**Table 14**: - Renamed Parameter “Output voltage VDDP” to “Voltage VDDP” (2x) - Renamed Parameter “Output voltage VDDC” to “Voltage VDDC”
1.1	2012-03-08	**Table 28**: Added value LIN input capacity C_{LIN_IN}

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