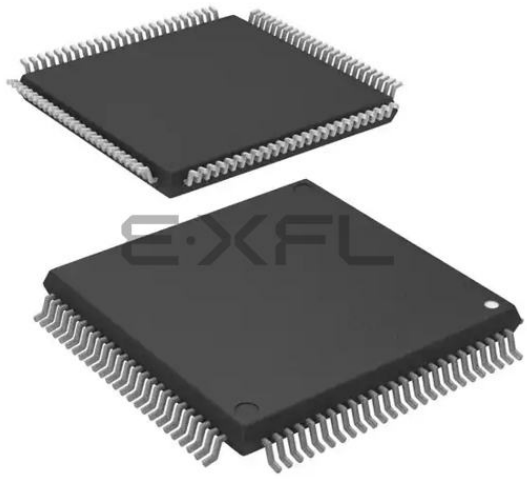
Renesas Electronics America Inc - M30873FHAGP#U3 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	M32C/80
Core Size	16/32-Bit
Speed	32MHz
Connectivity	CANbus, EBI/EMI, I²C, IEBus, IrDA, SIO, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	85
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30873fhagp-u3

1. Overview

1.1 Features

The M32C/87 Group (M32C/87, M32C/87A, M32C/87B) is a single-chip control MCU, fabricated using high-performance silicon gate CMOS technology, embedding the M32C/80 Series CPU core. The M32C/87 Group (M32C/87, M32C/87A, M32C/87B) is housed in 144-pin and 100-pin plastic molded LQFP/QFP packages.
With a 16-Mbyte address space, this MCU combines advanced instruction manipulation capabilities to process complex instructions by less bytes and execute instructions at higher speed.
The M32C/87 Group (M32C/87, M32C/87A, M32C/87B) has a multiplier and DMAC adequate for office automation, communication devices and industrial equipment, and other high-speed processing applications.

1.1.1 Applications

Audio components, cameras, office equipment, communication devices, mobile devices, etc.

1.1.2 Specifications

Tables 1.1 to 1.4 list the specifications of the M32C/87 Group (M32C/87, M32C/87A, M32C/87B).

Table 1.1 Specifications (144-Pin Package) (1/2)

Item	Function	Specification
CPU	Central processing unit	M32C/80 core (multiplier: 16 bits × 16 bits → 32 bits multiply-addition operation instructions: 16 × 16 + 48 → 48 bits) • Basic instructions: 108 • Minimum instruction execution time: 31.3 ns (f(CPU) = 32 MHz, VCC1 = 4.2 to 5.5 V) 41.7 ns (f(CPU) = 24 MHz, VCC1 = 3.0 to 5.5 V) • Operating modes: Single-chip mode, memory expansion mode, and microprocessor mode
Memory	ROM, RAM, data flash	See **Tables 1.5 to 1.7 Product List**.
Power Supply Voltage Detection		Vdet3 detection function, Vdet4 detection function, cold start/warm start determination function
External Bus Expansion	Bus/memory expansion function	• Address space: 16 Mbytes • External bus interface: 1 to 7 wait states can be inserted, 4 chip select outputs, 3 V and 5 V interfaces • Bus format: Switchable between separate bus and multiplexed bus formats, switchable data bus width (8-bit or 16-bit)
Clock	Clock generation circuits	• 4 circuits: Main clock, sub clock, on-chip oscillator, PLL frequency synthesizer • Oscillation stop detection: Main clock oscillation stop detection function • Frequency divider circuit: Dividing ratio selectable among 1, 2, 3, 4, 6, 8, 10, 12, 14, 16 • Low power consumption features: Wait mode, stop mode
Interrupts		• Interrupt vectors: 70 • External interrupt inputs: 14 ($\overline{\text{NMI}}$, $\overline{\text{INT}}$ × 9, key input × 4) • Interrupt priority levels: 7
Watchdog Timer		15-bit × 1 channel (with prescaler)
DMA	DMAC	• 4 channels, cycle steal method • Trigger sources: 43 • Transfer modes: 2 (single transfer and repeat transfer)
	DMACII	• Can be activated by all peripheral function interrupt sources • Transfer modes: 2 (single transfer and burst transfer) • Immediate transfer, calculation transfer, and chain transfer functions
Timer	Timer A	16-bit timer × 5 Timer mode, event counter mode, one-shot timer mode, pulse width modulation (PWM) mode, Event counter 2-phase pulse signal processing (2-phase encoder input) × 3
	Timer B	16-bit timer × 6 Timer mode, event counter mode, pulse period measurement mode, pulse width measurement mode
	Timer function for 3-phase motor control	3-phase inverter control × 1 (using timer A1, timer A2, timer A4, and timer B2) On-chip dead time timer

Table 1.7 M32C/87 Group (3) (M32C/87B: no CAN module) Current as of Jul. 2008

Part Number	Package Code	ROM Capacity	RAM Capacity	Remarks
M3087BFLBGP	PLQP0144KA-A (144P6Q-A)	1 MB + 4 KB(1)	48 KB	Flash memory
M30879FLBFP	PRQP0100JB-A (100P6S-A)			
M30879FLBGP	PLQP0100KB-A (100P6Q-A)			
M3087BFKBGP	PLQP0144KA-A (144P6Q-A)	768 KB + 4 KB(1)		
M30879FKBGP	PLQP0100KB-A (100P6Q-A)			
M30878FJBGP	PLQP0144KA-A (144P6Q-A)	512 KB + 4 KB(1)	31 KB	
M30876FJBGP	PLQP0100KB-A (100P6Q-A)			
M30875FHBGP	PLQP0144KA-A (144P6Q-A)	384 KB + 4 KB(1)	24 KB	
M30873FHBGP	PLQP0100KB-A (100P6Q-A)			
M30878MJB-XXXGP	PLQP0144KA-A (144P6Q-A)	512 KB	31 KB	Mask ROM
M30876MJB-XXXFP	PRQP0100JB-A (100P6S-A)			
M30876MJB-XXXGP	PLQP0100KB-A (100P6Q-A)			
M30875MHB-XXXGP	PLQP0144KA-A (144P6Q-A)	384 KB	24 KB	
M30873MHB-XXXGP	PLQP0100KB-A (100P6Q-A)			

NOTE:
1. Additional 4-Kbyte space is available for data flash memory.

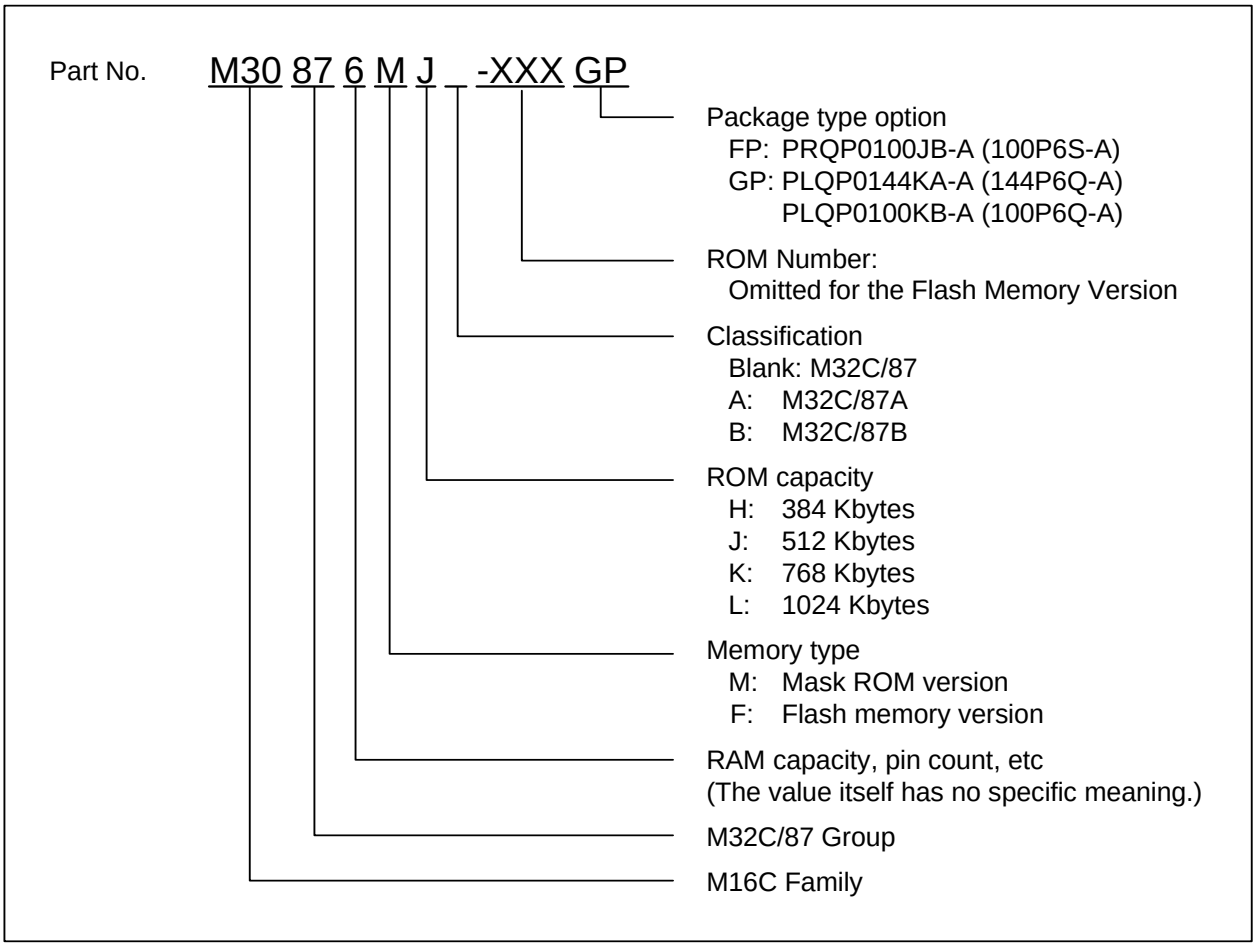


Figure 1.1 Product Numbering System

Table 1.8 144-Pin Package List of Pin Names (1/4)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin(1)	Intelligent I/O Pin	Analog Pin	Bus Control Pin
1		P9_6			TXD4/SDA4/SRXD4/ CAN1OUT		ANEX1	
2		P9_5			CLK4/CAN1IN/$\overline{\text{CAN1WU}}$		ANEX0	
3		P9_4		TB4IN	$\overline{\text{CTS4}}$/$\overline{\text{RTS4}}$/$\overline{\text{SS4}}$		DA1	
4		P9_3		TB3IN	$\overline{\text{CTS3}}$/$\overline{\text{RTS3}}$/$\overline{\text{SS3}}$		DA0	
5		P9_2		TB2IN	TXD3/SDA3/SRXD3	OUTC2_0/IEOUT/ISTXD2		
6		P9_1		TB1IN	RXD3/SCL3/STXD3	IEIN/ISRXD2		
7		P9_0		TB0IN	CLK3			
8		P14_6	$\overline{\text{INT8}}$					
9		P14_5	$\overline{\text{INT7}}$					
10		P14_4	$\overline{\text{INT6}}$					
11		P14_3				INPC1_7/OUTC1_7		
12		P14_2				INPC1_6/OUTC1_6		
13		P14_1				INPC1_5/OUTC1_5		
14		P14_0				INPC1_4/OUTC1_4		
15	BYTE							
16	CNVSS							
17	XCIN	P8_7						
18	XCOUT	P8_6						
19	$\overline{\text{RESET}}$							
20	XOUT							
21	VSS							
22	XIN							
23	VCC1							
24		P8_5	$\overline{\text{NMI}}$					
25		P8_4	$\overline{\text{INT2}}$					
26		P8_3	$\overline{\text{INT1}}$		CAN0IN/CAN1IN			
27		P8_2	$\overline{\text{INT0}}$		CAN0OUT/CAN1OUT			
28		P8_1		TA4IN/$\overline{\text{U}}$/RTP2_3	$\overline{\text{CTS5}}$/$\overline{\text{RTS5}}$	INPC1_5/OUTC1_5		
29		P8_0		TA4OUT/U	RXD5	ISRXD0		
30		P7_7		TA3IN/RTP2_2	CLK5/CAN0IN	INPC1_4/OUTC1_4/ ISCLK0		
31		P7_6		TA3OUT	TXD5/CAN0OUT	INPC1_3/OUTC1_3/ ISTXD0		
32		P7_5		TA2IN/$\overline{\text{W}}$/RTP2_1		INPC1_2/OUTC1_2/ ISRXD1		
33		P7_4		TA2OUT/W/ RTP2_0		INPC1_1/OUTC1_1/ ISCLK1		
34		P7_3		TA1IN/$\overline{\text{V}}$	$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$/$\overline{\text{SS2}}$	INPC1_0/OUTC1_0/ ISTXD1		
35		P7_2		TA1OUT/V	CLK2			
36		P7_1		TA0IN/TB5IN/ RTP0_3	RXD2/SCL2/STXD2	INPC1_7/OUTC1_7/ OUTC2_2/ISRXD2/IEIN		
37		P7_0		TA0OUT/RTP0_2	TXD2/SDA2/SRXD2	INPC1_6/OUTC1_6/ OUTC2_0/ISTXD2/IEOUT		
38		P6_7			TXD1/SDA1/SRXD1			
39	VCC1							
40		P6_6			RXD1/SCL1/STXD1			

NOTE:
1. The CAN pins cannot be used in M32C/87B. Only CAN0 pins can be used in M32C/87A.

Table 1.9 144-Pin Package List of Pin Names (2/4)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
41	VSS							
42		P6_5			CLK1			
43		P6_4			$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$/$\overline{\text{SS1}}$	OUTC2_1/ISCLK2		
44		P6_3			TXD0/SDA0/SRXD0/ IrDAOUT			
45		P6_2			RXD0/SCL0/STXD0/ IrDAIN			
46		P6_1		RTP0_1	CLK0			
47		P6_0		RTP0_0	$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$/$\overline{\text{SS0}}$			
48		P13_7				OUTC2_7		
49		P13_6				OUTC2_1/ISCLK2		
50		P13_5				OUTC2_2/ISRXD2/ IEIN		
51		P13_4				OUTC2_0/ISTXD2/ IEOUT		
52		P5_7						$\overline{\text{RDY}}$
53		P5_6						ALE
54		P5_5						$\overline{\text{HOLD}}$
55		P5_4						$\overline{\text{HLDA}}$/ALE
56		P13_3				OUTC2_3		
57	VSS							
58		P13_2				OUTC2_6		
59	VCC2							
60		P13_1				OUTC2_5		
61		P13_0				OUTC2_4		
62	CLKOUT	P5_3						BCLK/ALE
63		P5_2						$\overline{\text{RD}}$
64		P5_1						$\overline{\text{WRH}}$/$\overline{\text{BHE}}$
65		P5_0						$\overline{\text{WRL}}$/$\overline{\text{WR}}$
66		P12_7						
67		P12_6						
68		P12_5						
69		P4_7						$\overline{\text{CS0}}$/A23
70		P4_6						$\overline{\text{CS1}}$/A22
71		P4_5						$\overline{\text{CS2}}$/A21
72		P4_4						$\overline{\text{CS3}}$/A20
73		P4_3						A19
74	VCC2							
75		P4_2						A18
76	VSS							
77		P4_1						A17
78		P4_0						A16
79		P3_7						A15,[A15/D15]
80		P3_6						A14,[A14/D14]

Table 1.11 144-Pin Package List of Pin Names (4/4)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
121		P0_1					AN0_1	D1
122		P0_0					AN0_0	D0
123		P15_7			$\overline{\text{CTS6}}$/$\overline{\text{RTS6}}$		AN15_7	
124		P15_6			CLK6		AN15_6	
125		P15_5			RXD6		AN15_5	
126		P15_4			TXD6		AN15_4	
127		P15_3			$\overline{\text{CTS5}}$/$\overline{\text{RTS5}}$		AN15_3	
128		P15_2			RXD5	ISRXD0	AN15_2	
129		P15_1			CLK5	ISCLK0	AN15_1	
130	VSS							
131		P15_0			TXD5	ISTXD0	AN15_0	
132	VCC1							
133		P10_7	$\overline{\text{KI3}}$	RTP3_3			AN_7	
134		P10_6	$\overline{\text{KI2}}$	RTP3_2			AN_6	
135		P10_5	$\overline{\text{KI1}}$	RTP3_1			AN_5	
136		P10_4	$\overline{\text{KI0}}$	RTP3_0			AN_4	
137		P10_3		RTP1_3			AN_3	
138		P10_2		RTP1_2			AN_2	
139		P10_1		RTP1_1			AN_1	
140	AVSS							
141		P10_0		RTP1_0			AN_0	
142	VREF							
143	AVCC							
144		P9_7			RXD4/SCL4/STXD4		$\overline{\text{ADTRG}}$	

Table 1.12 100-Pin Package List of Pin Names (1/3)

Pin No.		Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin(1)	Intelligent I/O Pin	Analog Pin	Bus Control Pin
FP	GP								
1	99		P9_6			TXD4/SDA4/SRXD4/ CAN1OUT		ANEX1	
2	100		P9_5			CLK4/CAN1IN/ CAN1WU		ANEX0	
3	1		P9_4		TB4IN	CTS4/RTS4/SS4		DA1	
4	2		P9_3		TB3IN	CTS3/RTS3/SS3		DA0	
5	3		P9_2		TB2IN	TXD3/SDA3/SRXD3	OUTC2_0/IEOUT/ISTXD2		
6	4		P9_1		TB1IN	RXD3/SCL3/STXD3	IEIN/ISRXD2		
7	5		P9_0		TB0IN	CLK3			
8	6	BYTE							
9	7	CNVSS							
10	8	XCIN	P8_7						
11	9	XCOUT	P8_6						
12	10	RESET							
13	11	XOUT							
14	12	VSS							
15	13	XIN							
16	14	VCC1							
17	15		P8_5	NMI					
18	16		P8_4	INT2					
19	17		P8_3	INT1		CAN0IN/CAN1IN			
20	18		P8_2	INT0		CAN0OUT/CAN1OUT			
21	19		P8_1		TA4IN/U/RTP2_3	CTS5/RTS5	INPC1_5/OUTC1_5		
22	20		P8_0		TA4OUT/U	RXD5	ISRXD0		
23	21		P7_7		TA3IN/RTP2_2	CLK5/CAN0IN	INPC1_4/OUTC1_4/ ISCLK0		
24	22		P7_6		TA3OUT	TXD5/CAN0OUT	INPC1_3/OUTC1_3/ ISTXD0		
25	23		P7_5		TA2IN/W/RTP2_1		INPC1_2/OUTC1_2 ISRXD1		
26	24		P7_4		TA2OUT/W/ RTP2_0		INPC1_1/OUTC1_1/ ISCLK1		
27	25		P7_3		TA1IN/V	CTS2/RTS2/SS2	INPC1_0/OUTC1_0/ ISTXD1		
28	26		P7_2		TA1OUT/V	CLK2			
29	27		P7_1		TA0IN/TB5IN/ RTP0_3	RXD2/SCL2/STXD2	INPC1_7/OUTC1_7/ OUTC2_2/ISRXD2/IEIN		
30	28		P7_0		TA0OUT/RTP0_2	TXD2/SDA2/SRXD2	INPC1_6/OUTC1_6/ OUTC2_0/ISTXD2/IEOUT		
31	29		P6_7			TXD1/SDA1/SRXD1			
32	30		P6_6			RXD1/SCL1/STXD1			
33	31		P6_5			CLK1			
34	32		P6_4			CTS1/RTS1/SS1	OUTC2_1/ISCLK2		
35	33		P6_3			TXD0/SDA0/SRXD0/ IrDAOUT			
36	34		P6_2			RXD0/SCL0/STXD0/ IrDAIN			
37	35		P6_1		RTP0_1	CLK0			
38	36		P6_0		RTP0_0	CTS0/RTS0/SS0			
39	37		P5_7						RDY
40	38		P5_6						ALE

NOTE:
1. The CAN pins cannot be used in M32C/87B. Only CAN0 pins can be used in M32C/87A.

Table 4.11 SFR Address Map (11/20)

Address	Register[2][3]	Symbol	After Reset
0250h	CAN1 Slot Buffer Select Register	C1SBS	00h[1]
0251h	CAN1 Control Register 1	C1CTLR1	X000 00XXb[1]
0252h	CAN1 Sleep Control Register	C1SLPR	XXXX XXX0b[1]
0253h			
0254h	CAN1 Acceptance Filter Support Register	C1AFS	0000 0000b[1]
0255h			0000 0001b[1]
0256h			
0257h			
0258h			
0259h			
025Ah			
025Bh			
025Ch			
025Dh			
025Eh			
025Fh			
0260h	CAN1 Message Slot Buffer 0 Standard ID0	C1SLOT0_0	XXh
0261h	CAN1 Message Slot Buffer 0 Standard ID1	C1SLOT0_1	XXh
0262h	CAN1 Message Slot Buffer 0 Extended ID0	C1SLOT0_2	XXh
0263h	CAN1 Message Slot Buffer 0 Extended ID1	C1SLOT0_3	XXh
0264h	CAN1 Message Slot Buffer 0 Extended ID2	C1SLOT0_4	XXh
0265h	CAN1 Message Slot Buffer 0 Data Length Code	C1SLOT0_5	XXh
0266h	CAN1 Message Slot Buffer 0 Data 0	C1SLOT0_6	XXh
0267h	CAN1 Message Slot Buffer 0 Data 1	C1SLOT0_7	XXh
0268h	CAN1 Message Slot Buffer 0 Data 2	C1SLOT0_8	XXh
0269h	CAN1 Message Slot Buffer 0 Data 3	C1SLOT0_9	XXh
026Ah	CAN1 Message Slot Buffer 0 Data 4	C1SLOT0_10	XXh
026Bh	CAN1 Message Slot Buffer 0 Data 5	C1SLOT0_11	XXh
026Ch	CAN1 Message Slot Buffer 0 Data 6	C1SLOT0_12	XXh
026Dh	CAN1 Message Slot Buffer 0 Data 7	C1SLOT0_13	XXh
026Eh	CAN1 Message Slot Buffer 0 Time Stamp High-Order	C1SLOT0_14	XXh
026Fh	CAN1 Message Slot Buffer 0 Time Stamp Low-Order	C1SLOT0_15	XXh
0270h	CAN1 Message Slot Buffer 1 Standard ID0	C1SLOT1_0	XXh
0271h	CAN1 Message Slot Buffer 1 Standard ID1	C1SLOT1_1	XXh
0272h	CAN1 Message Slot Buffer 1 Extended ID0	C1SLOT1_2	XXh
0273h	CAN1 Message Slot Buffer 1 Extended ID1	C1SLOT1_3	XXh
0274h	CAN1 Message Slot Buffer 1 Extended ID2	C1SLOT1_4	XXh
0275h	CAN1 Message Slot Buffer 1 Data Length Code	C1SLOT1_5	XXh
0276h	CAN1 Message Slot Buffer 1 Data 0	C1SLOT1_6	XXh
0277h	CAN1 Message Slot Buffer 1 Data 1	C1SLOT1_7	XXh
0278h	CAN1 Message Slot Buffer 1 Data 2	C1SLOT1_8	XXh
0279h	CAN1 Message Slot Buffer 1 Data 3	C1SLOT1_9	XXh
027Ah	CAN1 Message Slot Buffer 1 Data 4	C1SLOT1_10	XXh
027Bh	CAN1 Message Slot Buffer 1 Data 5	C1SLOT1_11	XXh
027Ch	CAN1 Message Slot Buffer 1 Data 6	C1SLOT1_12	XXh
027Dh	CAN1 Message Slot Buffer 1 Data 7	C1SLOT1_13	XXh
027Eh	CAN1 Message Slot Buffer 1 Time Stamp High-Order	C1SLOT1_14	XXh
027Fh	CAN1 Message Slot Buffer 1 Time Stamp Low-Order	C1SLOT1_15	XXh

X: Undefined
Blank spaces are all reserved. No access is allowed.
NOTES:
1. Values are obtained by setting the SLEEP bit in the C1SLPR register to “1” (sleep mode exited) after reset and supplying a clock to the CAN module.
2. The CAN-associated registers (allocated in addresses 01E0h to 02BFh) cannot be used in M32C/87B. In M32C/87A, only CAN0-associated registers can be used.
3. Set the PM13 bit in the PM1 register to 1 (2 wait states for SFR area) before accessing the CAN-associated registers.

Table 4.19 SFR Address Map (19/20)

Address	Register	Symbol	After Reset
03A0h	Function Select Register A8(1)	PS8	X000 0000b
03A1h	Function Select Register A9(1)	PS9	00h
03A2h			
03A3h	Function Select Register B9(1)	PSL9	XXX0 XX00b
03A4h	Function Select Register E2	PSE2	XXXX XX0Xb
03A5h			
03A6h			
03A7h	Function Select Register D1	PSD1	00X0 XX00b
03A8h	Function Select Register D2	PSD2	XXXX XX0Xb
03A9h			
03AAh	Function Select Register C6(1)	PSC6	XXXX 0X00b
03ABh	Function Select Register E1	PSE1	00XX XX00b
03ACh	Function Select Register C2	PSC2	XXXX X00Xb
03ADh	Function Select Register C3	PSC3	X0XX XXXXb
03AEh			
03AFh	Function Select Register C	PSC	00h
03B0h	Function Select Register A0	PS0	00h
03B1h	Function Select Register A1	PS1	00h
03B2h	Function Select Register B0	PSL0	00h
03B3h	Function Select Register B1	PSL1	00h
03B4h	Function Select Register A2	PS2	00X0 0000b
03B5h	Function Select Register A3	PS3	00h
03B6h	Function Select Register B2	PSL2	00X0 0000b
03B7h	Function Select Register B3	PSL3	00h
03B8h	Function Select Register A4	PS4	00h
03B9h	Function Select Register A5(1)	PS5	XXX0 0000b
03BAh			
03BBh	Function Select Register B5(1)	PSL5	XXX0 0000b
03BCh	Function Select Register A6(1)	PS6	00h
03BDh	Function Select Register A7(1)	PS7	00h
03BEh	Function Select Register B6(1)	PSL6	00h
03BFh	Function Select Register B7(1)	PSL7	00h
03C0h	Port P6 Register	P6	XXh
03C1h	Port P7 Register	P7	XXh
03C2h	Port P6 Direction Register	PD6	00h
03C3h	Port P7 Direction Register	PD7	00h
03C4h	Port P8 Register	P8	XXh
03C5h	Port P9 Register	P9	XXh
03C6h	Port P8 Direction Register	PD8	00X0 0000b
03C7h	Port P9 Direction Register	PD9	00h
03C8h	Port P10 Register	P10	XXh
03C9h	Port P11 Register(1)	P11	XXh
03CAh	Port P10 Direction Register	PD10	00h
03CBh	Port P11 Direction Register(1)(2)	PD11	XXX0 0000b
03CCh	Port P12 Register(1)	P12	XXh
03CDh	Port P13 Register(1)	P13	XXh
03CEh	Port P12 Direction Register(1)(2)	PD12	00h
03CFh	Port P13 Direction Register(1)(2)	PD13	00h

X: Undefined
Blank spaces are all reserved. No access is allowed.
NOTES:
1. These registers cannot be used in the 100-pin package.
2. Set to FFh in the 100-pin package.

Table 5.3 Recommended Operating Conditions (2/3)
(VCC1 = VCC2 = 3.0 to 5.5 V, Topr = -20 to 85°C unless otherwise specified

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
IOH(peak)	Peak output high “H” current(2)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7(3)			-10.0	mA
IOH(avg)	Average output high “H” current(1)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7(3)			-5.0	mA
IOL(peak)	Peak output low “L” current(2)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7(3)			10.0	mA
IOL(avg)	Average output low “L” current(1)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7(3)			5.0	mA

NOTES:
1. Average output current is the average value within 100 ms.
2. A total IOL(peak) of P0, P1, P2, P8_6, P8_7, P9, P10, P11, P14, and P15 must be 80 mA or less.
   A total IOL(peak) of P3, P4, P5, P6, P7,P8_0 to P8_4, P12, and P13 must be 80 mA or less.
   A total IOH(peak) of P0, P1, P2, and P11 must be -40 mA or less.
   A total IOH(peak) of P8_6 to P8_7, P9, P10, P14, and P15 must be -40 mA or less.
   A total IOH(peak) of P3, P4, P5, P12, and P13 must be -40 mA or less.
   A total IOH(peak) of P6, P7, and P8_0 to P8_4 must be -40 mA or less.
3. P11 to P15 are provided in the 144-pin package only.

VCC1 = VCC2 = 5V

Timing Requirements
(VCC1 = VCC2 = 4.2 to 5.5 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.27 External Interrupt $\overline{INTi}$ Input (Edge Sensitive)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tw(INH)	$\overline{INTi}$ input high (“H”) pulse width	250		ns
tw(INL)	$\overline{INTi}$ input low (“L”) pulse width	250		ns

i = 0 to 8(1)

NOTE:
1. $\overline{INT6}$ to $\overline{INT8}$ are provided in the 144-pin package only.

VCC1 = VCC2 = 5V

Switching Characteristics
(VCC1 = VCC2 = 4.2 to 5.5 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.29 Memory Expansion Mode and Microprocessor Mode (when accessing external memory space)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min.	Max.	
td(BCLK-AD)	Address output delay time	See Figure 5.2		18	ns
th(BCLK-AD)	Address output hold time (BCLK standard)		-3		ns
th(RD-AD)	Address output hold time (RD standard)(3)		0		ns
th(WR-AD)	Address output hold time (WR standard)(3)		(note 1)		ns
td(BCLK-CS)	Chip-select signal output delay time			18	ns
th(BCLK-CS)	Chip-select signal output hold time (BCLK standard)		-3		ns
th(RD-CS)	Chip-select signal output hold time (RD standard)(3)		0		ns
th(WR-CS)	Chip-select signal output hold time (WR standard)(3)		(note 1)		ns
td(BCLK-RD)	RD signal output delay time			18	ns
th(BCLK-RD)	RD signal output hold time		-5		ns
td(BCLK-WR)	WR signal output delay time			18	ns
th(BCLK-WR)	WR signal output hold time		-5		ns
td(DB-WR)	Data output delay time (WR standard)		(note 2)		ns
th(WR-DB)	Data output hold time (WR standard)(3)		(note 1)		ns
tw(WR)	WR output width		(note 2)		ns

NOTES:

1. Values, which depend on BCLK frequency, can be obtained from the following equations.

$$th(WR\text{-}DB) = \frac{10^9}{f(BCLK) \times 2} - 15 \text{ [ns]}$$

$$th(WR\text{-}AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \text{ [ns]}$$

$$th(WR\text{-}CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \text{ [ns]}$$

2. Values, which depend on BCLK frequency and external bus cycles, can be obtained from the following equations.

$$td(DB\text{-}WR) = \frac{10^9 \times m}{f(BCLK)} - 20 \text{ [ns] (if external bus cycle is a}\phi + b\phi\text{, m = b)}$$

$$tw(WR) = \frac{10^9 \times n}{f(BCLK) \times 2} - 15 \text{ [ns] (if external bus cycle is a}\phi + b\phi\text{, n = (b × 2) - 1)}$$

3. tc [ns] is added when recovery cycle is inserted.

VCC1 = VCC2 = 3.3 V

Timing Requirements
(VCC1 = VCC2 = 3.0 to 3.6 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.36 External Clock Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc	External clock input cycle time	41		ns
tw(H)	External clock input high (“H”) pulse width	18		ns
tw(L)	External clock input low (“L”) pulse width	18		ns
tr	External clock rise time		5	ns
tf	External clock fall time		5	ns

Table 5.37 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	100		ns
tw(TAH)	TAiIN input high (“H”) pulse width	40		ns
tw(TAL)	TAiIN input low (“L”) pulse width	40		ns

i = 0 to 4

Table 5.38 Timer A Input (Gate Signal Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	400		ns
tw(TAH)	TAiIN input high (“H”) pulse width	200		ns
tw(TAL)	TAiIN input low (“L”) pulse width	200		ns

i = 0 to 4

Table 5.39 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	200		ns
tw(TAH)	TAiIN input high (“H”) pulse width	100		ns
tw(TAL)	TAiIN input low (“L”) pulse width	100		ns

i = 0 to 4

Table 5.40 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tw(TAH)	TAiIN input high (“H”) pulse width	100		ns
tw(TAL)	TAiIN input low (“L”) pulse width	100		ns

i = 0 to 4

VCC1 = VCC2 = 3.3 V

Timing Requirements
(VCC1 = VCC2 = 3.0 to 3.6 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.46 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(AD)	$\overline{\text{ADTRG}}$ input cycle time (required for trigger)	1000		ns
tw(ADL)	$\overline{\text{ADTRG}}$ input low (“L”) pulse width	125		ns

Table 5.47 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CK)	CLKi input cycle time	200		ns
tw(CKH)	CLKi input high (“H”) pulse width	100		ns
tw(CKL)	CLKi input low (“L”) pulse width	100		ns
td(C-Q)	TXDi output delay time		80	ns
th(C-Q)	TXDi output hold time	0		ns
tsu(D-C)	RXDi input setup time	70		ns
th(C-D)	RXDi input hold time	90		ns

i = 0 to 6

Table 5.48 Intelligent I/O Communication Function (Groups 0 and 1)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CK)	ISCLKi input cycle time	600		ns
tw(CKH)	ISCLKi input high (“H”) pulse width	300		ns
tw(CKL)	ISCLKi input low (“L”) pulse width	300		ns
td(C-Q)	ISTXDi output delay time		100	ns
th(C-Q)	ISTXDi output hold time	0		ns
tsu(D-C)	ISRXDi input setup time	100		ns
th(C-D)	ISRXDi input hold time	100		ns

i = 0, 1

Table 5.49 Intelligent I/O Communication Function (Group 2)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CK)	ISCLK2 input cycle time	600		ns
tw(CKH)	ISCLK2 input high (“H”) pulse width	300		ns
tw(CKL)	ISCLK2 input low (“L”) pulse width	300		ns
td(C-Q)	ISTXD2 output delay time		180	ns
th(C-Q)	ISTXD2 output hold time	0		ns
tsu(D-C)	ISRXD2 input setup time	150		ns
th(C-D)	ISRXD2 input hold time	100		ns

VCC1 = VCC2 = 3.3 V

Timing Requirements
(VCC1 = VCC2 = 3.0 to 3.6 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.50 External Interrupt $\overline{INTi}$ Input (Edge Sensitive)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tw(INH)	$\overline{INTi}$ input high (“H”) pulse width	250		ns
tw(INL)	$\overline{INTi}$ input low (“L”) pulse width	250		ns

i = 0 to 8(1)

NOTE:
1. $\overline{INT6}$ to $\overline{INT8}$ are provided in the 144-pin package only.

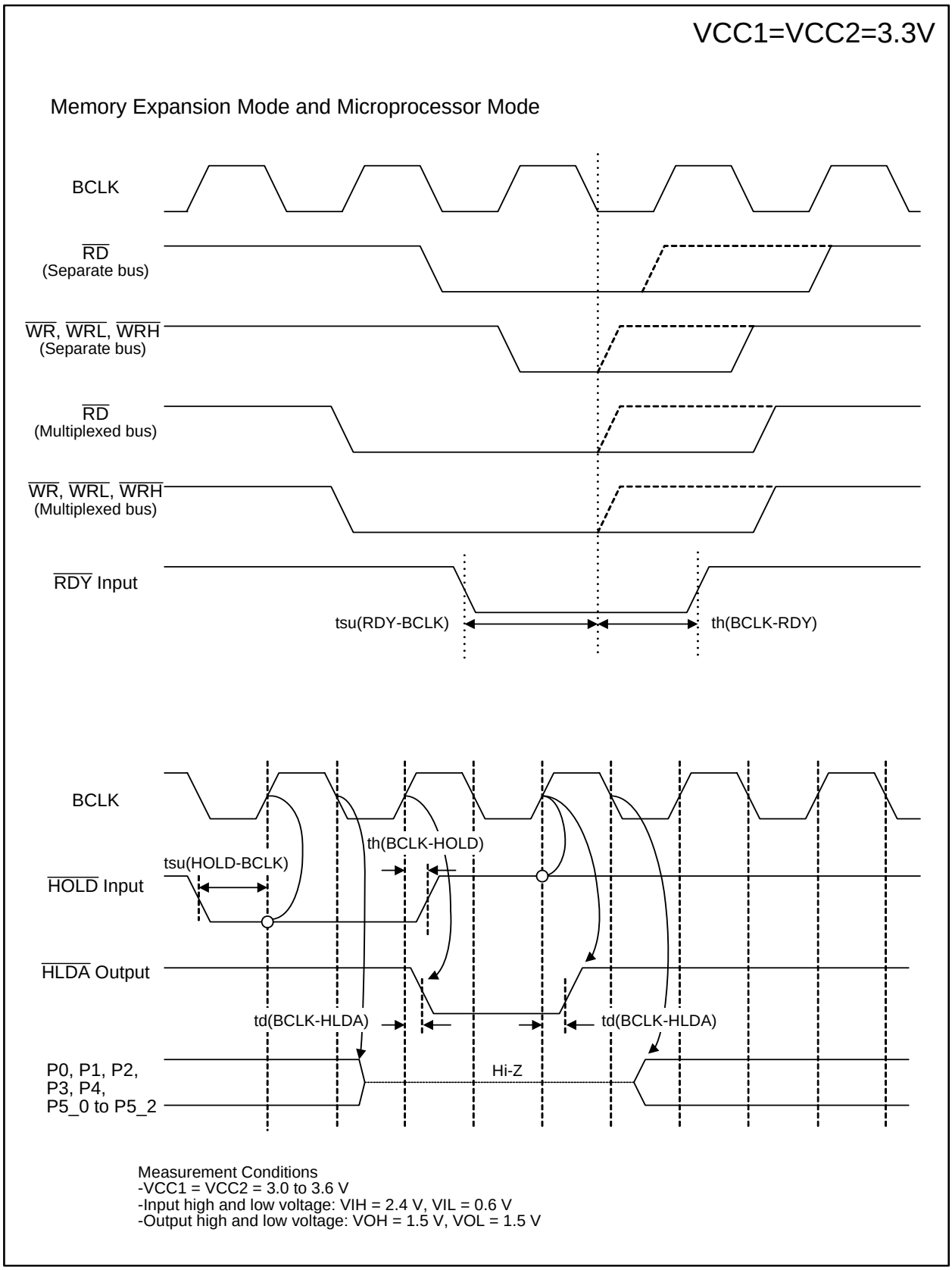
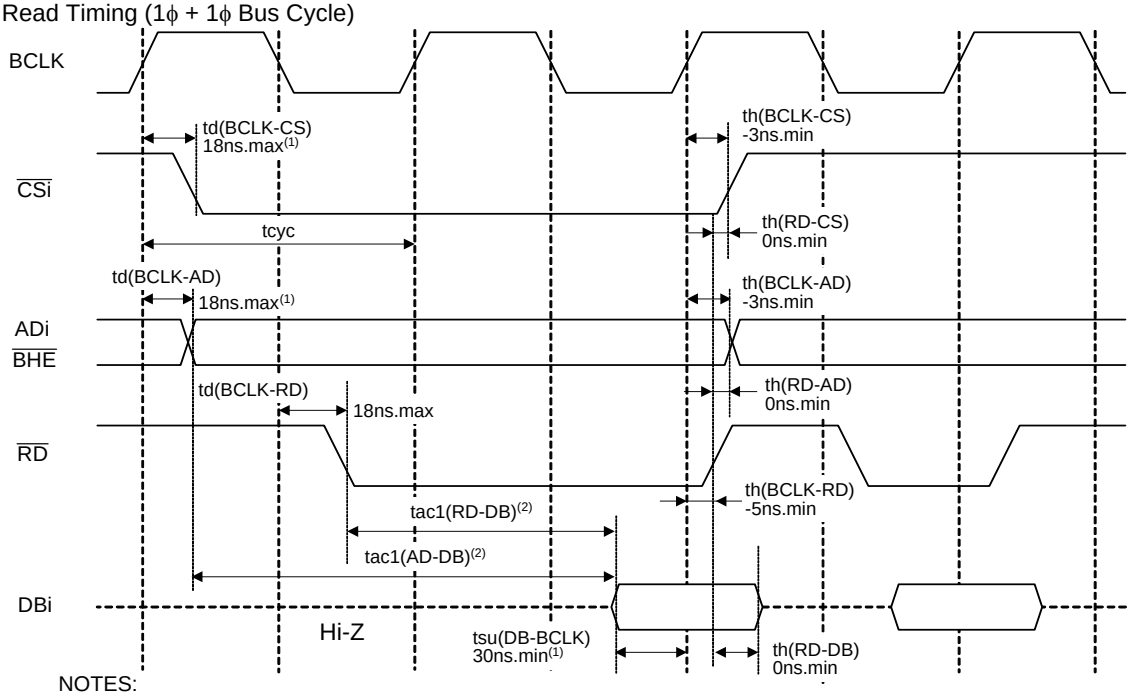


Figure 5.8 VCC1 = VCC2 = 3.3 V Timing Diagram (2/4)

Memory Expansion Mode and Microprocessor Mode
(when accessing an external memory space)

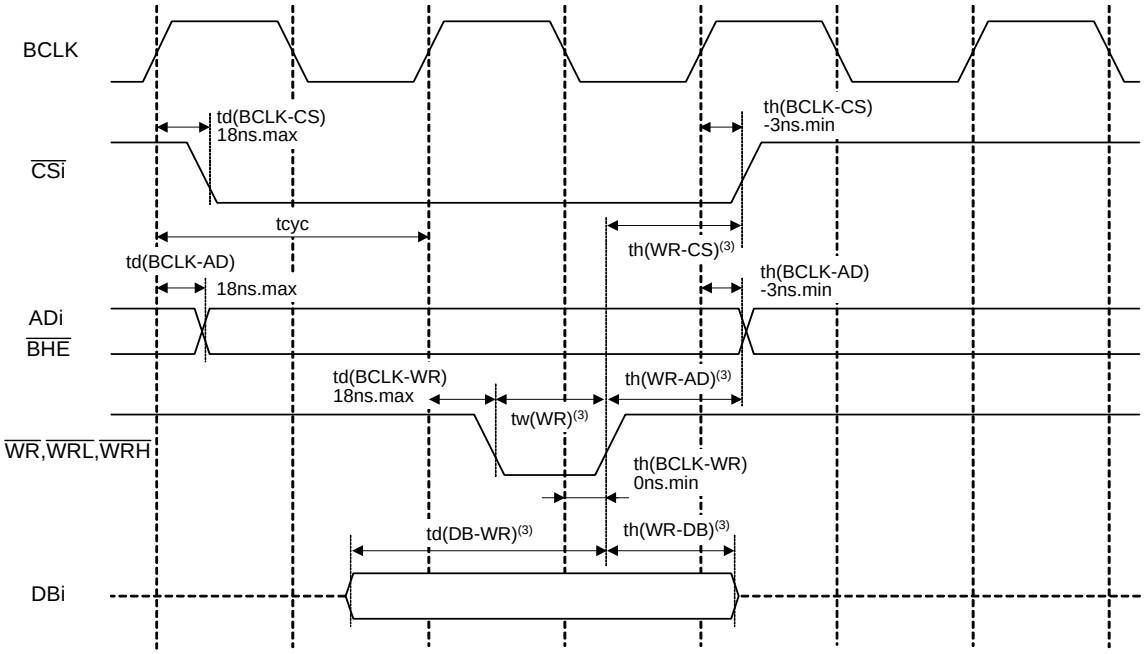
VCC1=VCC2=3.3V

Read Timing (1ϕ + 1ϕ Bus Cycle)



NOTES:
1. Values guaranteed only when the MCU is used stand-alone.
   A maximum of 35 ns is guaranteed for td(BCLK-AD) + tsu(DB-BCLK).
2. Varies with operation frequency:
   tac1(RD-DB) = (tcyc / 2 x m - 35) ns.max (if external bus cycle aϕ + bϕ, m = (b x 2) + 1)
   tac1(AD-DB) = (tcyc x n - 35) ns.max (if external bus cycle aϕ + bϕ, n = a + b)

Write Timing (1ϕ + 1ϕ Bus Cycle)



NOTES:
3. Varies with operation frequency:
   td(DB-WR) = (tcyc x m - 20) ns.min
   (if external bus cycle aϕ + bϕ, m = b)
   th(WR-DB) = (tcyc / 2 - 20) ns.min
   th(WR-AD) = (tcyc / 2 - 15) ns.min
   th(WR-CS) = (tcyc / 2 - 10) ns.min
   tw(WR) = (tcyc / 2 x n - 15) ns.min
   (if external bus cycle aϕ + bϕ, n = (b x 2) - 1)

Measurement Conditions:
- VCC1 = VCC2 = 3.0 to 3.6 V
- Input high and low voltage: VIH = 1.5 V, VIL = 0.5 V
- Output high and low voltage: VOH = 1.5 V, VOL = 1.5 V

$$tcyc = \frac{10^9}{f(BCLK)}$$

Figure 5.9 VCC1 = VCC2 = 3.3 V Timing Diagram (3/4)

REVISION HISTORY	M32C/87 Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.50	Dec.16, 04	–	New Document
1.00	Jul.14, 05	–	**M32C/87A and M32C/87B** added
		–	Package code changed: 144P6Q-A to PLQP0144KA-A, 100P6Q-A to PLQP0100KB-A, 100P6S-A to PRQP0100JB-A
		–	"Low Voltage Detection Reset" changed to "Brown-out Detection Reset"
			Overview
		2	• **Table 1.2 M32C/87 Group Performance (144-Pin Package)** M32C/87A and M32C/87B performance added to the CAN module performance; Power Consumption performance released
		3	• **Table 1.2 M32C/87 Group Performance (100-Pin Package)** M32C/87A and M32C/87B performance added to the CAN module performance; Power Consumption performance released
		4	• **Figure 1.1 M32C/87 Group Block Diagram** Note 4 deleted; note 5 added
		7	• **Figure 1.3 Pin Assignment for 144-Pin Package** Note 15 added
		8	• **Table 1.4 Pin Characteristics for 144-Pin Package** Note 1 added
		11	• **Figure 1.4 Pin Assignment for 100-Pin Package** Note 19 added
		12	• **Figure 1.5 Pin Assignment for 100-Pin Package** Note 15 added
		13	• **Table 1.5 Pin Characteristics for 100-Pin Package** Note 1 added
		17	• **Table 1.6 Pin Description** Note 2 added
			Memory
		22	• **Figure 3.1 Memory Map** Note 3 changed
			Special Function Register (SFR)
		26	• The RLVL register Value after reset modified
		26	• The IIO0IR to IIO11IR registers Value after reset modified
		27 to 30	• Name of the registers assosiated to Intelligent I/O changed
		27	• The G0RB register Value after reset modified
		27	• The G1BCR0 and G1BCR1 registers Value after reset modified
		29	• The G0CR register Value after reset modified
		32 to 37	• Note added to the CAN-associated registers
		40	• The TCSPR register Value after reset modified; note 1 added
		41	• The AD00 register Value after reset modified
		42	• The PSC register Value after reset modified
		42	• The PS2 register Value after reset modified
		43	• The PCR register Value after reset modified
		44	• The PSD1 register Value after reset modified
		45	• The PCR register Value after reset modified
			Electrical Characteristics
		48	• **Table 5.2 Electrical Characteristics** Parameter f(BCLK) and its values added; min. and max. values for f(RING) added
		49	• **Table 5.3 Electrical Characteristics** V_{OH} values modified**;** R_{PULLUP} value modified
		50	• **Table 5.3 Electrical Characteristics (Continued)** Measurement Condition and standard values for ICC added and some released
		52	• **Table 5.6 Flash Memory Version Electrical Characteristics** Word Program Time and Lock bit Program Time values modified; parameter All-Unlocked-Block-Erase Time deleted; note 1 deleted
		54	• **Table 5.10 Memory Expansion Mode and Microprocessor Mode** *tac1(RD-DB)* expression on note 1 modified; *tac2(RD-DB)* expression on note 1 added

REVISION HISTORY	M32C/87 Group Datasheet

Rev.	Date	Description	
		Page	Summary
			Electrical Characteristics
		57	• **Table 5.22 Memory Expansion Mode and Microprocessor Mode** *th(WR-DB)* expression on note 1 modified
		58	• **Table 5.23 Memory Expansion Mode and Microprocessor Mode** *th(WR-DB)* expression on note 1 modified; *th(ALE-AD)* expression on note 4 modified
		60	• **Figure 5.3 Vcc1=Vcc2=5V Timing Diagram (1)** *tac1(RD-DB)* expression on note 2 modified; *th(WR-DB)* and *tw(ER)* expressions on note 3 modified; *tcyc* expression added
		61	• **Figure 5.4 Vcc1=Vcc2=5V Timing Diagram (2)** *tac2(RD-DB) and tac2(AD-DB)* expressions on note 1 modified; *th(ALE-AD)* expressions on notes 1 and 2 modified; *td(DB-WR)* expression on note 2 modified; *tcyc* expression added
		62	• **Figure 5.5 Vcc1=Vcc2=5V Timing Diagram (3)** $\overline{\text{NMI}}$ input diagram added
		64	• **Table 5.24 Electrical Characteristics** V_{OH} values changed**;** R_{PULLUP} and Icc values modified
		65	• **Table 5.25 A/D Conversion Characteristics** tCONV value modified
		66	• **Table 5.28 Memory Expansion Mode and Microprocessor Mode** *tac1(RD-DB)* expression on note 1 modified; *tac2(RD-DB)* expression on note 1 added
		69	• **Table 5.40 Memory Expansion Mode and Microprocessor Mode** *th(BCLK-AD), th(BCLK-CS)* and *th(BCLK-RD)* values modified; *th(WR-AD)* expression on note 1 modified
		70	• **Table 5.41 Memory Expansion Mode and Microprocessor Mode** *th(BCLK-AD), th(BCLK-CS)* and *th(BCLK-RD)* values modified; *th(WR-AD)* expression on note 1 modified; *th(ALE-AD)* expression on note 4 modified
		71	• **Figure 5.7 Vcc1=Vcc2=3.3V Timing Diagram (1)** *th(BCLK-AD), th(BCLK-CS)* and *th(BCLK-RD)* values modified; *tac1(AD-DB)* expression on note 2 modified; *th(WR-DB)*, *th(WR-AD) and tw(WR)* expression on note 3 modified; *tcyc* expression added
		72	• **Figure 5.8 Vcc1=Vcc2=3.3V Timing Diagram (2)** *tac2(RD-DB) and tac1(AD-DB)* expressions on note 1 modified; *th(ALE-AD)* expressions on notes 1 and 2 modified; *td(WR-AD)*, *td(DB-WR) and th(WR-DB)* expressions on note 2 modified; *tcyc* expression added
		73	• **Figure 5.9 Vcc1=Vcc2=3.3V Timing Diagram (3)** $\overline{\text{NMI}}$ input diagram added
1.01	Aug. 29, 05		Overview
		17	• **Tables 1.6 Pin Description** Intelligent I/O functions modified
			Special Function Register (SFR)
		29	• The G1BCR0 register Value after reset modified
		29	• The G1BCR1 register Value after reset modified
			Electrical Characteristics
		49	• **Table 5.3 Electrical Characteristics** Icc standard value modified

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