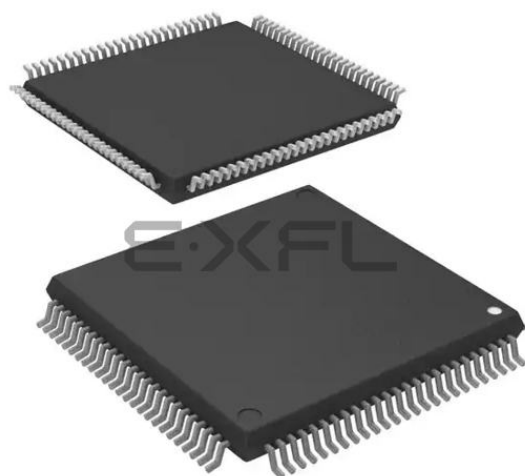




Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	M32C/80
Core Size	16/32-Bit
Speed	32MHz
Connectivity	EBI/EMI, I ² C, IEBus, IrDA, SIO, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	85
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30873fhbgp-u5

1. Overview

1.1 Features

The M32C/87 Group (M32C/87, M32C/87A, M32C/87B) is a single-chip control MCU, fabricated using high-performance silicon gate CMOS technology, embedding the M32C/80 Series CPU core. The M32C/87 Group (M32C/87, M32C/87A, M32C/87B) is housed in 144-pin and 100-pin plastic molded LQFP/QFP packages.

With a 16-Mbyte address space, this MCU combines advanced instruction manipulation capabilities to process complex instructions by less bytes and execute instructions at higher speed.

The M32C/87 Group (M32C/87, M32C/87A, M32C/87B) has a multiplier and DMAC adequate for office automation, communication devices and industrial equipment, and other high-speed processing applications.

1.1.1 Applications

Audio components, cameras, office equipment, communication devices, mobile devices, etc.

Table 1.7 M32C/87 Group (3) (M32C/87B: no CAN module) Current as of Jul. 2008

Part Number	Package Code	ROM Capacity	RAM Capacity	Remarks
M3087BFLBGP	PLQP0144KA-A (144P6Q-A)	1 MB + 4 KB ⁽¹⁾	48 KB	Flash memory
M30879FLBFP	PRQP0100JB-A (100P6S-A)			
M30879FLBGP	PLQP0100KB-A (100P6Q-A)			
M3087BFKBGP	PLQP0144KA-A (144P6Q-A)	768 KB + 4 KB ⁽¹⁾		
M30879FKBGP	PLQP0100KB-A (100P6Q-A)			
M30878FJBGP	PLQP0144KA-A (144P6Q-A)	512 KB + 4 KB ⁽¹⁾	31 KB	
M30876FJBGP	PLQP0100KB-A (100P6Q-A)			
M30875FHBGP	PLQP0144KA-A (144P6Q-A)	384 KB + 4 KB ⁽¹⁾	24 KB	
M30873FHBGP	PLQP0100KB-A (100P6Q-A)			
M30878MJB-XXXGP	PLQP0144KA-A (144P6Q-A)	512 KB	31 KB	Mask ROM
M30876MJB-XXXFP	PRQP0100JB-A (100P6S-A)			
M30876MJB-XXXGP	PLQP0100KB-A (100P6Q-A)			
M30875MHB-XXXGP	PLQP0144KA-A (144P6Q-A)	384 KB	24 KB	
M30873MHB-XXXGP	PLQP0100KB-A (100P6Q-A)			

NOTE:

1. Additional 4-Kbyte space is available for data flash memory.

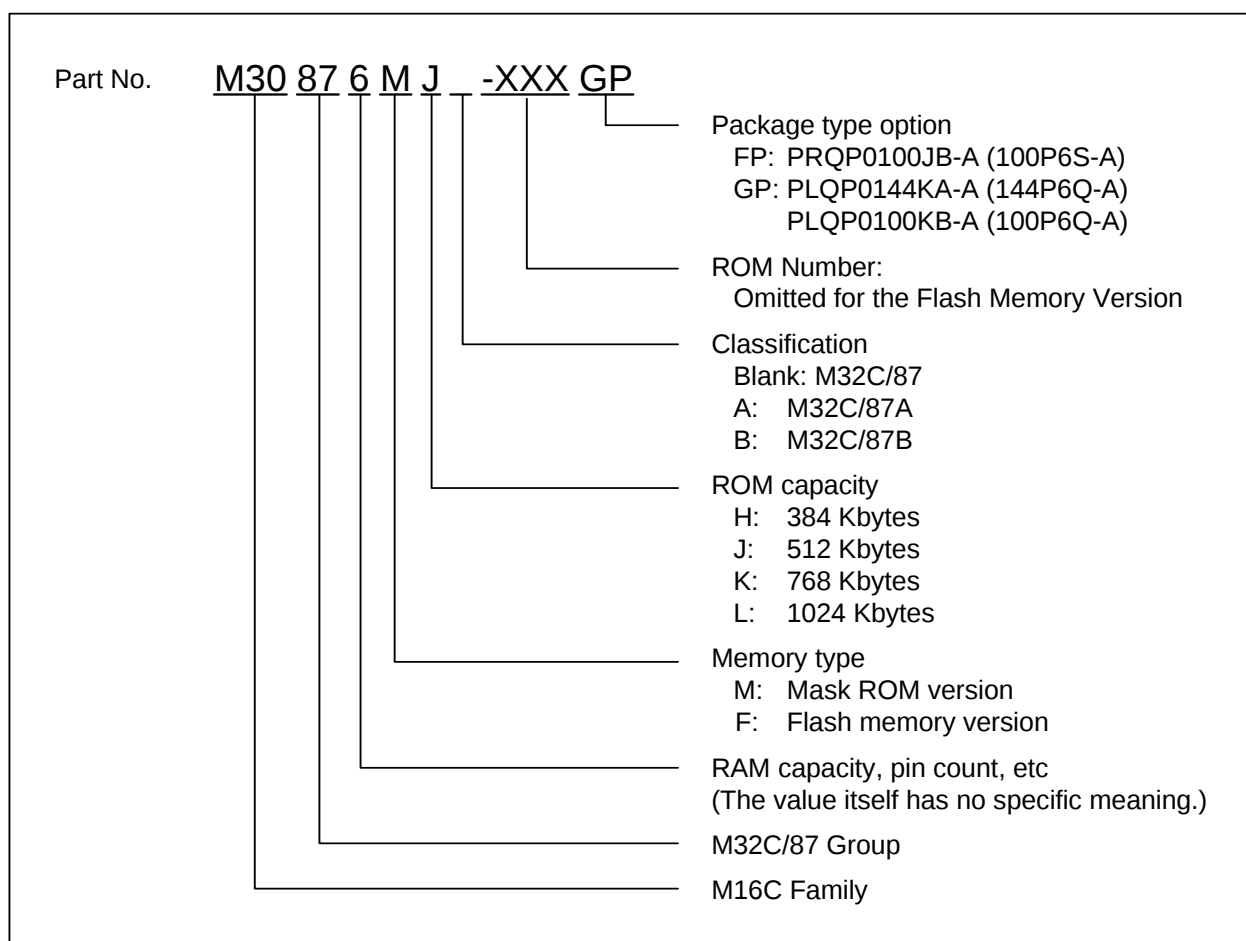
**Figure 1.1 Product Numbering System**

Table 1.8 144-Pin Package List of Pin Names (1/4)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin ⁽¹⁾	Intelligent I/O Pin	Analog Pin	Bus Control Pin
1		P9_6			TXD4/SDA4/SRXD4/ CAN1OUT		ANEX1	
2		P9_5			CLK4/CAN1IN/ <u>CAN1WU</u>		ANEX0	
3		P9_4		TB4IN	CTS4/RTS4/SS4		DA1	
4		P9_3		TB3IN	<u>CTS3</u> /RTS3/SS3		DA0	
5		P9_2		TB2IN	TXD3/SDA3/SRXD3	OUTC2_0/IEOUT/ISTXD2		
6		P9_1		TB1IN	RXD3/SCL3/STXD3	IEIN/ISRXD2		
7		P9_0		TB0IN	CLK3			
8		P14_6	<u>INT8</u>					
9		P14_5	<u>INT7</u>					
10		P14_4	<u>INT6</u>					
11		P14_3				INPC1_7/OUTC1_7		
12		P14_2				INPC1_6/OUTC1_6		
13		P14_1				INPC1_5/OUTC1_5		
14		P14_0				INPC1_4/OUTC1_4		
15	BYTE							
16	CNVSS							
17	XCIN	P8_7						
18	XCOUT	P8_6						
19	<u>RESET</u>							
20	XOUT							
21	VSS							
22	XIN							
23	VCC1							
24		P8_5	<u>NMI</u>					
25		P8_4	<u>INT2</u>					
26		P8_3	<u>INT1</u>		CAN0IN/CAN1IN			
27		P8_2	<u>INT0</u>		CAN0OUT/CAN1OUT			
28		P8_1		TA4IN/ <u>U</u> /RTP2_3	<u>CTS5</u> / <u>RTS5</u>	INPC1_5/OUTC1_5		
29		P8_0		TA4OUT/ <u>U</u>	RXD5	ISRXD0		
30		P7_7		TA3IN/RTP2_2	CLK5/CAN0IN	INPC1_4/OUTC1_4/ ISCLK0		
31		P7_6		TA3OUT	TXD5/CAN0OUT	INPC1_3/OUTC1_3/ ISTXD0		
32		P7_5		TA2IN/ <u>W</u> /RTP2_1		INPC1_2/OUTC1_2/ ISRXD1		
33		P7_4		TA2OUT/ <u>W</u> / RTP2_0		INPC1_1/OUTC1_1/ ISCLK1		
34		P7_3		TA1IN/ <u>V</u>	<u>CTS2</u> / <u>RTS2</u> / <u>SS2</u>	INPC1_0/OUTC1_0/ ISTXD1		
35		P7_2		TA1OUT/ <u>V</u>	CLK2			
36		P7_1		TA0IN/TB5IN/ RTP0_3	RXD2/SCL2/STXD2	INPC1_7/OUTC1_7/ OUTC2_2/ISRXD2/IEIN		
37		P7_0		TA0OUT/RTP0_2	TXD2/SDA2/SRXD2	INPC1_6/OUTC1_6/ OUTC2_0/ISTXD2/IEOUT		
38		P6_7			TXD1/SDA1/SRXD1			
39	VCC1							
40		P6_6			RXD1/SCL1/STXD1			

NOTE:

1. The CAN pins cannot be used in M32C/87B. Only CAN0 pins can be used in M32C/87A.

Table 1.10 144-Pin Package List of Pin Names (3/4)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
81		P3_5						A13,[A13/D13]
82		P3_4						A12,[A12/D12]
83		P3_3						A11,[A11/D11]
84		P3_2						A10,[A10/D10]
85		P3_1						A9,[A9/D9]
86		P12_4						
87		P12_3			CTS6/RTS6			
88		P12_2			RXD6			
89		P12_1			CLK6			
90		P12_0			TXD6			
91	VCC2							
92		P3_0						A8,[A8/D8]
93	VSS							
94		P2_7					AN2_7	A7,[A7/D7]
95		P2_6					AN2_6	A6,[A6/D6]
96		P2_5					AN2_5	A5,[A5/D5]
97		P2_4					AN2_4	A4,[A4/D4]
98		P2_3					AN2_3	A3,[A3/D3]
99		P2_2					AN2_2	A2,[A2/D2]
100		P2_1					AN2_1	A1,[A1/D1]
101		P2_0					AN2_0	A0,[A0/D0]
102		P1_7	INT5					D15
103		P1_6	INT4					D14
104		P1_5	INT3					D13
105		P1_4						D12
106		P1_3						D11
107		P1_2						D10
108		P1_1						D9
109		P1_0						D8
110		P0_7					AN0_7	D7
111		P0_6					AN0_6	D6
112		P0_5					AN0_5	D5
113		P0_4					AN0_4	D4
114		P11_4						
115		P11_3				INPC1_3/OUTC1_3		
116		P11_2				INPC1_2/OUTC1_2/ ISRXD1		
117		P11_1				INPC1_1/OUTC1_1/ ISCLK1		
118		P11_0				INPC1_0/OUTC1_0/ ISTXD1		
119		P0_3					AN0_3	D3
120		P0_2					AN0_2	D2

Table 1.13 100-Pin Package List of Pin Names (2/3)

Pin No.		Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
FP	GP								
41	39		P5_5						HOLD
42	40		P5_4						HLD/ALE
43	41	CLKOUT	P5_3						BCLK/ALE
44	42		P5_2						RD
45	43		P5_1						WRH/BHE
46	44		P5_0						WRL/WR
47	45		P4_7						CS0/A23
48	46		P4_6						CS1/A22
49	47		P4_5						CS2/A21
50	48		P4_4						CS3/A20
51	49		P4_3						A19
52	50		P4_2						A18
53	51		P4_1						A17
54	52		P4_0						A16
55	53		P3_7						A15,[A15/D15]
56	54		P3_6						A14,[A14/D14]
57	55		P3_5						A13,[A13/D13]
58	56		P3_4						A12,[A12/D12]
59	57		P3_3						A11,[A11/D11]
60	58		P3_2						A10,[A10/D10]
61	59		P3_1						A9,[A9/D9]
62	60	VCC2							
63	61		P3_0						A8,[A8/D8]
64	62	VSS							
65	63		P2_7					AN2_7	A7,[A7/D7]
66	64		P2_6					AN2_6	A6,[A6/D6]
67	65		P2_5					AN2_5	A5,[A5/D5]
68	66		P2_4					AN2_4	A4,[A4/D4]
69	67		P2_3					AN2_3	A3,[A3/D3]
70	68		P2_2					AN2_2	A2,[A2/D2]
71	69		P2_1					AN2_1	A1,[A1/D1]
72	70		P2_0					AN2_0	A0,[A0/D0]

4. Special Function Registers (SFRs)

Special Function Registers (SFRs) are the control registers of peripheral functions. Tables 4.1 to 4.20 list SFR address maps.

Table 4.1 SFR Address Map (1/20)

Address	Register	Symbol	After Reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0 ⁽¹⁾	PM0	1000 0000b(CNVSS="L") 0000 0011b(CNVSS="H")
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	0000 1000b
0007h	System Clock Control Register 1	CM1	0010 0000b
0008h			
0009h	Address Match Interrupt Enable Register	AIER	00h
000Ah	Protect Register	PRCR	XXXX 0000b
000Bh	External Data Bus Width Control Register	DS	XXXX 1000b(BYTE="L") XXXX 0000b(BYTE="H")
000Ch	Main Clock Division Register	MCD	XXX0 1000b
000Dh	Oscillation Stop Detection Register	CM2	00h
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDC	00XX XXXXb
0010h			
0011h	Address Match Interrupt Register 0	RMAD0	000000h
0012h			
0013h	Processor Mode Register 2	PM2	00h
0014h	Address Match Interrupt Register 1	RMAD1	000000h
0015h			
0016h			
0017h	Voltage Detection Register 2	VCR2	00h
0018h	Address Match Interrupt Register 2	RMAD2	000000h
0019h			
001Ah			
001Bh	Voltage Detection Register 1	VCR1	0000 1000b
001Ch	Address Match Interrupt Register 3	RMAD3	000000h
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h			
0024h			
0025h			
0026h	PLL Control Register 0	PLC0	0001 X010b
0027h	PLL Control Register 1	PLC1	000X 0000b
0028h	Address Match Interrupt Register 4	RMAD4	000000h
0029h			
002Ah			
002Bh			
002Ch	Address Match Interrupt Register 5	RMAD5	000000h
002Dh			
002Eh			
002Fh	Vdet4 Detection Interrupt Register	D4INT	XX00 0000b

X: Undefined

Blank spaces are all reserved. No access is allowed.

NOTE:

1. Bits PM01 and PM00 in the PM0 register maintain values set before reset, even after software reset or watchdog timer reset has been performed.

Table 4.3 SFR Address Map (3/20)

Address	Register	Symbol	After Reset
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h	DMA0 Interrupt Control Register	DM0IC	XXXX X000b
0069h	Timer B5 Interrupt Control Register	TB5IC	XXXX X000b
006Ah	DMA2 Interrupt Control Register	DM2IC	XXXX X000b
006Bh	UART2 Receive/ACK Interrupt Control Register	S2RIC	XXXX X000b
006Ch	Timer A0 Interrupt Control Register	TA0IC	XXXX X000b
006Dh	UART3 Receive/ACK Interrupt Control Register	S3RIC	XXXX X000b
006Eh	Timer A2 Interrupt Control Register	TA2IC	XXXX X000b
006Fh	UART4 Receive/ACK Interrupt Control Register	S4RIC	XXXX X000b
0070h	Timer A4 Interrupt Control Register	TA4IC	XXXX X000b
0071h	UART0/UART3 Bus Conflict Detection Interrupt Control Register	BCN0IC/BCN3IC	XXXX X000b
0072h	UART0 Receive/ACK Interrupt Control Register	S0RIC	XXXX X000b
0073h	A/D0 Conversion Interrupt Control Register	AD0IC	XXXX X000b
0074h	UART1 Receive/ACK Interrupt Control Register	S1RIC	XXXX X000b
0075h	I/O Interrupt Control Register 0 / CAN1 interrupt Control Register 0	IIO0IC/CAN3IC	XXXX X000b
0076h	Timer B1 Interrupt Control Register	TB1IC	XXXX X000b
0077h	I/O Interrupt Control Register 2	IIO2IC	XXXX X000b
0078h	Timer B3 Interrupt Control Register	TB3IC	XXXX X000b
0079h	I/O Interrupt Control Register 4	IIO4IC	XXXX X000b
007Ah	INT5 Interrupt Control Register	INT5IC	XX00 X000b
007Bh	I/O Interrupt Control Register 6	IIO6IC	XXXX X000b
007Ch	INT3 Interrupt Control Register	INT3IC	XX00 X000b
007Dh	I/O Interrupt Control Register 8	IIO8IC	XXXX X000b
007Eh	INT1 Interrupt Control Register	INT1IC	XX00 X000b
007Fh	I/O Interrupt Control Register 10 / CAN0 Interrupt Control Register 1	IIO10IC/CAN1IC	XXXX X000b
0080h			
0081h	I/O Interrupt Control Register 11 / CAN0 Interrupt Control Register 2	IIO11IC/CAN2IC	XXXX X000b
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h	DMA1 Interrupt Control Register	DM1IC	XXXX X000b
0089h	UART2 Transmit/NACK Interrupt Control Register	S2TIC	XXXX X000b
008Ah	DMA3 Interrupt Control Register	DM3IC	XXXX X000b
008Bh	UART3 Transmit/NACK Interrupt Control Register	S3TIC	XXXX X000b
008Ch	Timer A1 Interrupt Control Register	TA1IC	XXXX X000b
008Dh	UART4 Transmit/NACK Interrupt Control Register	S4TIC	XXXX X000b
008Eh	Timer A3 Interrupt Control Register	TA3IC	XXXX X000b
008Fh	UART2 Bus Conflict Detection Interrupt Control Register	BCN2IC	XXXX X000b

X: Undefined

Blank spaces are all reserved. No access is allowed.

Table 4.4 SFR Address Map (4/20)

Address	Register	Symbol	After Reset
0090h	UART0 Transmit/NACK Interrupt Control Register	S0TIC	XXXX X000b
0091h	UART1/UART4 Bus Conflict Detection Interrupt Control Register	BCN1IC/BCN4IC	XXXX X000b
0092h	UART1 Transmit/NACK Interrupt Control Register	S1TIC	XXXX X000b
0093h	Key Input Interrupt Control Register	KUPIC	XXXX X000b
0094h	Timer B0 Interrupt Control Register	TB0IC	XXXX X000b
0095h	I/O Interrupt Control Register 1 / CAN1 Interrupt Control Register 1	IIO1IC/CAN4IC	XXXX X000b
0096h	Timer B2 Interrupt Control Register	TB2IC	XXXX X000b
0097h	I/O Interrupt Control Register 3	IIO3IC	XXXX X000b
0098h	Timer B4 Interrupt Control Register	TB4IC	XXXX X000b
0099h	I/O Interrupt Control Register 5 / CAN1 Interrupt Control Register 2	IIO5IC/CAN5IC	XXXX X000b
009Ah	INT4 Interrupt Control Register	INT4IC	XX00 X000b
009Bh	I/O Interrupt Control Register 7	IIO7IC	XXXX X000b
009Ch	INT2 Interrupt Control Register	INT2IC	XX00 X000b
009Dh	I/O Interrupt Control Register 9 / CAN0 Interrupt Control Register 0	IIO9IC/CAN0IC	XXXX X000b
009Eh	INT0 Interrupt Control Register	INT0IC	XX00 X000b
009Fh	Exit Priority Register	RLVL	XXXX 0000b
00A0h	Interrupt Request Register 0	IIO0IR	0000 000Xb
00A1h	Interrupt Request Register 1	IIO1IR	0000 000Xb
00A2h	Interrupt Request Register 2	IIO2IR	0000 000Xb
00A3h	Interrupt Request Register 3	IIO3IR	0000 000Xb
00A4h	Interrupt Request Register 4	IIO4IR	0000 000Xb
00A5h	Interrupt Request Register 5	IIO5IR	0000 000Xb
00A6h	Interrupt Request Register 6	IIO6IR	0000 000Xb
00A7h	Interrupt Request Register 7	IIO7IR	0000 000Xb
00A8h	Interrupt Request Register 8	IIO8IR	0000 000Xb
00A9h	Interrupt Request Register 9	IIO9IR	0000 000Xb
00AAh	Interrupt Request Register 10	IIO10IR	0000 000Xb
00ABh	Interrupt Request Register 11	IIO11IR	0000 000Xb
00ACh			
00ADh			
00AEh			
00AFh			
00B0h	Interrupt Enable Register 0	IIO0IE	00h
00B1h	Interrupt Enable Register 1	IIO1IE	00h
00B2h	Interrupt Enable Register 2	IIO2IE	00h
00B3h	Interrupt Enable Register 3	IIO3IE	00h
00B4h	Interrupt Enable Register 4	IIO4IE	00h
00B5h	Interrupt Enable Register 5	IIO5IE	00h
00B6h	Interrupt Enable Register 6	IIO6IE	00h
00B7h	Interrupt Enable Register 7	IIO7IE	00h
00B8h	Interrupt Enable Register 8	IIO8IE	00h
00B9h	Interrupt Enable Register 9	IIO9IE	00h
00BAh	Interrupt Enable Register 10	IIO10IE	00h
00BBh	Interrupt Enable Register 11	IIO11IE	00h
00BCh			
00BDh			
00BEh			
00BFh to 00DFh			

X: Undefined

Blank spaces are all reserved. No access is allowed.

Table 4.5 SFR Address Map (5/20)

Address	Register	Symbol	After Reset
00E0h			
00E1h			
00E2h			
00E3h			
00E4h			
00E5h			
00E6h			
00E7h			
00E8h	Group 0 SI/O Receive Buffer Register	G0RB	XXXX XXXXb
00E9h			XXX0 XXXXb
00EAh	Group 0 Transmit Buffer/Receive Data Register	G0TB/G0DR	XXh
00EBh			
00ECh	Group 0 Receive Input Register	G0RI	XXh
00EDh	Group 0 SI/O Communication Mode Register	G0MR	00h
00EEh	Group 0 Transmit Output Register	G0TO	XXh
00EFh	Group 0 SI/O Communication Control Register	G0CR	0000 X011b
00F0h	Group 0 Data Compare Register 0	G0CMP0	XXh
00F1h	Group 0 Data Compare Register 1	G0CMP1	XXh
00F2h	Group 0 Data Compare Register 2	G0CMP2	XXh
00F3h	Group 0 Data Compare Register 3	G0CMP3	XXh
00F4h	Group 0 Data Mask Register 0	G0MSK0	XXh
00F5h	Group 0 Data Mask Register 1	G0MSK1	XXh
00F6h	Communication Clock Select Register	CCS	XXXX 0000b
00F7h			
00F8h	Group 0 Receive CRC Code Register	G0RCRC	XXXXh
00F9h			
00FAh	Group 0 Transmit CRC Code Register	G0TCRC	0000h
00FBh			
00FCh	Group 0 SI/O Expansion Mode Register	G0EMR	00h
00FDh	Group 0 SI/O Extended Receive Control Register	G0ERC	00h
00FEh	Group 0 SI/O Special Communication Interrupt Detection Register	G0IRF	0000 XXXXb
00FFh	Group 0 SI/O Extended Transmit Control Register	G0ETC	0000 0XXXb
0100h	Group 1 Time Measurement/Waveform Generation Register 0	G1TM0/G1PO0	XXXXh
0101h			
0102h	Group 1 Time Measurement/Waveform Generation Register 1	G1TM1/G1PO1	XXXXh
0103h			
0104h	Group 1 Time Measurement/Waveform Generation Register 2	G1TM2/G1PO2	XXXXh
0105h			
0106h	Group 1 Time Measurement/Waveform Generation Register 3	G1TM3/G1PO3	XXXXh
0107h			
0108h	Group 1 Time Measurement/Waveform Generation Register 4	G1TM4/G1PO4	XXXXh
0109h			
010Ah	Group 1 Time Measurement/Waveform Generation Register 5	G1TM5/G1PO5	XXXXh
010Bh			
010Ch	Group 1 Time Measurement/Waveform Generation Register 6	G1TM6/G1PO6	XXXXh
010Dh			
010Eh	Group 1 Time Measurement/Waveform Generation Register 7	G1TM7/G1PO7	XXXXh
010Fh			
0110h	Group 1 Waveform Generation Control Register 0	G1POCR0	0000 X000b
0111h	Group 1 Waveform Generation Control Register 1	G1POCR1	0X00 X000b
0112h	Group 1 Waveform Generation Control Register 2	G1POCR2	0X00 X000b
0113h	Group 1 Waveform Generation Control Register 3	G1POCR3	0X00 X000b
0114h	Group 1 Waveform Generation Control Register 4	G1POCR4	0X00 X000b
0115h	Group 1 Waveform Generation Control Register 5	G1POCR5	0X00 X000b
0116h	Group 1 Waveform Generation Control Register 6	G1POCR6	0X00 X000b
0117h	Group 1 Waveform Generation Control Register 7	G1POCR7	0X00 X000b
0118h	Group 1 Time Measurement Control Register 0	G1TMCR0	00h
0119h	Group 1 Time Measurement Control Register 1	G1TMCR1	00h

X: Undefined

Blank spaces are all reserved. No access is allowed.

Table 4.6 SFR Address Map (6/20)

Address	Register	Symbol	After Reset
011Ah	Group 1 Time Measurement Control Register 2	G1TMCR2	00h
011Bh	Group 1 Time Measurement Control Register 3	G1TMCR3	00h
011Ch	Group 1 Time Measurement Control Register 4	G1TMCR4	00h
011Dh	Group 1 Time Measurement Control Register 5	G1TMCR5	00h
011Eh	Group 1 Time Measurement Control Register 6	G1TMCR6	00h
011Fh	Group 1 Time Measurement Control Register 7	G1TMCR7	00h
0120h	Group 1 Base Timer Register	G1BT	XXXXh
0121h			
0122h	Group 1 Base Timer Control Register 0	G1BCR0	00h
0123h	Group 1 Base Timer Control Register 1	G1BCR1	X000 000Xb
0124h	Group 1 Time Measurement Prescaler Register 6	G1TPR6	00h
0125h	Group 1 Time Measurement Prescaler Register 7	G1TPR7	00h
0126h	Group 1 Function Enable Register	G1FE	00h
0127h	Group 1 Function Select Register	G1FS	00h
0128h	Group 1 SI/O Receive Buffer Register	G1RB	XXXX XXXXb
0129h			X000 XXXXb
012Ah	Group 1 Transmit Buffer/Receive Data Register	G1TB/G1DR	XXh
012Bh			
012Ch	Group 1 Receive Input Register	G1RI	XXh
012Dh	Group 1 SI/O Communication Mode Register	G1MR	00h
012Eh	Group 1 Transmit Output Register	G1TO	XXh
012Fh	Group 1 SI/O Communication Control Register	G1CR	0000 X011b
0130h	Group 1 Data Compare Register 0	G1CMP0	XXh
0131h	Group 1 Data Compare Register 1	G1CMP1	XXh
0132h	Group 1 Data Compare Register 2	G1CMP2	XXh
0133h	Group 1 Data Compare Register 3	G1CMP3	XXh
0134h	Group 1 Data Mask Register 0	G1MSK0	XXh
0135h	Group 1 Data Mask Register 1	G1MSK1	XXh
0136h			
0137h			
0138h	Group 1 Receive CRC Code Register	G1RCRC	XXXXh
0139h			
013Ah	Group 1 Transmit CRC Code Register	G1TCRC	0000h
013Bh			
013Ch	Group 1 SI/O Expansion Mode Register	G1EMR	00h
013Dh	Group 1 SI/O Extended Receive Control Register	G1ERC	00h
013Eh	Group 1 SI/O Special Communication Interrupt Detection Register	G1IRF	0000 XXXXb
013Fh	Group 1 SI/O Extended Transmit Control Register	G1ETC	0000 0XXXXb
0140h	Group 2 Waveform Generation Register 0	G2PO0	XXXXh
0141h			
0142h	Group 2 Waveform Generation Register 1	G2PO1	XXXXh
0143h			
0144h	Group 2 Waveform Generation Register 2	G2PO2	XXXXh
0145h			
0146h	Group 2 Waveform Generation Register 3	G2PO3	XXXXh
0147h			
0148h	Group 2 Waveform Generation Register 4	G2PO4	XXXXh
0149h			
014Ah	Group 2 Waveform Generation Register 5	G2PO5	XXXXh
014Bh			
014Ch	Group 2 Waveform Generation Register 6	G2PO6	XXXXh
014Dh			
014Eh	Group 2 Waveform Generation Register 7	G2PO7	XXXXh
014Fh			

X: Undefined

Blank spaces are all reserved. No access is allowed.

Table 4.10 SFR Address Map (10/20)

Address	Register ⁽³⁾⁽⁴⁾	Symbol	After Reset
0220h	CAN0 Single Shot Control Register	C0SCTLR	0000h ⁽¹⁾⁽²⁾
0221h			
0222h			
0223h			
0224h	CAN0 Single Shot Status Register	C0SSSTR	0000h ⁽¹⁾⁽²⁾
0225h			
0226h			
0227h			
0228h	CAN0 Global Mask Register Standard ID0	C0GMR0	XXX0 0000b ⁽¹⁾⁽²⁾
0229h	CAN0 Global Mask Register Standard ID1	C0GMR1	XX00 0000b ⁽¹⁾⁽²⁾
022Ah	CAN0 Global Mask Register Extended ID0	C0GMR2	XXXX 0000b ⁽¹⁾⁽²⁾
022Bh	CAN0 Global Mask Register Extended ID1	C0GMR3	00h ⁽¹⁾⁽²⁾
022Ch	CAN0 Global Mask Register Extended ID2	C0GMR4	XX00 0000b ⁽¹⁾⁽²⁾
022Dh			
022Eh			
022Fh			
0230h	CAN0 Message Slot 0 Control Register / CAN0 Local Mask Register A Standard ID0	C0MCTL0 / C0LMAR0	0000 0000b ⁽¹⁾⁽²⁾ / XXX0 0000b ⁽¹⁾⁽²⁾
0231h	CAN0 Message Slot 1 Control Register / CAN0 Local Mask Register A Standard ID1	C0MCTL1 / C0LMAR1	0000 0000b ⁽¹⁾⁽²⁾ / XX00 0000b ⁽¹⁾⁽²⁾
0232h	CAN0 Message Slot 2 Control Register / CAN0 Local Mask Register A Extended ID0	C0MCTL2 / C0LMAR2	0000 0000b ⁽¹⁾⁽²⁾ / XXXX 0000b ⁽¹⁾⁽²⁾
0233h	CAN0 Message Slot 3 Control Register / CAN0 Local Mask Register A Extended ID1	C0MCTL3 / C0LMAR3	00h ⁽¹⁾⁽²⁾ / 00h ⁽¹⁾⁽²⁾
0234h	CAN0 Message Slot 4 Control Register / CAN0 Local Mask Register A Extended ID2	C0MCTL4 / C0LMAR4	0000 0000b ⁽¹⁾⁽²⁾ / XX00 0000b ⁽¹⁾⁽²⁾
0235h	CAN0 Message Slot 5 Control Register	C0MCTL5	00h ⁽¹⁾⁽²⁾
0236h	CAN0 Message Slot 6 Control Register	C0MCTL6	00h ⁽¹⁾⁽²⁾
0237h	CAN0 Message Slot 7 Control Register	C0MCTL7	00h ⁽¹⁾⁽²⁾
0238h	CAN0 Message Slot 8 Control Register / CAN0 Local Mask Register B Standard ID0	C0MCTL8 / C0LMAR0	0000 0000b ⁽¹⁾⁽²⁾ / XXX0 0000b ⁽¹⁾⁽²⁾
0239h	CAN0 Message Slot 9 Control Register / CAN0 Local Mask Register B Standard ID1	C0MCTL9 / C0LMAR1	0000 0000b ⁽¹⁾⁽²⁾ / XX00 0000b ⁽¹⁾⁽²⁾
023Ah	CAN0 Message Slot 10 Control Register / CAN0 Local Mask Register B Extended ID0	C0MCTL10 / C0LMAR2	0000 0000b ⁽¹⁾⁽²⁾ / XXXX 0000b ⁽¹⁾⁽²⁾
023Bh	CAN0 Message Slot 11 Control Register / CAN0 Local Mask Register B Extended ID1	C0MCTL11 / C0LMAR3	00h ⁽¹⁾⁽²⁾ / 00h ⁽¹⁾⁽²⁾
023Ch	CAN0 Message Slot 12 Control Register / CAN0 Local Mask Register B Extended ID2	C0MCTL12 / C0LMAR4	0000 0000b ⁽¹⁾⁽²⁾ / XX00 0000b ⁽¹⁾⁽²⁾
023Dh	CAN0 Message Slot 13 Control Register	C0MCTL13	00h ⁽¹⁾⁽²⁾
023Eh	CAN0 Message Slot 14 Control Register	C0MCTL14	00h ⁽¹⁾⁽²⁾
023Fh	CAN0 Message Slot 15 Control Register	C0MCTL15	00h ⁽¹⁾⁽²⁾
0240h	CAN0 Slot Buffer Select Register	C0SBS	00h ⁽²⁾
0241h	CAN0 Control Register 1	C0CTLR1	X000 00XXb ⁽²⁾
0242h	CAN0 Sleep Control Register	C0SLPR	XXXX XXX0b
0243h			
0244h	CAN0 Acceptance Filter Support Register	C0AFS	0000 0000b ⁽²⁾ 0000 0001b ⁽²⁾
0245h			
0246h			
0247h			
0248h			
0249h			
024Ah to 024Fh			

X: Undefined

Blank spaces are all reserved. No access is allowed.

NOTES:

1. The BANKSEL bit in the C0CTLR1 register can switch functions for addresses 0220h to 023Fh.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) after reset and supplying a clock to the CAN module.
3. The CAN-associated registers (allocated in addresses 01E0h to 02BFh) cannot be used in M32C/87B. In M32C/87A, only CAN0-associated registers can be used.
4. Set the PM13 bit in the PM1 register to 1 (2 wait states for SFR area) before accessing the CAN-associated registers.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter		Condition	Value	Unit
VCC1, VCC2	Supply voltage		VCC1 = AVCC	-0.3 to 6.0	V
VCC2	Supply voltage		–	-0.3 to VCC1 + 0.1	V
AVCC	Analog supply voltage		VCC1 = AVCC	-0.3 to 6.0	V
VI	Input voltage	RESET, CNVSS, BYTE, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P14_0 to P14_6, P15_0 to P15_7 ⁽¹⁾ , VREF, XIN		-0.3 to VCC1 + 0.3	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7 ⁽¹⁾		-0.3 to VCC2 + 0.3	
		P7_0, P7_1		-0.3 to 6.0	
VO	Output voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P14_0 to P14_6, P15_0 to P15_7 ⁽¹⁾ , XOUT		-0.3 to VCC1 + 0.3	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7 ⁽¹⁾		-0.3 to VCC2 + 0.3	
		P7_0, P7_1		-0.3 to 6.0	
Pd	Power consumption		-40°C ≤ Topr ≤ 85°C	500	mW
Topr	Operating ambient temperature	during CPU operation		-20 to 85/ -40 to 85 ⁽²⁾	°C
		during programming or erasing Flash memory		0 to 60	°C
Tstg	Storage temperature			-65 to 150	°C

NOTES:

1. P11 to P15 are provided in the 144-pin package only.
2. Contact a Renesas sales office if temperature range of -40 to 85°C is required.

Table 5.3 Recommended Operating Conditions (2/3)
(VCC1 = VCC2 = 3.0 to 5.5 V, Topr = -20 to 85°C unless otherwise specified)

Symbol	Parameter	Standard			Unit
		Min.	Typ.	Max.	
IOH(peak)	Peak output high "H" current ⁽²⁾			-10.0	mA
IOH(avg)	Average output high "H" current ⁽¹⁾			-5.0	mA
IOL(peak)	Peak output low "L" current ⁽²⁾			10.0	mA
IOL(avg)	Average output low "L" current ⁽¹⁾			5.0	mA

NOTES:

1. Average output current is the average value within 100 ms.
2. A total IOL(peak) of P0, P1, P2, P8_6, P8_7, P9, P10, P11, P14, and P15 must be 80 mA or less.
A total IOL(peak) of P3, P4, P5, P6, P7, P8_0 to P8_4, P12, and P13 must be 80 mA or less.
A total IOH(peak) of P0, P1, P2, and P11 must be -40 mA or less.
A total IOH(peak) of P8_6 to P8_7, P9, P10, P14, and P15 must be -40 mA or less.
A total IOH(peak) of P3, P4, P5, P12, and P13 must be -40 mA or less.
A total IOH(peak) of P6, P7, and P8_0 to P8_4 must be -40 mA or less.
3. P11 to P15 are provided in the 144-pin package only.

$$VCC1 = VCC2 = 5V$$

Timing Requirements

(VCC1 = VCC2 = 4.2 to 5.5 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.13 External Clock Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc	External clock input cycle time	31.25		ns
tw(H)	External clock input high ("H") pulse width	13.75		ns
tw(L)	External clock input low ("L") pulse width	13.75		ns
tr	External clock rise time		5	ns
tf	External clock fall time		5	ns

Table 5.14 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	100		ns
tw(TAH)	TAiIN input high ("H") pulse width	40		ns
tw(TAL)	TAiIN input low ("L") pulse width	40		ns

i = 0 to 4

Table 5.15 Timer A Input (Gate Signal Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	400		ns
tw(TAH)	TAiIN input high ("H") pulse width	200		ns
tw(TAL)	TAiIN input low ("L") pulse width	200		ns

i = 0 to 4

Table 5.16 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	200		ns
tw(TAH)	TAiIN input high ("H") pulse width	100		ns
tw(TAL)	TAiIN input low ("L") pulse width	100		ns

i = 0 to 4

Table 5.17 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tw(TAH)	TAiIN input high ("H") pulse width	100		ns
tw(TAL)	TAiIN input low ("L") pulse width	100		ns

i = 0 to 4

$$VCC1 = VCC2 = 5V$$

Timing Requirements

(VCC1 = VCC2 = 4.2 to 5.5 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.18 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(UP)	TAiOUT input cycle time	2000		ns
tw(UPH)	TAiOUT input high ("H") pulse width	1000		ns
tw(UPL)	TAiOUT input low ("L") pulse width	1000		ns
tsu(UP-TIN)	TAiOUT input setup time	400		ns
th(TIN-UP)	TAiOUT input hold time	400		ns

i = 0 to 4

Table 5.19 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	800		ns
tsu(TAIN-TAOUT)	TAiOUT input setup time	200		ns
tsu(TAOUT-TAIN)	TAiIN input setup time	200		ns

i = 0 to 4

Table 5.20 Timer B Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TB)	TBiIN input cycle time (counted on one edge)	100		ns
tw(TBH)	TBiIN input high ("H") pulse width (counted on one edge)	40		ns
tw(TBL)	TBiIN input low ("L") pulse width (counted on one edge)	40		ns
tc(TB)	TBiIN input cycle time (counted on both edges)	200		ns
tw(TBH)	TBiIN input high ("H") pulse width (counted on both edges)	80		ns
tw(TBL)	TBiIN input low ("L") pulse width (counted on both edges)	80		ns

i = 0 to 5

Table 5.21 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TB)	TBiIN input cycle time	400		ns
tw(TBH)	TBiIN input high ("H") pulse width	200		ns
tw(TBL)	TBiIN input low ("L") pulse width	200		ns

i = 0 to 5

Table 5.22 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TB)	TBiIN input cycle time	400		ns
tw(TBH)	TBiIN input high ("H") pulse width	200		ns
tw(TBL)	TBiIN input low ("L") pulse width	200		ns

i = 0 to 5

$$VCC1 = VCC2 = 5V$$

Timing Requirements

(VCC1 = VCC2 = 4.2 to 5.5 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.23 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(AD)	ADTRG input cycle time (required for trigger)	1000		ns
tw(ADL)	ADTRG input low ("L") pulse width	125		ns

Table 5.24 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CK)	CLKi input cycle time	200		ns
tw(CKH)	CLKi input high ("H") pulse width	100		ns
tw(CKL)	CLKi input low ("L") pulse width	100		ns
td(C-Q)	TXDi output delay time		80	ns
th(C-Q)	TXDi output hold time	0		ns
tsu(D-C)	RXDi input setup time	70		ns
th(C-D)	RXDi input hold time	90		ns

i = 0 to 6

Table 5.25 Intelligent I/O Communication Function (Groups 0 and 1)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CK)	ISCLKi input cycle time	600		ns
tw(CKH)	ISCLKi input high ("H") pulse width	300		ns
tw(CKL)	ISCLKi input low ("L") pulse width	300		ns
td(C-Q)	ISTXDi output delay time		100	ns
th(C-Q)	ISTXDi output hold time	0		ns
tsu(D-C)	ISRXDi input setup time	100		ns
th(C-D)	ISRXDi input hold time	100		ns

i = 0, 1

Table 5.26 Intelligent I/O Communication Function (Group 2)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CK)	ISCLK2 input cycle time	600		ns
tw(CKH)	ISCLK2 input high ("H") pulse width	300		ns
tw(CKL)	ISCLK2 input low ("L") pulse width	300		ns
td(C-Q)	ISTXD2 output delay time		180	ns
th(C-Q)	ISTXD2 output hold time	0		ns
tsu(D-C)	ISRXD2 input setup time	150		ns
th(C-D)	ISRXD2 input hold time	100		ns

$$VCC1 = VCC2 = 5V$$

Switching Characteristics

(VCC1 = VCC2 = 4.2 to 5.5 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.29 Memory Expansion Mode and Microprocessor Mode (when accessing external memory space)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min.	Max.	
td(BCLK-AD)	Address output delay time	See Figure 5.2		18	ns
th(BCLK-AD)	Address output hold time (BCLK standard)		-3		ns
th(RD-AD)	Address output hold time (RD standard) ⁽³⁾		0		ns
th(WR-AD)	Address output hold time (WR standard) ⁽³⁾		(note 1)		ns
td(BCLK-CS)	Chip-select signal output delay time			18	ns
th(BCLK-CS)	Chip-select signal output hold time (BCLK standard)		-3		ns
th(RD-CS)	Chip-select signal output hold time (RD standard) ⁽³⁾		0		ns
th(WR-CS)	Chip-select signal output hold time (WR standard) ⁽³⁾		(note 1)		ns
td(BCLK-RD)	RD signal output delay time			18	ns
th(BCLK-RD)	RD signal output hold time		-5		ns
td(BCLK-WR)	WR signal output delay time			18	ns
th(BCLK-WR)	WR signal output hold time		-5		ns
td(DB-WR)	Data output delay time (WR standard)		(note 2)		ns
th(WR-DB)	Data output hold time (WR standard) ⁽³⁾		(note 1)		ns
tw(WR)	WR output width		(note 2)		ns

NOTES:

- Values, which depend on BCLK frequency, can be obtained from the following equations.

$$th(WR-DB) = \frac{10^9}{f(BCLK) \times 2} - 15 \text{ [ns]}$$

$$th(WR-AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \text{ [ns]}$$

$$th(WR-CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \text{ [ns]}$$

- Values, which depend on BCLK frequency and external bus cycles, can be obtained from the following equations.

$$td(DB-WR) = \frac{10^9 \times m}{f(BCLK)} - 20 \text{ [ns]} \text{ (if external bus cycle is } a\phi + b\phi, m = b)$$

$$tw(WR) = \frac{10^9 \times n}{f(BCLK) \times 2} - 15 \text{ [ns]} \text{ (if external bus cycle is } a\phi + b\phi, n = (b \times 2) - 1)$$

- tc [ns] is added when recovery cycle is inserted.

$$VCC1 = VCC2 = 3.3 \text{ V}$$

Timing Requirements

(VCC1 = VCC2 = 3.0 to 3.6 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.51 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tac1(RD-DB)	Data input access time (RD standard)		(note 1)	ns
tac1(AD-DB)	Data input access time (AD standard, CS standard)		(note 1)	ns
tac2(RD-DB)	Data input access time (RD standard, when accessing a space with the multiplexed bus)		(note 1)	ns
tac2(AD-DB)	Data input access time (AD standard, when accessing a space with the multiplexed bus)		(note 1)	ns
tsu(DB-BCLK)	Data input setup time	30		ns
tsu(RDY-BCLK)	$\overline{\text{RDY}}$ input setup time	40		ns
tsu(HOLD-BCLK)	$\overline{\text{HOLD}}$ input setup time	60		ns
th(RD-DB)	Data input hold time	0		ns
th(BCLK-RDY)	$\overline{\text{RDY}}$ input hold time	0		ns
th(BCLK-HOLD)	$\overline{\text{HOLD}}$ input hold time	0		ns
td(BCLK-HLDA)	$\overline{\text{HLDA}}$ output delay time		25	ns

NOTE:

- Values, which depend on BCLK frequency and external bus cycles, can be obtained from the following equations. Insert wait states or lower the operation frequency, f(BCLK), if the calculated value is negative.

$$tac1(RD-DB) = \frac{10^9 \times m}{f(BCLK) \times 2} - 35 \text{ [ns]} \text{ (if external bus cycle is } a\phi + b\phi, m = (b \times 2) + 1)$$

$$tac1(AD-DB) = \frac{10^9 \times n}{f(BCLK)} - 35 \text{ [ns]} \text{ (if external bus cycle is } a\phi + b\phi, n = a + b)$$

$$tac2(RD-DB) = \frac{10^9 \times m}{f(BCLK) \times 2} - 35 \text{ [ns]} \text{ (if external bus cycle is } a\phi + b\phi, m = (b \times 2) - 1)$$

$$tac2(AD-DB) = \frac{10^9 \times p}{f(BCLK) \times 2} - 35 \text{ [ns]} \text{ (if external bus cycle is } a\phi + b\phi, p = \{(a + b - 1) \times 2\} + 1)$$

REVISION HISTORY		M32C/87 Group Datasheet	
Rev.	Date	Description	
		Page	Summary
		46	Special Function Registers (SFRs) • Table 4.20 A value of After Reset column in 03FFh modified

All trademarks and registered trademarks are the property of their respective owners.
 IEBus is a registered trademark of NEC Electronics Corporation.

Notes:

1. This document is provided for reference purposes only so that Renesas customers may select the appropriate Renesas products for their use. Renesas neither makes warranties or representations with respect to the accuracy or completeness of the information contained in this document nor grants any license to any intellectual property rights or any other rights of Renesas or any third party with respect to the information in this document.
2. Renesas shall have no liability for damages or infringement of any intellectual property or other rights arising out of the use of any information in this document, including, but not limited to, product data, diagrams, charts, programs, algorithms, and application circuit examples.
3. You should not use the products or the technology described in this document for the purpose of military applications such as the development of weapons of mass destruction or for the purpose of any other military use. When exporting the products or technology described herein, you should follow the applicable export control laws and regulations, and procedures required by such laws and regulations.
4. All information included in this document such as product data, diagrams, charts, programs, algorithms, and application circuit examples, is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas products listed in this document, please confirm the latest product information with a Renesas sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas such as that disclosed through our website. (<http://www.renesas.com>)
5. Renesas has used reasonable care in compiling the information included in this document, but Renesas assumes no liability whatsoever for any damages incurred as a result of errors or omissions in the information included in this document.
6. When using or otherwise relying on the information in this document, you should evaluate the information in light of the total system before deciding about the applicability of such information to the intended application. Renesas makes no representations, warranties or guarantees regarding the suitability of its products for any particular application and specifically disclaims any liability arising out of the application and use of the information in this document or Renesas products.
7. With the exception of products specified by Renesas as suitable for automobile applications, Renesas products are not designed, manufactured or tested for applications or otherwise in systems the failure or malfunction of which may cause a direct threat to human life or create a risk of human injury or which require especially high quality and reliability such as safety systems, or equipment or systems for transportation and traffic, healthcare, combustion control, aerospace and aeronautics, nuclear power, or undersea communication transmission. If you are considering the use of our products for such purposes, please contact a Renesas sales office beforehand. Renesas shall have no liability for damages arising out of the uses set forth above.
8. Notwithstanding the preceding paragraph, you should not use Renesas products for the purposes listed below:
 - (1) artificial life support devices or systems
 - (2) surgical implantations
 - (3) healthcare intervention (e.g., excision, administration of medication, etc.)
 - (4) any other purposes that pose a direct threat to human lifeRenesas shall have no liability for damages arising out of the uses set forth in the above and purchasers who elect to use Renesas products in any of the foregoing applications shall indemnify and hold harmless Renesas Technology Corp., its affiliated companies and their officers, directors, and employees against any and all damages arising out of such applications.
9. You should use the products described herein within the range specified by Renesas, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas shall have no liability for malfunctions or damages arising out of the use of Renesas products beyond such specified ranges.
10. Although Renesas endeavors to improve the quality and reliability of its products, IC products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Please be sure to implement safety measures to guard against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other applicable measures. Among others, since the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
11. In case Renesas products listed in this document are detached from the products to which the Renesas products are attached or affixed, the risk of accident such as swallowing by infants and small children is very high. You should implement safety measures so that Renesas products may not be easily detached from your products. Renesas shall have no liability for damages arising out of such detachment.
12. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written approval from Renesas.
13. Please contact a Renesas sales office if you have any questions regarding the information contained in this document, Renesas semiconductor products, or if you have any other inquiries.



RENESAS SALES OFFICES

<http://www.renesas.com>

Refer to "<http://www.renesas.com/en/network>" for the latest and detailed information.

Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7858/7898

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2377-3473

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 3518-3399

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.
Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510