Renesas Electronics America Inc - M30875FHAGP#U3 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M32C/80
Core Size	16/32-Bit
Speed	32MHz
Connectivity	CANbus, EBI/EMI, I²C, IEBus, IrDA, SIO, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	121
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 34x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30875fhagp-u3

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Table 4.8 SFR Address Map (8/20)

Address	Register	Symbol	After Reset
01C0h	UART5 Transmit/Receive Mode Register	U5MR	00h
01C1h	UART5 Baud Rate Register	U5BRG	XXh
01C2h	UART5 Transmit Buffer Register	U5TB	XXXXh
01C3h			
01C4h	UART5 Transmit/Receive Control Register 0	U5C0	0000 1000b
01C5h	UART5 Transmit/Receive Control Register 1	U5C1	XXXX 0010b
01C6h	UART5 Receive Buffer Register	U5RB	XXXXh
01C7h			
01C8h	UART6 Transmit/Receive Mode Register	U6MR	00h
01C9h	UART6 Baud Rate Register	U6BRG	XXh
01CAh	UART6 Transmit Buffer Register	U6TB	XXXXh
01CBh			
01CCh	UART6 Transmit/Receive Control Register 0	U6C0	0000 1000b
01CDh	UART6 Transmit/Receive Control Register 1	U6C1	XXXX 0010b
01CEh	UART6 Receive Buffer Register	U6RB	XXXXh
01CFh			
01D0h	UART5, UART6 Transmit/Receive Control Register	U56CON	X000 0000b
01D1h	UART5, UART6 Input Pin Function Select Register	U56IS	X000 X000b
01D2h			
01D3h			
01D4h			
01D5h			
01D6h			
01D7h			
01D8h	RTP Output Buffer Register 0	RTP0R	XXh
01D9h	RTP Output Buffer Register 1	RTP1R	XXh
01DAh	RTP Output Buffer Register 2	RTP2R	XXh
01DBh	RTP Output Buffer Register 3	RTP3R	XXh
01DCh			
01DDh			
01DEh			
01DFh			
01E0h	CAN0 Message Slot Buffer 0 Standard ID0(1)(2)	C0SLOT0_0	XXh
01E1h	CAN0 Message Slot Buffer 0 Standard ID1(1)(2)	C0SLOT0_1	XXh
01E2h	CAN0 Message Slot Buffer 0 Extended ID0(1)(2)	C0SLOT0_2	XXh
01E3h	CAN0 Message Slot Buffer 0 Extended ID1(1)(2)	C0SLOT0_3	XXh
01E4h	CAN0 Message Slot Buffer 0 Extended ID2(1)(2)	C0SLOT0_4	XXh
01E5h	CAN0 Message Slot Buffer 0 Data Length Code(1)(2)	C0SLOT0_5	XXh
01E6h	CAN0 Message Slot Buffer 0 Data 0(1)(2)	C0SLOT0_6	XXh
01E7h	CAN0 Message Slot Buffer 0 Data 1(1)(2)	C0SLOT0_7	XXh
01E8h	CAN0 Message Slot Buffer 0 Data 2(1)(2)	C0SLOT0_8	XXh
01E9h	CAN0 Message Slot Buffer 0 Data 3(1)(2)	C0SLOT0_9	XXh
01EAh	CAN0 Message Slot Buffer 0 Data 4(1)(2)	C0SLOT0_10	XXh
01EBh	CAN0 Message Slot Buffer 0 Data 5(1)(2)	C0SLOT0_11	XXh
01ECh	CAN0 Message Slot Buffer 0 Data 6(1)(2)	C0SLOT0_12	XXh
01EDh	CAN0 Message Slot Buffer 0 Data 7(1)(2)	C0SLOT0_13	XXh
01EEh	CAN0 Message Slot Buffer 0 Time Stamp High-Order(1)(2)	C0SLOT0_14	XXh
01EFh	CAN0 Message Slot Buffer 0 Time Stamp Low-Order(1)(2)	C0SLOT0_15	XXh

X: Undefined
Blank spaces are all reserved. No access is allowed.

NOTES:

1. The CAN-associated registers (allocated in addresses 01E0h to 02BFh) cannot be used in M32C/87B. In M32C/87A, only CAN0-associated registers can be used.
2. Set the PM13 bit in the PM1 register to 1 (2 wait states for SFR area) before accessing the CAN-associated registers.

Table 4.14 SFR Address Map (14/20)

Address	Register	Symbol	After Reset
02C0h	X0 Register, Y0 Register	X0R, Y0R	XXXXh
02C1h			
02C2h	X1 Register, Y1 Register	X1R, Y1R	XXXXh
02C3h			
02C4h	X2 Register, Y2 Register	X2R, Y2R	XXXXh
02C5h			
02C6h	X3 Register, Y3 Register	X3R, Y3R	XXXXh
02C7h			
02C8h	X4 Register, Y4 Register	X4R, Y4R	XXXXh
02C9h			
02CAh	X5 Register, Y5 Register	X5R, Y5R	XXXXh
02CBh			
02CCh	X6 Register, Y6 Register	X6R, Y6R	XXXXh
02CDh			
02CEh	X7 Register, Y7 Register	X7R, Y7R	XXXXh
02CFh			
02D0h	X8 Register, Y8 Register	X8R, Y8R	XXXXh
02D1h			
02D2h	X9 Register, Y9 Register	X9R, Y9R	XXXXh
02D3h			
02D4h	X10 Register, Y10 Register	X10R, Y10R	XXXXh
02D5h			
02D6h	X11 Register, Y11 Register	X11R, Y11R	XXXXh
02D7h			
02D8h	X12 Register, Y12 Register	X12R, Y12R	XXXXh
02D9h			
02DAh	X13 Register, Y13 Register	X13R, Y13R	XXXXh
02DBh			
02DCh	X14 Register, Y14 Register	X14R, Y14R	XXXXh
02DDh			
02DEh	X15 Register, Y15 Register	X15R, Y15R	XXXXh
02DFh			
02E0h	X/Y Control Register	XYC	XXXX XX00b
02E1h			
02E2h			
02E3h			
02E4h	UART1 Special Mode Register 4	U1SMR4	00h
02E5h	UART1 Special Mode Register 3	U1SMR3	00h
02E6h	UART1 Special Mode Register 2	U1SMR2	00h
02E7h	UART1 Special Mode Register	U1SMR	00h
02E8h	UART1 Transmit/Receive Mode Register	U1MR	00h
02E9h	UART1 Baud Rate Register	U1BRG	XXh
02EAh	UART1 Transmit Buffer Register	U1TB	XXXXh
02EBh			
02ECh	UART1 Transmit/Receive Control Register 0	U1C0	0000 1000b
02EDh	UART1 Transmit/Receive Control Register 1	U1C1	0000 0010b
02EEh	UART1 Receive Buffer Register	U1RB	XXXXh
02EFh			

X: Undefined
Blank spaces are all reserved. No access is allowed.

Table 4.15 SFR Address Map (15/20)

Address	Register	Symbol	After Reset
02F0h			
02F1h			
02F2h			
02F3h			
02F4h	UART4 Special Mode Register 4	U4SMR4	00h
02F5h	UART4 Special Mode Register 3	U4SMR3	00h
02F6h	UART4 Special Mode Register 2	U4SMR2	00h
02F7h	UART4 Special Mode Register	U4SMR	00h
02F8h	UART4 Transmit/Receive Mode Register	U4MR	00h
02F9h	UART4 Baud Rate Register	U4BRG	XXh
02FAh	UART4 Transmit Buffer Register	U4TB	XXXXh
02FBh			
02FCh	UART4 Transmit/Receive Control Register 0	U4C0	0000 1000b
02FDh	UART4 Transmit/Receive Control Register 1	U4C1	0000 0010b
02FEh	UART4 Receive Buffer Register	U4RB	XXXXh
02FFh			
0300h	Timer B3, B4, B5 Count Start Register	TBSR	000X XXXXb
0301h			
0302h	Timer A11 Register	TA11	XXXXh
0303h			
0304h	Timer A21 Register	TA21	XXXXh
0305h			
0306h	Timer A41 Register	TA41	XXXXh
0307h			
0308h	Three-Phase PWM Control Register 0	INVC0	00h
0309h	Three-Phase PWM Control Register 1	INVC1	00h
030Ah	Three-Phase Output Buffer Register 0	IDB0	XX11 1111b
030Bh	Three-Phase Output Buffer Register 1	IDB1	XX11 1111b
030Ch	Dead Time Timer	DTT	XXh
030Dh	Timer B2 Interrupt Generation Frequency Set Counter	ICTB2	XXh
030Eh			
030Fh			
0310h	Timer B3 Register	TB3	XXXXh
0311h			
0312h	Timer B4 Register	TB4	XXXXh
0313h			
0314h	Timer B5 Register	TB5	XXXXh
0315h			
0316h			
0317h			
0318h			
0319h			
031Ah			
031Bh	Timer B3 Mode Register	TB3MR	00XX 0000b
031Ch	Timer B4 Mode Register	TB4MR	00XX 0000b
031Dh	Timer B5 Mode Register	TB5MR	00XX 0000b
031Eh	External Interrupt Source Select Register 1(1)	IFSRA	00h
031Fh	External Interrupt Source Select Register	IFSR	00h

X: Undefined
Blank spaces are all reserved. No access is allowed.
NOTE:
1. The IFSRA register is included in the 144-pin package only.

Table 4.16 SFR Address Map (16/20)

Address	Register	Symbol	After Reset
0320h			
0321h			
0322h			
0323h			
0324h	UART3 Special Mode Register 4	U3SMR4	00h
0325h	UART3 Special Mode Register 3	U3SMR3	00h
0326h	UART3 Special Mode Register 2	U3SMR2	00h
0327h	UART3 Special Mode Register	U3SMR	00h
0328h	UART3 Transmit/Receive Mode Register	U3MR	00h
0329h	UART3 Baud Rate Register	U3BRG	XXh
032Ah	UART3 Transmit Buffer Register	U3TB	XXXXh
032Bh			
032Ch	UART3 Transmit/Receive Control Register 0	U3C0	0000 1000b
032Dh	UART3 Transmit/Receive Control Register 1	U3C1	0000 0010b
032Eh	UART3 Receive Buffer Register	U3RB	XXXXh
032Fh			
0330h			
0331h			
0332h			
0333h			
0334h	UART2 Special Mode Register 4	U2SMR4	00h
0335h	UART2 Special Mode Register 3	U2SMR3	00h
0336h	UART2 Special Mode Register 2	U2SMR2	00h
0337h	UART2 Special Mode Register	U2SMR	00h
0338h	UART2 Transmit/Receive Mode Register	U2MR	00h
0339h	UART2 Baud Rate Register	U2BRG	XXh
033Ah	UART2 Transmit Buffer Register	U2TB	XXXXh
033Bh			
033Ch	UART2 Transmit/Receive Control Register 0	U2C0	0000 1000b
033Dh	UART2 Transmit/Receive Control Register 1	U2C1	0000 0010b
033Eh	UART2 Receive Buffer Register	U2RB	XXXXh
033Fh			
0340h	Count Start Register	TABSR	00h
0341h	Clock Prescaler Reset Register	CPSRF	0XXX XXXXb
0342h	One-Shot Start Register	ONSF	00h
0343h	Trigger Select Register	TRGSR	00h
0344h	Up/Down Select Register	UDF	00h
0345h			
0346h	Timer A0 Register	TA0	XXXXh
0347h			
0348h	Timer A1 Register	TA1	XXXXh
0349h			
034Ah	Timer A2 Register	TA2	XXXXh
034Bh			
044Ch	Timer A3 Register	TA3	XXXXh
034Dh			
034Eh	Timer A4 Register	TA4	XXXXh
034Fh			

X: Undefined
Blank spaces are all reserved. No access is allowed.

Table 4.17 SFR Address Map (17/20)

Address	Register	Symbol	After Reset
0350h	Timer B0 Register	TB0	XXXXh
0351h			
0352h	Timer B1 Register	TB1	XXXXh
0353h			
0354h	Timer B2 Register	TB2	XXXXh
0355h			
0356h	Timer A0 Mode Register	TA0MR	00h
0357h	Timer A1 Mode Register	TA1MR	00h
0358h	Timer A2 Mode Register	TA2MR	00h
0359h	Timer A3 Mode Register	TA3MR	00h
035Ah	Timer A4 Mode Register	TA4MR	00h
035Bh	Timer B0 Mode Register	TB0MR	00XX 0000b
035Ch	Timer B1 Mode Register	TB1MR	00XX 0000b
035Dh	Timer B2 Mode Register	TB2MR	00XX 0000b
035Eh	Timer B2 Special Mode Register	TB2SC	XXXX XXX0b
035Fh	Count Source Prescaler Register(1)	TCSPR	0XXX 0000b
0360h			
0361h			
0362h			
0363h			
0364h	UART0 Special Mode Register 4	U0SMR4	00h
0365h	UART0 Special Mode Register 3	U0SMR3	00h
0366h	UART0 Special Mode Register 2	U0SMR2	00h
0367h	UART0 Special Mode Register	U0SMR	00h
0368h	UART0 Transmit/Receive Mode Register	U0MR	00h
0369h	UART0 Baud Rate Register	U0BRG	XXh
036Ah	UART0 Transmit Buffer Register	U0TB	XXXXh
036Bh			
036Ch	UART0 Transmit/Receive Control Register 0	U0C0	0000 1000b
036Dh	UART0 Transmit/Receive Control Register 1	U0C1	0000 0010b
036Eh	UART0 Receive Buffer Register	U0RB	XXXXh
036Fh			
0370h			
0371h			
0372h	IrDA Control Register	IRCON	X000 0000b
0373h			
0374h			
0375h			
0376h			
0377h			
0378h	DMA0 Request Source Select Register	DM0SL	0X00 0000b
0379h	DMA1 Request Source Select Register	DM1SL	0X00 0000b
037Ah	DMA2 Request Source Select Register	DM2SL	0X00 0000b
037Bh	DMA3 Request Source Select Register	DM3SL	0X00 0000b
037Ch	CRC Data Register	CRCD	XXXXh
037Dh			
037Eh	CRC Input Register	CRCIN	XXh
037Fh			

X: Undefined
Blank spaces are all reserved. No access is allowed.
NOTE:
1. The TCSPR register maintains values set before reset, even after software reset or watchdog timer reset has been performed.

Table 4.18 SFR Address Map (18/20)

Address	Register	Symbol	After Reset
0380h	A/D0 Register 0	AD00	00XXh
0381h			
0382h	A/D0 Register 1	AD01	00XXh
0383h			
0384h	A/D0 Register 2	AD02	00XXh
0385h			
0386h	A/D0 Register 3	AD03	00XXh
0387h			
0388h	A/D0 Register 4	AD04	00XXh
0389h			
038Ah	A/D0 Register 5	AD05	00XXh
038Bh			
038Ch	A/D0 Register 6	AD06	00XXh
038Dh			
038Eh	A/D0 Register 7	AD07	00XXh
038Fh			
0390h			
0391h			
0392h	A/D0 Control Register 4	AD0CON4	XXXX 00XXb
0393h			
0394h	A/D0 Control Register 2	AD0CON2	XX0X X000b
0395h	A/D0 Control Register 3	AD0CON3	XXXX X000b
0396h	A/D0 Control Register 0	AD0CON0	00h
0397h	A/D0 Control Register 1	AD0CON1	00h
0398h	D/A Register 0	DA0	XXh
0399h			
039Ah	D/A Register 1	DA1	XXh
039Bh			
039Ch	D/A Control Register	DACON	XXXX XX00b
039Dh	D/A Control Register 1	DACON1	XXXX 0000b
039Eh			
039Fh			

X: Undefined
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Table 5.2 Recommended Operating Conditions (1/3)
(VCC1 = VCC2 = 3.0 to 5.5 V, Topr = -20 to 85°C unless otherwise specified)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
VCC1, VCC2	Supply voltage (VCC1 ≥ VCC2)		3.0	5.0	5.5	V
AVCC	Analog supply voltage			VCC1		V
VSS	Supply voltage			0		V
AVSS	Analog supply voltage			0		V
VIH	Input high “H” voltage	P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7(2)	0.8VCC2		VCC2	V
		P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7(1), P9_0 to P9_7, P10_0 to P10_7, P14_0 to P14_6, P15_0 to P15_7(2), XIN, $\overline{\text{RESET}}$, CNVSS, BYTE	0.8VCC1		VCC1	
		P7_0, P7_1	0.8VCC1		6.0	
		P0_0 to P0_7, P1_0 to P1_7 (in single-chip mode)	0.8VCC2		VCC2	
		P0_0 to P0_7, P1_0 to P1_7 (in memory expansion mode and microprocessor mode)	0.5VCC2		VCC2	
VIL	Input low “L” voltage	P2_0 to P2_7,P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7(2)	0		0.2VCC2	V
		P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7(1), P9_0 to P9_7, P10_0 to P10_7, P14_0 to P14_6, P15_0 to P15_7(2), XIN, $\overline{\text{RESET}}$, CNVSS, BYTE	0		0.2VCC1	
		P0_0 to P0_7, P1_0 to P1_7 (in single-chip mode)	0		0.2VCC2	
		P0_0 to P0_7, P1_0 to P1_7 (in memory expansion mode and microprocessor mode)	0		0.16VCC2	

NOTES:
1. VIH and VIL reference for P8_7 apply when P8_7 is used as a programmable input port. It does not apply when P8_7 is used as XCIN.
2. P11 to P15 are provided in the 144-pin package only.

VCC1 = VCC2 = 5V

Timing Requirements
(VCC1 = VCC2 = 4.2 to 5.5 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.13 External Clock Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc	External clock input cycle time	31.25		ns
tw(H)	External clock input high (“H”) pulse width	13.75		ns
tw(L)	External clock input low (“L”) pulse width	13.75		ns
tr	External clock rise time		5	ns
tf	External clock fall time		5	ns

Table 5.14 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	100		ns
tw(TAH)	TAiIN input high (“H”) pulse width	40		ns
tw(TAL)	TAiIN input low (“L”) pulse width	40		ns

i = 0 to 4

Table 5.15 Timer A Input (Gate Signal Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	400		ns
tw(TAH)	TAiIN input high (“H”) pulse width	200		ns
tw(TAL)	TAiIN input low (“L”) pulse width	200		ns

i = 0 to 4

Table 5.16 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	200		ns
tw(TAH)	TAiIN input high (“H”) pulse width	100		ns
tw(TAL)	TAiIN input low (“L”) pulse width	100		ns

i = 0 to 4

Table 5.17 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tw(TAH)	TAiIN input high (“H”) pulse width	100		ns
tw(TAL)	TAiIN input low (“L”) pulse width	100		ns

i = 0 to 4

VCC1 = VCC2 = 5V

Timing Requirements
(VCC1 = VCC2 = 4.2 to 5.5 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.18 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(UP)	TAiOUT input cycle time	2000		ns
tw(UPH)	TAiOUT input high (“H”) pulse width	1000		ns
tw(UPL)	TAiOUT input low (“L”) pulse width	1000		ns
tsu(UP-TIN)	TAiOUT input setup time	400		ns
th(TIN-UP)	TAiOUT input hold time	400		ns

i = 0 to 4

Table 5.19 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	800		ns
tsu(TAIN-TAOUT)	TAiOUT input setup time	200		ns
tsu(TAOUT-TAIN)	TAiIN input setup time	200		ns

i = 0 to 4

Table 5.20 Timer B Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TB)	TBiIN input cycle time (counted on one edge)	100		ns
tw(TBH)	TBiIN input high (“H”) pulse width (counted on one edge)	40		ns
tw(TBL)	TBiIN input low (“L”) pulse width (counted on one edge)	40		ns
tc(TB)	TBiIN input cycle time (counted on both edges)	200		ns
tw(TBH)	TBiIN input high (“H”) pulse width (counted on both edges)	80		ns
tw(TBL)	TBiIN input low (“L”) pulse width (counted on both edges)	80		ns

i = 0 to 5

Table 5.21 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TB)	TBiIN input cycle time	400		ns
tw(TBH)	TBiIN input high (“H”) pulse width	200		ns
tw(TBL)	TBiIN input low (“L”) pulse width	200		ns

i = 0 to 5

Table 5.22 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TB)	TBiIN input cycle time	400		ns
tw(TBH)	TBiIN input high (“H”) pulse width	200		ns
tw(TBL)	TBiIN input low (“L”) pulse width	200		ns

i = 0 to 5

VCC1 = VCC2 = 5V

Timing Requirements
(VCC1 = VCC2 = 4.2 to 5.5 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.23 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(AD)	$\overline{\text{ADTRG}}$ input cycle time (required for trigger)	1000		ns
tw(ADL)	$\overline{\text{ADTRG}}$ input low (“L”) pulse width	125		ns

Table 5.24 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CK)	CLKi input cycle time	200		ns
tw(CKH)	CLKi input high (“H”) pulse width	100		ns
tw(CKL)	CLKi input low (“L”) pulse width	100		ns
td(C-Q)	TXDi output delay time		80	ns
th(C-Q)	TXDi output hold time	0		ns
tsu(D-C)	RXDi input setup time	70		ns
th(C-D)	RXDi input hold time	90		ns

i = 0 to 6

Table 5.25 Intelligent I/O Communication Function (Groups 0 and 1)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CK)	ISCLKi input cycle time	600		ns
tw(CKH)	ISCLKi input high (“H”) pulse width	300		ns
tw(CKL)	ISCLKi input low (“L”) pulse width	300		ns
td(C-Q)	ISTXDi output delay time		100	ns
th(C-Q)	ISTXDi output hold time	0		ns
tsu(D-C)	ISRXDi input setup time	100		ns
th(C-D)	ISRXDi input hold time	100		ns

i = 0, 1

Table 5.26 Intelligent I/O Communication Function (Group 2)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CK)	ISCLK2 input cycle time	600		ns
tw(CKH)	ISCLK2 input high (“H”) pulse width	300		ns
tw(CKL)	ISCLK2 input low (“L”) pulse width	300		ns
td(C-Q)	ISTXD2 output delay time		180	ns
th(C-Q)	ISTXD2 output hold time	0		ns
tsu(D-C)	ISRXD2 input setup time	150		ns
th(C-D)	ISRXD2 input hold time	100		ns

VCC1 = VCC2 = 5V

Timing Requirements
(VCC1 = VCC2 = 4.2 to 5.5 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.28 Memory Expansion mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tac1(RD-DB)	Data input access time (RD standard)		(note 1)	ns
tac1(AD-DB)	Data input access time (AD standard, CS standard)		(note 1)	ns
tac2(RD-DB)	Data input access time (RD standard, when accessing a space with the multiplexed bus)		(note 1)	ns
tac2(AD-DB)	Data input access time (AD standard, when accessing a space with the multiplexed bus)		(note 1)	ns
tsu(DB-BCLK)	Data input setup time	26		ns
tsu(RDY-BCLK)	$\overline{\text{RDY}}$ input setup time	26		ns
tsu(HOLD-BCLK)	$\overline{\text{HOLD}}$ input setup time	30		ns
th(RD-DB)	Data input hold time	0		ns
th(BCLK-RDY)	$\overline{\text{RDY}}$ input hold time	0		ns
th(BCLK-HOLD)	$\overline{\text{HOLD}}$ input hold time	0		ns
td(BCLK-HLDA)	$\overline{\text{HLDA}}$ output delay time		25	ns

NOTE:
1. Values, which depend on BCLK frequency and external bus cycles, can be obtained from the following equations. Insert wait states or lower the operation frequency, f(BCLK), if the calculated value is negative.

$$\text{tac1(RD-DB)} = \frac{10^9 \times m}{f(BCLK) \times 2} - 35\ [ns]$$ (if external bus cycle is $a\phi + b\phi$, $m = (b \times 2) + 1$)

$$\text{tac1(AD-DB)} = \frac{10^9 \times n}{f(BCLK)} - 35\ [ns]$$ (if external bus cycle is $a\phi + b\phi$, $n = a + b$)

$$\text{tac2(RD-DB)} = \frac{10^9 \times m}{f(BCLK) \times 2} - 35\ [ns]$$ (if external bus cycle is $a\phi + b\phi$, $m = (b \times 2) - 1$)

$$\text{tac2(AD-DB)} = \frac{10^9 \times p}{f(BCLK) \times 2} - 35\ [ns]$$ (if external bus cycle is $a\phi + b\phi$, $p = \{(a + b - 1) \times 2\} + 1$)

VCC1 = VCC2 = 3.3 V

Table 5.33 Electrical Characteristics (3/3)
(VCC1 = VCC2 = 3.3 V, VSS = 0 V, Topr = 25°C)

Symbol	Parameter	Measurement Condition(1)		Standard			Unit
				Min.	Typ.	Max.	
ICC	Power supply current	Flash memory version	f(CPU) = 24 MHz		23	33	mA
			f(CPU) = 16 MHz		17		mA
			f(CPU) = 8 MHz		11		mA
			f(CPU) = f(Ring) In on-chip oscillator low-power consumption mode		2.6		mA
			f(CPU) = 32 kHz In low-power consumption mode While flash memory is operating		430		µA
			f(CPU) = 32 kHz In low-power consumption mode While flash memory is stopped(2)		30		µA
			Wait mode: f(CPU) = f(Ring) After entering wait mode from on-chip oscillator low-power consumption mode		45		µA
			Stop mode (while clock is stopped)		0.8	5	µA
			Stop mode (while clock is stopped) Topr = 85°C			50	µA
		Mask ROM version	f(CPU) = 24 MHz		23	33	mA
			f(CPU) = 16 MHz		17		mA
			f(CPU) = 8 MHz		11		mA
			f(CPU) = f(Ring) In on-chip oscillator low-power consumption mode		1		mA
			f(CPU) = 32 kHz In low-power consumption mode		30		µA
			Wait mode: f(CPU) = f(Ring) After entering wait mode from on-chip oscillator low-power consumption mode		45		µA
			Stop mode (while clock is stopped)		0.8	5	µA
			Stop mode (while clock is stopped) Topr = 85°C			50	µA

NOTES:
1. In single-chip mode, leave the output pins open and connect the input pins to VSS.
2. Value is obtained when setting the FMSTP bit in the FMR0 register to 1 (flash memory stopped) and running the program on RAM.

VCC1 = VCC2 = 3.3 V

Timing Requirements
(VCC1 = VCC2 = 3.0 to 3.6 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.41 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(UP)	TAiOUT input cycle time	2000		ns
tw(UPH)	TAiOUT input high (“H”) pulse width	1000		ns
tw(UPL)	TAiOUT input low (“L”) pulse width	1000		ns
tsu(UP-TIN)	TAiOUT input setup time	400		ns
th(TIN-UP)	TAiOUT input hold time	400		ns

i = 0 to 4

Table 5.42 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	2		µs
tsu(TAIN-TAOUT)	TAiOUT input setup time	500		ns
tsu(TAOUT-TAIN)	TAiIN input setup time	500		ns

i = 0 to 4

Table 5.43 Timer B Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TB)	TBiIN input cycle time (counted on one edge)	100		ns
tw(TBH)	TBiIN input high (“H”) pulse width (counted on one edge)	40		ns
tw(TBL)	TBiIN input low (“L”) pulse width (counted on one edge)	40		ns
tc(TB)	TBiIN input cycle time (counted on both edges)	200		ns
tw(TBH)	TBiIN input high (“H”) pulse width (counted on both edges)	80		ns
tw(TBL)	TBiIN input low (“L”) pulse width (counted on both edges)	80		ns

i = 0 to 5

Table 5.44 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TB)	TBiIN input cycle time	400		ns
tw(TBH)	TBiIN input high (“H”) pulse width	200		ns
tw(TBL)	TBiIN input low (“L”) pulse width	200		ns

i = 0 to 5

Table 5.45 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TB)	TBiIN input cycle time	400		ns
tw(TBH)	TBiIN input high (“H”) pulse width	200		ns
tw(TBL)	TBiIN input low (“L”) pulse width	200		ns

i = 0 to 5

VCC1 = VCC2 = 3.3 V

Timing Requirements
(VCC1 = VCC2 = 3.0 to 3.6 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.46 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(AD)	$\overline{\text{ADTRG}}$ input cycle time (required for trigger)	1000		ns
tw(ADL)	$\overline{\text{ADTRG}}$ input low (“L”) pulse width	125		ns

Table 5.47 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CK)	CLKi input cycle time	200		ns
tw(CKH)	CLKi input high (“H”) pulse width	100		ns
tw(CKL)	CLKi input low (“L”) pulse width	100		ns
td(C-Q)	TXDi output delay time		80	ns
th(C-Q)	TXDi output hold time	0		ns
tsu(D-C)	RXDi input setup time	70		ns
th(C-D)	RXDi input hold time	90		ns

i = 0 to 6

Table 5.48 Intelligent I/O Communication Function (Groups 0 and 1)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CK)	ISCLKi input cycle time	600		ns
tw(CKH)	ISCLKi input high (“H”) pulse width	300		ns
tw(CKL)	ISCLKi input low (“L”) pulse width	300		ns
td(C-Q)	ISTXDi output delay time		100	ns
th(C-Q)	ISTXDi output hold time	0		ns
tsu(D-C)	ISRXDi input setup time	100		ns
th(C-D)	ISRXDi input hold time	100		ns

i = 0, 1

Table 5.49 Intelligent I/O Communication Function (Group 2)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CK)	ISCLK2 input cycle time	600		ns
tw(CKH)	ISCLK2 input high (“H”) pulse width	300		ns
tw(CKL)	ISCLK2 input low (“L”) pulse width	300		ns
td(C-Q)	ISTXD2 output delay time		180	ns
th(C-Q)	ISTXD2 output hold time	0		ns
tsu(D-C)	ISRXD2 input setup time	150		ns
th(C-D)	ISRXD2 input hold time	100		ns

VCC1 = VCC2 = 3.3 V

Switching Characteristics
(VCC1 = VCC2 = 3.0 to 3.6 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.52 Memory Expansion Mode and Microprocessor Mode (when accessing external memory space)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min.	Max.	
td(BCLK-AD)	Address output delay time	See Figure 5.2		18	ns
th(BCLK-AD)	Address output hold time (BCLK standard)		-3		ns
th(RD-AD)	Address output hold time (RD standard)(3)		0		ns
th(WR-AD)	Address output hold time (WR standard)(3)		(note 1)		ns
td(BCLK-CS)	Chip-select signal output delay time			18	ns
th(BCLK-CS)	Chip-select signal output hold time (BCLK standard)		-3		ns
th(RD-CS)	Chip-select signal output hold time (RD standard)(3)		0		ns
th(WR-CS)	Chip-select signal output hold time (WR standard)(3)		(note 1)		ns
td(BCLK-RD)	RD signal output delay time			18	ns
th(BCLK-RD)	RD signal output hold time		-5		ns
td(BCLK-WR)	WR signal output delay time			18	ns
th(BCLK-WR)	WR signal output hold time		0		ns
td(DB-WR)	Data output delay time (WR standard)		(note 2)		ns
th(WR-DB)	Data output hold time (WR standard)(3)		(note 1)		ns
tw(WR)	WR output width		(note 2)		ns

NOTES:

1. Values, which depend on BCLK frequency, can be obtained from the following equations.

$$th(WR\text{-}DB) = \frac{10^9}{f(BCLK) \times 2} - 20\ [ns]$$

$$th(WR\text{-}AD) = \frac{10^9}{f(BCLK) \times 2} - 15\ [ns]$$

$$th(WR\text{-}CS) = \frac{10^9}{f(BCLK) \times 2} - 10\ [ns]$$

2. Values, which depend on BCLK frequency and external bus cycles, can be obtained from the following equations.

$$td(DB\text{-}WR) = \frac{10^9 \times m}{f(BCLK)} - 20\ [ns]\ (\text{if external bus cycle is } a\phi + b\phi,\ m = b)$$

$$tw(WR) = \frac{10^9 \times n}{f(BCLK) \times 2} - 15\ [ns]\ (\text{if external bus cycle is } a\phi + b\phi,\ n = (b \times 2) - 1)$$

3. tc [ns] is added when recovery cycle is inserted.

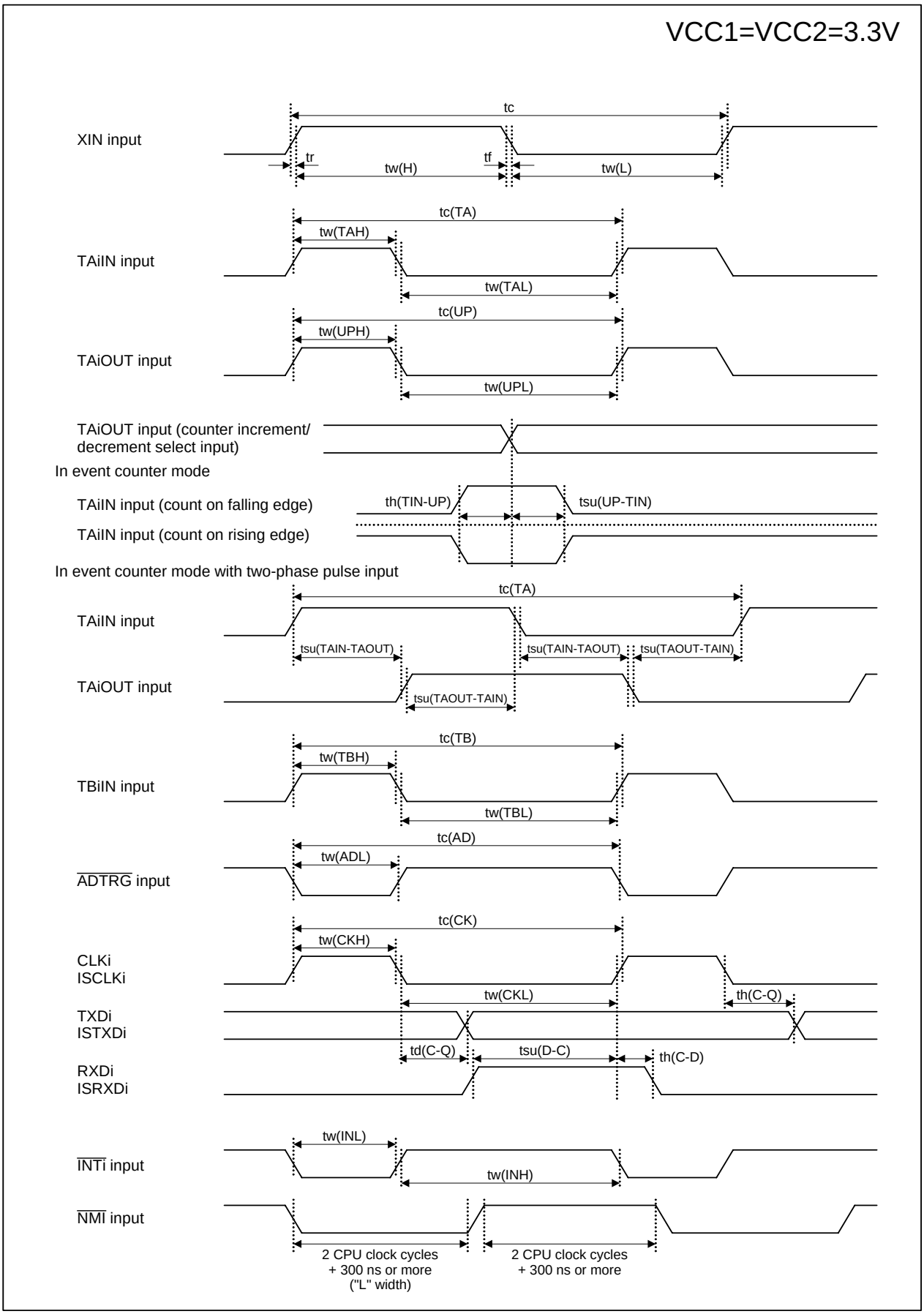

Figure 5.7 VCC1 = VCC2 = 3.3 V Timing Diagram (1/4)

REVISION HISTORY	M32C/87 Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.50	Dec.16, 04	–	New Document
1.00	Jul.14, 05	–	**M32C/87A and M32C/87B** added
		–	Package code changed: 144P6Q-A to PLQP0144KA-A, 100P6Q-A to PLQP0100KB-A, 100P6S-A to PRQP0100JB-A
		–	"Low Voltage Detection Reset" changed to "Brown-out Detection Reset"
			Overview
		2	• **Table 1.2 M32C/87 Group Performance (144-Pin Package)** M32C/87A and M32C/87B performance added to the CAN module performance; Power Consumption performance released
		3	• **Table 1.2 M32C/87 Group Performance (100-Pin Package)** M32C/87A and M32C/87B performance added to the CAN module performance; Power Consumption performance released
		4	• **Figure 1.1 M32C/87 Group Block Diagram** Note 4 deleted; note 5 added
		7	• **Figure 1.3 Pin Assignment for 144-Pin Package** Note 15 added
		8	• **Table 1.4 Pin Characteristics for 144-Pin Package** Note 1 added
		11	• **Figure 1.4 Pin Assignment for 100-Pin Package** Note 19 added
		12	• **Figure 1.5 Pin Assignment for 100-Pin Package** Note 15 added
		13	• **Table 1.5 Pin Characteristics for 100-Pin Package** Note 1 added
		17	• **Table 1.6 Pin Description** Note 2 added
			Memory
		22	• **Figure 3.1 Memory Map** Note 3 changed
			Special Function Register (SFR)
		26	• The RLVL register Value after reset modified
		26	• The IIO0IR to IIO11IR registers Value after reset modified
		27 to 30	• Name of the registers assosiated to Intelligent I/O changed
		27	• The G0RB register Value after reset modified
		27	• The G1BCR0 and G1BCR1 registers Value after reset modified
		29	• The G0CR register Value after reset modified
		32 to 37	• Note added to the CAN-associated registers
		40	• The TCSPR register Value after reset modified; note 1 added
		41	• The AD00 register Value after reset modified
		42	• The PSC register Value after reset modified
		42	• The PS2 register Value after reset modified
		43	• The PCR register Value after reset modified
		44	• The PSD1 register Value after reset modified
		45	• The PCR register Value after reset modified
			Electrical Characteristics
		48	• **Table 5.2 Electrical Characteristics** Parameter f(BCLK) and its values added; min. and max. values for f(RING) added
		49	• **Table 5.3 Electrical Characteristics** V_{OH} values modified**;** R_{PULLUP} value modified
		50	• **Table 5.3 Electrical Characteristics (Continued)** Measurement Condition and standard values for ICC added and some released
		52	• **Table 5.6 Flash Memory Version Electrical Characteristics** Word Program Time and Lock bit Program Time values modified; parameter All-Unlocked-Block-Erase Time deleted; note 1 deleted
		54	• **Table 5.10 Memory Expansion Mode and Microprocessor Mode** *tac1(RD-DB)* expression on note 1 modified; *tac2(RD-DB)* expression on note 1 added

REVISION HISTORY	M32C/87 Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.50	Oct 20, 2007	All	**All in this manual** • Descriptions and formats unified • Notation of numbers changed (e.g. 00_2 → 00b, FF_{16} → FFh) • Notation of pin name changed (e.g. RTP00 → RTP_0, A15(/D15) → [A15/D15]) • [Term changed] Serial I/O → Serial interface Clock synchronous serial I/O mode → Clock synchronous mode Clock asynchronous serial I/O mode → Clock asynchronous mode Clock synchronous variable length → Variable data length clock synchronous Voltage detection circuit → Power supply voltage detection function Low voltage detection interrupt → Vdet4 detection interrupt Brown-out detection reset → Vdet3 detection function
			Overview
		1	• Header **SINGLE-CHIP 16/32-BIT CMOS MICROCOMPUTER → RENESAS MCU**
			• **1.1 Features** title added; **1.1 Applications** changed to **1.1.1 Applications**
		2	• **1.2 Performance Overview** changed to **1.1.2 Specifications**
		2-5	• **Tables 1.1** to **1.4** Structure, descriptions in Specification field, NOTE, and value partially revised or deleted
			• **Real-Time Port** Item deleted; **ROM Correction Function** Item added
		8	• **1.3 Block Diagram** moved following the **1.2 Product List**
		6-7	• **1.2 Product List** Tables revised; NOTE 1 added
		9, 14, 15	• **Figures 1.3** to **1.5** Arrows for VSS and VCC deleted; NOTES partially modified
		11,17	• **Tables 1.9** and **1.13** CLKOUT pin moved from Bus Control Pin column to Control Pin column
		19-22	• **Tables 1.15** to **1.19** Descriptions revised; NOTE 1 added
			Memory
		26	• Text partially modified
			SFR
		34-39	• **Tables 4.8** to **4.13** NOTE “Set the PM13 bit in the PM1 register to 1 (2 wait states for SFR area) before accessing the CAN-associated registers.” added
		45	• **Table 4.19** The PSL5 register added to the Address field of 03BBh item; the PSL7 register added to the Address field of 03BFh item
			• [Register names changed]
		27	002Fh Low Voltage Detection Interrupt Register → Vdet4 Detection Interrupt Register
		34	01C1h UART5 Bit Rate Register → UART5 Baud Rate Register 01C9h UART6 Bit Rate Register → UART6 Baud Rate Register 01D0h UART5, UART6 Transmit/Receive Control Register 2 → UART5, UART6 Transmit/Receive Control Register 01DBh to 01D8h Pulse Output Data Register → RTP Output Buffer Register
		41	0303h to 0302h Timer A1-1 Register → Timer A11 Register 0305h to 0304h Timer A2-1 Register → Timer A21 Register 0307h to 0306h Timer A4-1 Register → Timer A41 Register
		42	0340h Count Start Flag → Count Start Register 0341h Clock Prescaler Reset Flag → Clock Prescaler Reset Register

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Colophon .7.2