Renesas Electronics America Inc - M30875FHAGP#U5 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M32C/80
Core Size	16/32-Bit
Speed	32MHz
Connectivity	CANbus, EBI/EMI, I²C, IEBus, IrDA, SIO, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	121
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 34x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30875fhagp-u5

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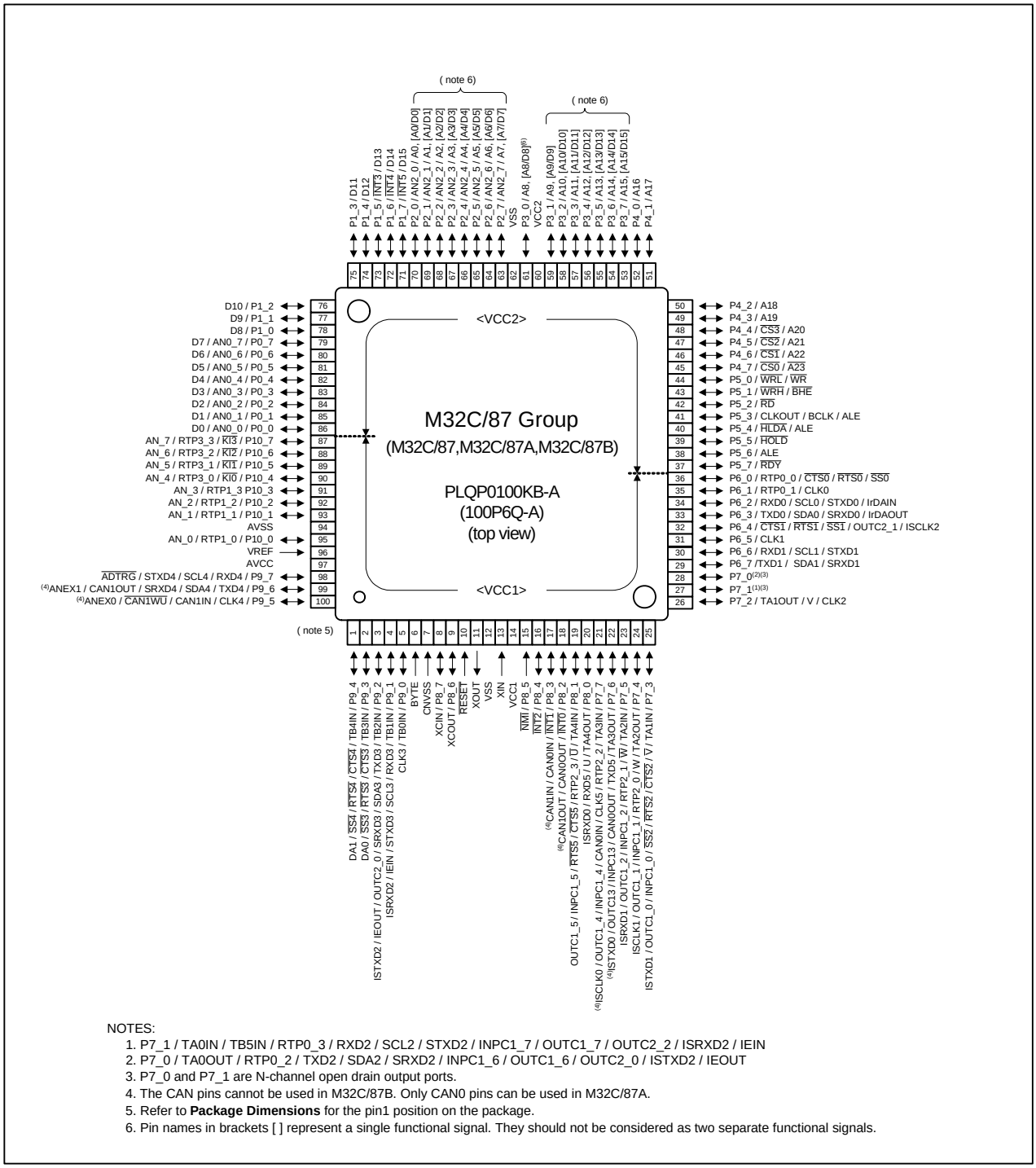
Table 1.4 Specifications (100-Pin Package) (2/2)

Item	Function	Specification
Serial Interface	UART0 to UART4	Clock synchronous/asynchronous × 5 I^2C bus, special mode 2, GCI mode, SIM mode, IrDA mode(2), IEBus (optional)(1)(3)
	UART5	Clock synchronous/asynchronous × 1
A/D Converter		10-bit resolution × 26 channels (in single-chip mode) 10-bit resolution × 10 channels (in memory expansion mode and microprocessor mode) Including sample and hold function
D/A Converter		8-bit resolution × 2 channels
CRC Calculation Circuit		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) compliant
X/Y Converter		16 bits x 16 bits
Intelligent I/O		16-bit timer × 2 • Time measurement function (input capture): 8 channels • Waveform generation function (output compare): 10 channels • Communication function: Clock synchronous mode, clock asynchronous mode, HDLC data processing mode, IEBus (optional)(1)(3) • 2-phase pulse signal processing (2-phase encoder input) × 1
ROM Correction Function		Address match interrupt × 8
CAN modules		Supporting CAN 2.0B specification M32C/87: 16 slots × 2 channels, M32C/87A: 16 slots × 1 channel M32C/87B: none
I/O Ports	Programmable I/O ports	• Input only: 1 • CMOS I/O: 85, selectable pull-up resistor • N channel open drain ports: 2
Flash Memory		• Erase and program voltage: 3.3 V ± 0.3 V or 5.0 V ± 0.5 V • Erase and program endurance: 100 times (all areas) • Program security: ROM code protect and ID code check • Debug functions: On-chip debug and on-board flash reprogram
Operating Frequency/Supply Voltage		32 MHz: VCC1 = 4.2 to 5.5 V, VCC2 = 3.0 V to VCC1 24 MHz: VCC1 = 3.0 to 5.5 V, VCC2 = 3.0 V to VCC1
Current Consumption		32 mA (32 MHz, VCC1 = VCC2 = 5 V) 23 mA (24 MHz, VCC1 = VCC2 = 3.3 V) 45 μA (approx. 1 MHz, VCC1 = VCC2 = 3.3 V, on-chip oscillator low-power consumption mode → wait mode) 0.8 μA (VCC1 = VCC2 = 3.3 V, stop mode)
Operating Ambient Temperature (°C)		-20 to 85°C, -40 to 85°C (optional)(3)
Package		100-pin LQFP (PLQP0100KB-A) 100-pin QFP (PRQP0100JB-A)

NOTES:
1. IEBus is a registered trademark of NEC Electronics Corporation.
2. Available in UART0.
3. Please contact a Renesas sales office for optional features.



NOTES:
1. P7_1 / TA0IN / TB5IN / RTP0_3 / RXD2 / SCL2 / STXD2 / INPC1_7 / OUTC1_7 / OUTC2_2 / ISRXD2 / IEIN
2. P7_0 / TA0OUT / RTP0_2 / TXD2 / SDA2 / SRXD2 / INPC1_6 / OUTC1_6 / OUTC2_0 / ISTXD2 / IEOUT
3. P7_0 and P7_1 are N-channel open drain output ports.
4. The CAN pins cannot be used in M32C/87B. Only CAN0 pins can be used in M32C/87A.
5. Refer to **Package Dimensions** for the pin1 position on the package.
6. Pin names in brackets [ ] represent a single functional signal. They should not be considered as two separate functional signals.

Figure 1.5 Pin Assignment for 100-Pin Package

Table 1.12 100-Pin Package List of Pin Names (1/3)

Pin No.		Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin(1)	Intelligent I/O Pin	Analog Pin	Bus Control Pin
FP	GP								
1	99		P9_6			TXD4/SDA4/SRXD4/ CAN1OUT		ANEX1	
2	100		P9_5			CLK4/CAN1IN/ CAN1WU		ANEX0	
3	1		P9_4		TB4IN	CTS4/RTS4/SS4		DA1	
4	2		P9_3		TB3IN	CTS3/RTS3/SS3		DA0	
5	3		P9_2		TB2IN	TXD3/SDA3/SRXD3	OUTC2_0/IEOUT/ISTXD2		
6	4		P9_1		TB1IN	RXD3/SCL3/STXD3	IEIN/ISRXD2		
7	5		P9_0		TB0IN	CLK3			
8	6	BYTE							
9	7	CNVSS							
10	8	XCIN	P8_7						
11	9	XCOUT	P8_6						
12	10	RESET							
13	11	XOUT							
14	12	VSS							
15	13	XIN							
16	14	VCC1							
17	15		P8_5	NMI					
18	16		P8_4	INT2					
19	17		P8_3	INT1		CAN0IN/CAN1IN			
20	18		P8_2	INT0		CAN0OUT/CAN1OUT			
21	19		P8_1		TA4IN/U/RTP2_3	CTS5/RTS5	INPC1_5/OUTC1_5		
22	20		P8_0		TA4OUT/U	RXD5	ISRXD0		
23	21		P7_7		TA3IN/RTP2_2	CLK5/CAN0IN	INPC1_4/OUTC1_4/ ISCLK0		
24	22		P7_6		TA3OUT	TXD5/CAN0OUT	INPC1_3/OUTC1_3/ ISTXD0		
25	23		P7_5		TA2IN/W/RTP2_1		INPC1_2/OUTC1_2 ISRXD1		
26	24		P7_4		TA2OUT/W/ RTP2_0		INPC1_1/OUTC1_1/ ISCLK1		
27	25		P7_3		TA1IN/V	CTS2/RTS2/SS2	INPC1_0/OUTC1_0/ ISTXD1		
28	26		P7_2		TA1OUT/V	CLK2			
29	27		P7_1		TA0IN/TB5IN/ RTP0_3	RXD2/SCL2/STXD2	INPC1_7/OUTC1_7/ OUTC2_2/ISRXD2/IEIN		
30	28		P7_0		TA0OUT/RTP0_2	TXD2/SDA2/SRXD2	INPC1_6/OUTC1_6/ OUTC2_0/ISTXD2/IEOUT		
31	29		P6_7			TXD1/SDA1/SRXD1			
32	30		P6_6			RXD1/SCL1/STXD1			
33	31		P6_5			CLK1			
34	32		P6_4			CTS1/RTS1/SS1	OUTC2_1/ISCLK2		
35	33		P6_3			TXD0/SDA0/SRXD0/ IrDAOUT			
36	34		P6_2			RXD0/SCL0/STXD0/ IrDAIN			
37	35		P6_1		RTP0_1	CLK0			
38	36		P6_0		RTP0_0	CTS0/RTS0/SS0			
39	37		P5_7						RDY
40	38		P5_6						ALE

NOTE:
1. The CAN pins cannot be used in M32C/87B. Only CAN0 pins can be used in M32C/87A.

Table 1.16 Pin Functions (100-Pin and 144-Pin Packages) (2/4)

Type	Symbol	I/O Type	Supply Voltage	Description
Main clock input	XIN	I	VCC1	Input/output pins for the main clock oscillation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT. To apply an external clock, apply it to XIN and leave XOUT open.
Main clock output	XOUT	O	VCC1	
Sub clock input	XCIN	I	VCC1	Input/output pins for the sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOUT. To apply an external clock, apply it to XCIN and leave XCOUT open.
Sub clock output	XCOUT	O	VCC1	
BCLK output	BCLK	O	VCC2	Bus clock output pin.
Clock output	CLKOUT	O	VCC2	The CLKOUT pin outputs the clock having the same frequency as fC, f8, or f32.
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT2}}$	I	VCC1	$\overline{\text{INT}}$ interrupt input pins.
	$\overline{\text{INT3}}$ to $\overline{\text{INT5}}$	I	VCC2	
$\overline{\text{NMI}}$ interrupt input	$\overline{\text{NMI}}$	I	VCC1	$\overline{\text{NMI}}$ interrupt input pin. Connect the $\overline{\text{NMI}}$ pin to VCC1 via a resistor when the $\overline{\text{NMI}}$ interrupt is not used.
Timer A	TA0OUT to TA4OUT	I/O	VCC1	Timer A0 to A4 input/output pins. (TA0OUT is N-channel open drain output.)
	TA0IN to TA4IN	I	VCC1	Timer A0 to A4 input pins.
Timer B	TB0IN to TB5IN	I	VCC1	Timer B0 to B5 input pins.
Three-phase motor control timer output	U, $\overline{\text{U}}$, V, $\overline{\text{V}}$, W, $\overline{\text{W}}$	O	VCC1	Three-phase motor control timer output pins.
Serial interface	$\overline{\text{CTS0}}$ to $\overline{\text{CTS5}}$	I	VCC1	Input pins to control data transmission.
	$\overline{\text{RTS0}}$ to $\overline{\text{RTS5}}$	O	VCC1	Output pins to control data reception.
	CLK0 to CLK5	I/O	VCC1	Serial clock input/output pins.
	RXD0 to RXD5	I	VCC1	Serial data input pins.
	TXD0 to TXD5	O	VCC1	Serial data output pins. (TXD2 is N-channel open drain output.)
I^2C mode	SDA0 to SDA4	I/O	VCC1	Serial data input/output pins. (SDA2 is N-channel open drain output.)
	SCL0 to SCL4	I/O	VCC1	Serial clock input/output pins. (SCL2 is N-channel open drain output.)
Serial interface special function	STXD0 to STXD4	O	VCC1	Serial data output pins when slave mode is selected. (STXD2 is N-channel open drain output.)
	SRXD0 to SRXD4	I	VCC1	Serial data input pins when slave mode is selected.
	$\overline{\text{SS0}}$ to $\overline{\text{SS4}}$	I	VCC1	Control input pins used in the serial interface special mode.
IrDA	IrDAIN	I	VCC1	IrDA serial data input pin.
	IrDAOUT	O	VCC1	IrDA serial data output pin.
CAN(1)	CAN0IN, CAN1IN	I	VCC1	Received data input pins for the CAN communication function.
	CAN0OUT, CAN1OUT	O	VCC1	Transmit data output pins for the CAN communication function.
	$\overline{\text{CAN1WU}}$	I	VCC1	CAN wake-up interrupt input pin.

I: Input O: Output I/O: Input and output

NOTE:

1. The CAN pins cannot be used in M32C/87B. Only CAN0 pins can be used in M32C/87A.

Table 1.18 Pin Functions (100-Pin and 144-Pin Package) (4/4)

Type	Symbol	I/O Type	Supply Voltage	Description
I/O port	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7	I/O	VCC2	8-bit CMOS I/O ports. The Port Pi Direction Register (i = 0 to 15) determines if each pin is used as an input port or an output port. The Pull-Up Control Registers determine if the input ports, divided into groups of four, are pulled up or not.
	P6_0 to P6_7, P7_0 to P7_7, P9_0 to P9_7, P10_0 to P10_7	I/O	VCC1	These 8-bit I/O ports are functionally equivalent to P0. (P7_0 and P7_1 are N-channel open drain output.)
	P8_0 to P8_4 P8_6, P8_7	I/O	VCC1	These I/O ports are functionally equivalent to P0.
Input port	P8_5	I	VCC1	Shares the pin with $\overline{\text{NMI}}$. Input port to read $\overline{\text{NMI}}$ pin level.
Key input interrupt input	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	VCC1	Key input interrupt input pins.

I: Input O: Output I/O: Input and output

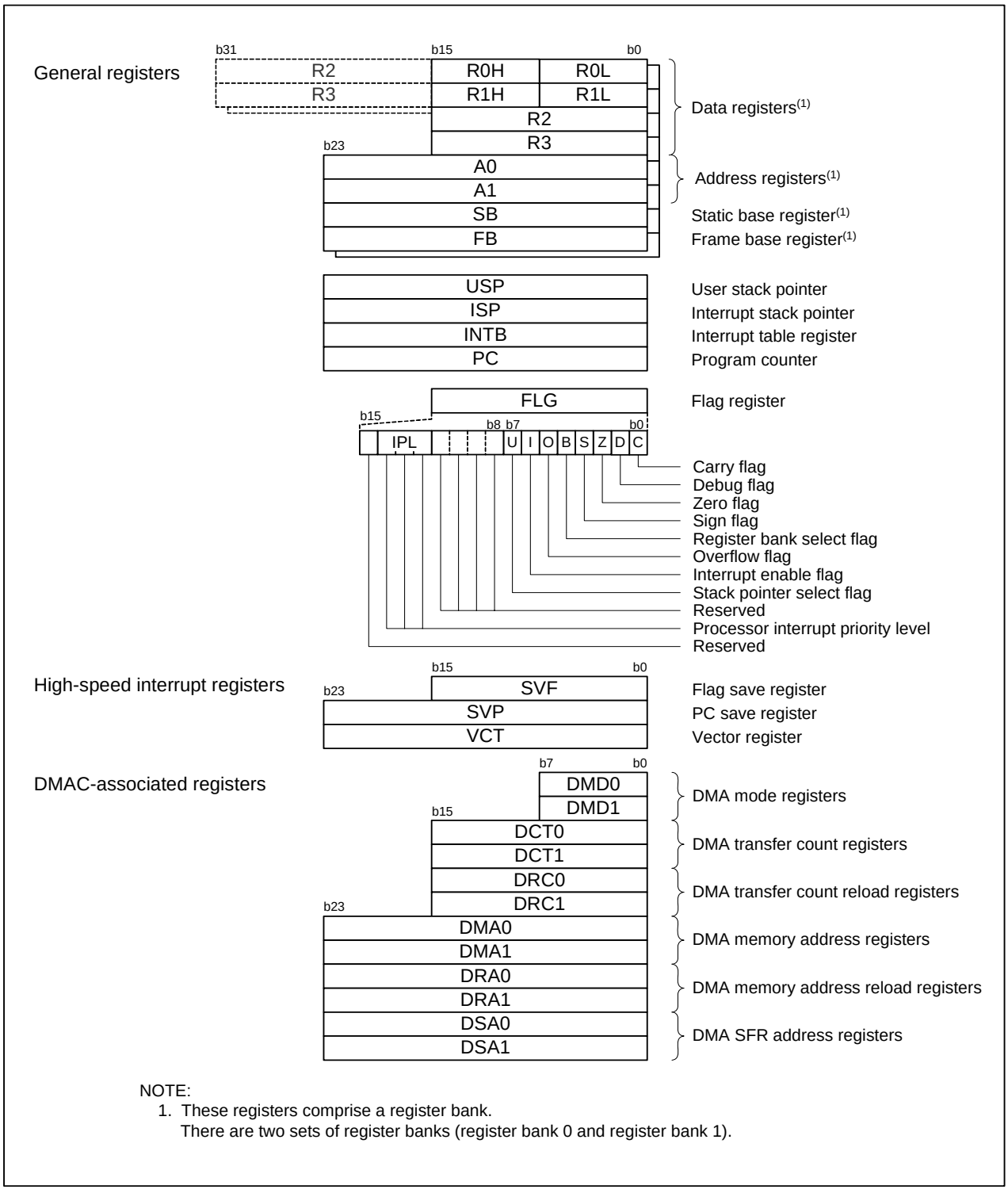
Table 1.19 Pin Functions (144-Pin Package Only)

Type	Symbol	I/O Type	Supply Voltage	Description
$\overline{\text{INT}}$ Interrupt Input	$\overline{\text{INT6}}$ to $\overline{\text{INT8}}$	I	VCC1	$\overline{\text{INT}}$ interrupt input pins.
Serial interface	$\overline{\text{CTS6}}$	I	VCC1/ VCC2	Input pin to control data transmission.
	$\overline{\text{RTS6}}$	O	VCC1/ VCC2	Output pin to control data reception.
	CLK6	I/O	VCC1/ VCC2	Serial clock input/output pin.
	RXD6	I	VCC1/ VCC2	Serial data input pin.
	TXD6	O	VCC1/ VCC2	Serial data output pin.
Intelligent I/O	OUTC2_3 to OUTC2_7	O	VCC2	Output pins for the waveform generation function.
A/D converter	AN15_0 to AN15_7	I	VCC1	Analog input pins for the A/D converter.
I/O port	P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7	I/O	VCC2	These I/O ports are functionally equivalent to P0.
	P14_0 to P14_6, P15_0 to P15_7	I/O	VCC1	These I/O ports are functionally equivalent to P0.

I: Input O: Output I/O: Input and output

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers.
The register bank is comprised of eight registers (R0, R1, R2, R3, A0, A1, SB, and FB) out of 28 CPU registers. There are two sets of register banks.



NOTE:
1. These registers comprise a register bank.
There are two sets of register banks (register bank 0 and register bank 1).

Figure 2.1 CPU Register

4. Special Function Registers (SFRs)

Special Function Registers (SFRs) are the control registers of peripheral functions. Tables 4.1 to 4.20 list SFR address maps.

Table 4.1 SFR Address Map (1/20)

Address	Register	Symbol	After Reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0(1)	PM0	1000 0000b(CNVSS="L") 0000 0011b(CNVSS="H")
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	0000 1000b
0007h	System Clock Control Register 1	CM1	0010 0000b
0008h			
0009h	Address Match Interrupt Enable Register	AIER	00h
000Ah	Protect Register	PRCR	XXXX 0000b
000Bh	External Data Bus Width Control Register	DS	XXXX 1000b(BYTE="L") XXXX 0000b(BYTE="H")
000Ch	Main Clock Division Register	MCD	XXX0 1000b
000Dh	Oscillation Stop Detection Register	CM2	00h
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDC	00XX XXXXb
0010h	Address Match Interrupt Register 0	RMAD0	000000h
0011h			
0012h			
0013h	Processor Mode Register 2	PM2	00h
0014h	Address Match Interrupt Register 1	RMAD1	000000h
0015h			
0016h			
0017h	Voltage Detection Register 2	VCR2	00h
0018h	Address Match Interrupt Register 2	RMAD2	000000h
0019h			
001Ah			
001Bh	Voltage Detection Register 1	VCR1	0000 1000b
001Ch	Address Match Interrupt Register 3	RMAD3	000000h
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h			
0024h			
0025h			
0026h	PLL Control Register 0	PLC0	0001 X010b
0027h	PLL Control Register 1	PLC1	000X 0000b
0028h	Address Match Interrupt Register 4	RMAD4	000000h
0029h			
002Ah			
002Bh			
002Ch	Address Match Interrupt Register 5	RMAD5	000000h
002Dh			
002Eh			
002Fh	Vdet4 Detection Interrupt Register	D4INT	XX00 0000b

X: Undefined
Blank spaces are all reserved. No access is allowed.
NOTE:
1. Bits PM01 and PM00 in the PM0 register maintain values set before reset, even after software reset or watchdog timer reset has been performed.

Table 4.4 SFR Address Map (4/20)

Address	Register	Symbol	After Reset
0090h	UART0 Transmit/NACK Interrupt Control Register	S0TIC	XXXX X000b
0091h	UART1/UART4 Bus Conflict Detection Interrupt Control Register	BCN1IC/BCN4IC	XXXX X000b
0092h	UART1 Transmit/NACK Interrupt Control Register	S1TIC	XXXX X000b
0093h	Key Input Interrupt Control Register	KUPIC	XXXX X000b
0094h	Timer B0 Interrupt Control Register	TB0IC	XXXX X000b
0095h	II/O Interrupt Control Register 1 / CAN1 Interrupt Control Register 1	IIO1IC/CAN4IC	XXXX X000b
0096h	Timer B2 Interrupt Control Register	TB2IC	XXXX X000b
0097h	II/O Interrupt Control Register 3	IIO3IC	XXXX X000b
0098h	Timer B4 Interrupt Control Register	TB4IC	XXXX X000b
0099h	II/O Interrupt Control Register 5 /CAN1 Interrupt Control Register 2	IIO5IC/CAN5IC	XXXX X000b
009Ah	$\overline{\text{INT4}}$ Interrupt Control Register	INT4IC	XX00 X000b
009Bh	II/O Interrupt Control Register 7	IIO7IC	XXXX X000b
009Ch	$\overline{\text{INT2}}$ Interrupt Control Register	INT2IC	XX00 X000b
009Dh	II/O Interrupt Control Register 9 / CAN0 Interrupt Control Register 0	IIO9IC/CAN0IC	XXXX X000b
009Eh	$\overline{\text{INT0}}$ Interrupt Control Register	INT0IC	XX00 X000b
009Fh	Exit Priority Register	RLVL	XXXX 0000b
00A0h	Interrupt Request Register 0	IIO0IR	0000 000Xb
00A1h	Interrupt Request Register 1	IIO1IR	0000 000Xb
00A2h	Interrupt Request Register 2	IIO2IR	0000 000Xb
00A3h	Interrupt Request Register 3	IIO3IR	0000 000Xb
00A4h	Interrupt Request Register 4	IIO4IR	0000 000Xb
00A5h	Interrupt Request Register 5	IIO5IR	0000 000Xb
00A6h	Interrupt Request Register 6	IIO6IR	0000 000Xb
00A7h	Interrupt Request Register 7	IIO7IR	0000 000Xb
00A8h	Interrupt Request Register 8	IIO8IR	0000 000Xb
00A9h	Interrupt Request Register 9	IIO9IR	0000 000Xb
00AAh	Interrupt Request Register 10	IIO10IR	0000 000Xb
00ABh	Interrupt Request Register 11	IIO11IR	0000 000Xb
00ACh			
00ADh			
00AEh			
00AFh			
00B0h	Interrupt Enable Register 0	IIO0IE	00h
00B1h	Interrupt Enable Register 1	IIO1IE	00h
00B2h	Interrupt Enable Register 2	IIO2IE	00h
00B3h	Interrupt Enable Register 3	IIO3IE	00h
00B4h	Interrupt Enable Register 4	IIO4IE	00h
00B5h	Interrupt Enable Register 5	IIO5IE	00h
00B6h	Interrupt Enable Register 6	IIO6IE	00h
00B7h	Interrupt Enable Register 7	IIO7IE	00h
00B8h	Interrupt Enable Register 8	IIO8IE	00h
00B9h	Interrupt Enable Register 9	IIO9IE	00h
00BAh	Interrupt Enable Register 10	IIO10IE	00h
00BBh	Interrupt Enable Register 11	IIO11IE	00h
00BCh			
00BDh			
00BEh			
00BFh to 00DFh			

X: Undefined
Blank spaces are all reserved. No access is allowed.

VCC1 = VCC2 = 5V

Table 5.11 Voltage Detection Circuit Electrical Characteristics (VCC1 = VCC2 = 3.0 to 5.5 V, VSS = 0 V, Topr = 25°C unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet4	Vdet4 detection voltage	VCC1 = 3.0 V to 5.5 V	3.3	3.8	4.4	V
Vdet3	Vdet3 detection voltage			3.0		V
Vdet3s	Hardware reset 2 hold voltage				2.0	V
Vdet3r	Hardware reset 2 release voltage			3.1		V

NOTES:
1. Vdet4 > Vdet3
2. Vdet3r > Vdet3 is not guaranteed.

Table 5.12 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
td(P-R)	Wait time to stabilize internal supply voltage when power-on	VCC1 = 3.0 to 5.5 V			2	ms
td(S-R)	Wait time to release hardware reset 2	VCC1 = Vdet3r to 5.5 V		6(1)	20	ms
td(E-A)	Start-up time for Vdet3 and Vdet4 detection circuit	VCC1 = 3.0 to 5.5 V			20	µs

NOTE:
1. When VCC1 = 5 V

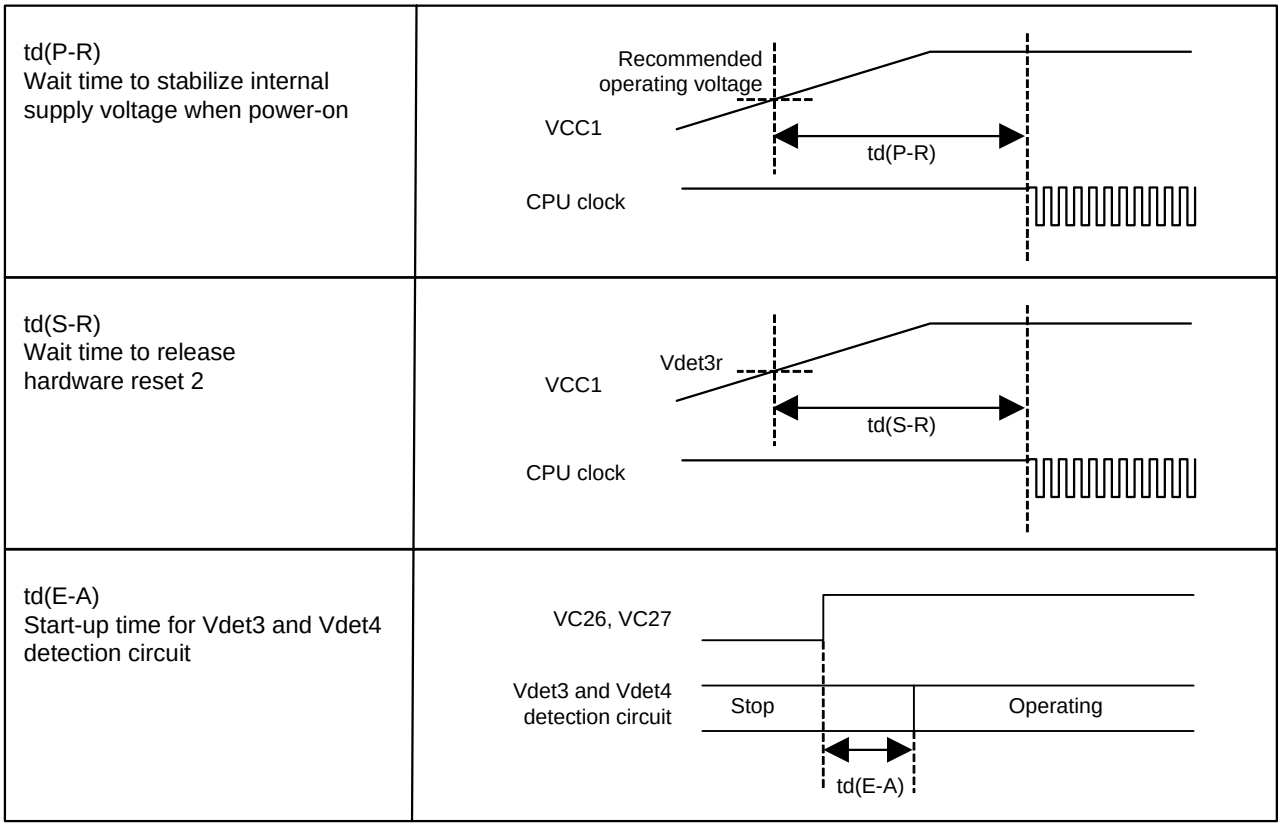


Figure 5.1 Power Supply Timing Diagram

VCC1 = VCC2 = 5V

Timing Requirements
(VCC1 = VCC2 = 4.2 to 5.5 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.13 External Clock Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc	External clock input cycle time	31.25		ns
tw(H)	External clock input high (“H”) pulse width	13.75		ns
tw(L)	External clock input low (“L”) pulse width	13.75		ns
tr	External clock rise time		5	ns
tf	External clock fall time		5	ns

Table 5.14 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	100		ns
tw(TAH)	TAiIN input high (“H”) pulse width	40		ns
tw(TAL)	TAiIN input low (“L”) pulse width	40		ns

i = 0 to 4

Table 5.15 Timer A Input (Gate Signal Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	400		ns
tw(TAH)	TAiIN input high (“H”) pulse width	200		ns
tw(TAL)	TAiIN input low (“L”) pulse width	200		ns

i = 0 to 4

Table 5.16 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	200		ns
tw(TAH)	TAiIN input high (“H”) pulse width	100		ns
tw(TAL)	TAiIN input low (“L”) pulse width	100		ns

i = 0 to 4

Table 5.17 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tw(TAH)	TAiIN input high (“H”) pulse width	100		ns
tw(TAL)	TAiIN input low (“L”) pulse width	100		ns

i = 0 to 4

VCC1 = VCC2 = 5V

Timing Requirements
(VCC1 = VCC2 = 4.2 to 5.5 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.28 Memory Expansion mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tac1(RD-DB)	Data input access time (RD standard)		(note 1)	ns
tac1(AD-DB)	Data input access time (AD standard, CS standard)		(note 1)	ns
tac2(RD-DB)	Data input access time (RD standard, when accessing a space with the multiplexed bus)		(note 1)	ns
tac2(AD-DB)	Data input access time (AD standard, when accessing a space with the multiplexed bus)		(note 1)	ns
tsu(DB-BCLK)	Data input setup time	26		ns
tsu(RDY-BCLK)	$\overline{\text{RDY}}$ input setup time	26		ns
tsu(HOLD-BCLK)	$\overline{\text{HOLD}}$ input setup time	30		ns
th(RD-DB)	Data input hold time	0		ns
th(BCLK-RDY)	$\overline{\text{RDY}}$ input hold time	0		ns
th(BCLK-HOLD)	$\overline{\text{HOLD}}$ input hold time	0		ns
td(BCLK-HLDA)	$\overline{\text{HLDA}}$ output delay time		25	ns

NOTE:
1. Values, which depend on BCLK frequency and external bus cycles, can be obtained from the following equations. Insert wait states or lower the operation frequency, f(BCLK), if the calculated value is negative.

$$\text{tac1(RD-DB)} = \frac{10^9 \times m}{f(BCLK) \times 2} - 35\ [ns]$$ (if external bus cycle is $a\phi + b\phi$, $m = (b \times 2) + 1$)

$$\text{tac1(AD-DB)} = \frac{10^9 \times n}{f(BCLK)} - 35\ [ns]$$ (if external bus cycle is $a\phi + b\phi$, $n = a + b$)

$$\text{tac2(RD-DB)} = \frac{10^9 \times m}{f(BCLK) \times 2} - 35\ [ns]$$ (if external bus cycle is $a\phi + b\phi$, $m = (b \times 2) - 1$)

$$\text{tac2(AD-DB)} = \frac{10^9 \times p}{f(BCLK) \times 2} - 35\ [ns]$$ (if external bus cycle is $a\phi + b\phi$, $p = \{(a + b - 1) \times 2\} + 1$)

VCC1 = VCC2 = 5V

Switching Characteristics
(VCC1 = VCC2 = 4.2 to 5.5 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.29 Memory Expansion Mode and Microprocessor Mode (when accessing external memory space)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min.	Max.	
td(BCLK-AD)	Address output delay time	See Figure 5.2		18	ns
th(BCLK-AD)	Address output hold time (BCLK standard)		-3		ns
th(RD-AD)	Address output hold time (RD standard)(3)		0		ns
th(WR-AD)	Address output hold time (WR standard)(3)		(note 1)		ns
td(BCLK-CS)	Chip-select signal output delay time			18	ns
th(BCLK-CS)	Chip-select signal output hold time (BCLK standard)		-3		ns
th(RD-CS)	Chip-select signal output hold time (RD standard)(3)		0		ns
th(WR-CS)	Chip-select signal output hold time (WR standard)(3)		(note 1)		ns
td(BCLK-RD)	RD signal output delay time			18	ns
th(BCLK-RD)	RD signal output hold time		-5		ns
td(BCLK-WR)	WR signal output delay time			18	ns
th(BCLK-WR)	WR signal output hold time		-5		ns
td(DB-WR)	Data output delay time (WR standard)		(note 2)		ns
th(WR-DB)	Data output hold time (WR standard)(3)		(note 1)		ns
tw(WR)	WR output width		(note 2)		ns

NOTES:

1. Values, which depend on BCLK frequency, can be obtained from the following equations.

$$th(WR\text{-}DB) = \frac{10^9}{f(BCLK) \times 2} - 15 \text{ [ns]}$$

$$th(WR\text{-}AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \text{ [ns]}$$

$$th(WR\text{-}CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \text{ [ns]}$$

2. Values, which depend on BCLK frequency and external bus cycles, can be obtained from the following equations.

$$td(DB\text{-}WR) = \frac{10^9 \times m}{f(BCLK)} - 20 \text{ [ns] (if external bus cycle is a}\phi + b\phi\text{, m = b)}$$

$$tw(WR) = \frac{10^9 \times n}{f(BCLK) \times 2} - 15 \text{ [ns] (if external bus cycle is a}\phi + b\phi\text{, n = (b × 2) - 1)}$$

3. tc [ns] is added when recovery cycle is inserted.

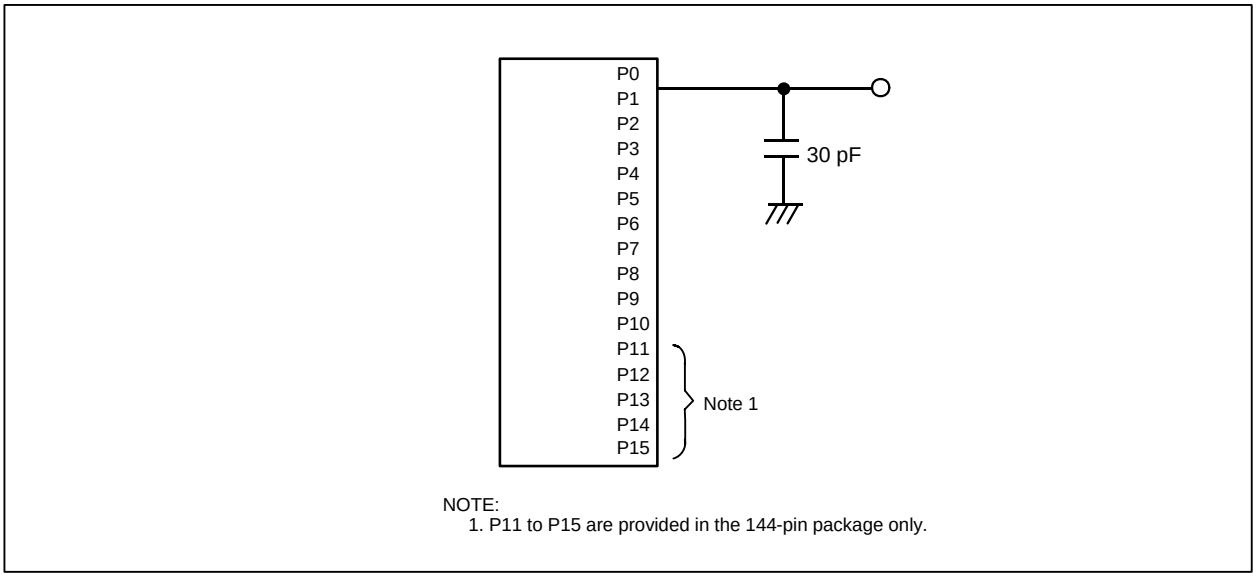


Figure 5.2 P0 to P15 Measurement Circuit

VCC1 = VCC2 = 3.3 V

Table 5.31 Electrical Characteristics (1/3)

(VCC1 = VCC2 = 3.0 to 3.6 V, VSS = 0 V, Topr = -20 to 85°C, f(CPU) = 24 MHz unless otherwise specified)

Symbol	Parameter		Measurement Condition	Standard			Unit
				Min.	Typ.	Max.	
VOH	Output high “H” voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7(1)	IOH = -1 mA	VCC2 - 0.6		VCC2	V
		P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7,P10_0 to P10_7, P14_0 to P14_6, P15_0 to P15_7(1)		VCC1 - 0.6		VCC1	
		XOUT	IOH = -0.1 mA	2.7		VCC1	V
		XCOUT Drive capability = high	No load applied		2.5		V
		XCOUT Drive capability = low	No load applied		1.6		V
VOL	Output low “L” voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7,P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7(1)	IOL = 1 mA			0.5	V
		XOUT	IOL = 0.1 mA			0.5	V
		XCOUT Drive capability = high	No load applied		0		V
		XCOUT Drive capability = low	No load applied		0		V
VT+ - VT-	Hysteresis	$\overline{\text{HOLD}}$, $\overline{\text{RDY}}$, TA0IN to TA4IN, $\overline{\text{TB0IN}}$ to $\overline{\text{TB5IN}}$, $\overline{\text{INT0}}$ to $\overline{\text{INT8}}$, $\overline{\text{ADTRG}}$, $\overline{\text{CTS0}}$ to $\overline{\text{CTS6}}$, CLK0 to CLK6, TA0OUT to TA4OUT, $\overline{\text{NMI}}$, $\overline{\text{KI0}}$ to $\overline{\text{KI3}}$, RXD0 to RXD6, SCL0 to SCL4, SDA0 to SDA4, INPC1_0 to INPC1_7, ISCLK0 to ISCLK2, ISRXD0 to ISRXD2, IEIN, CAN0IN, CAN1IN, $\overline{\text{CAN1WU}}$		0.2		1.0	V
		$\overline{\text{RESET}}$		0.2		1.8	V

NOTE:

1. P11 to P15 are provided in the 144-pin package only.

VCC1 = VCC2 = 3.3 V

Timing Requirements
(VCC1 = VCC2 = 3.0 to 3.6 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.36 External Clock Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc	External clock input cycle time	41		ns
tw(H)	External clock input high (“H”) pulse width	18		ns
tw(L)	External clock input low (“L”) pulse width	18		ns
tr	External clock rise time		5	ns
tf	External clock fall time		5	ns

Table 5.37 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	100		ns
tw(TAH)	TAiIN input high (“H”) pulse width	40		ns
tw(TAL)	TAiIN input low (“L”) pulse width	40		ns

i = 0 to 4

Table 5.38 Timer A Input (Gate Signal Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	400		ns
tw(TAH)	TAiIN input high (“H”) pulse width	200		ns
tw(TAL)	TAiIN input low (“L”) pulse width	200		ns

i = 0 to 4

Table 5.39 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	200		ns
tw(TAH)	TAiIN input high (“H”) pulse width	100		ns
tw(TAL)	TAiIN input low (“L”) pulse width	100		ns

i = 0 to 4

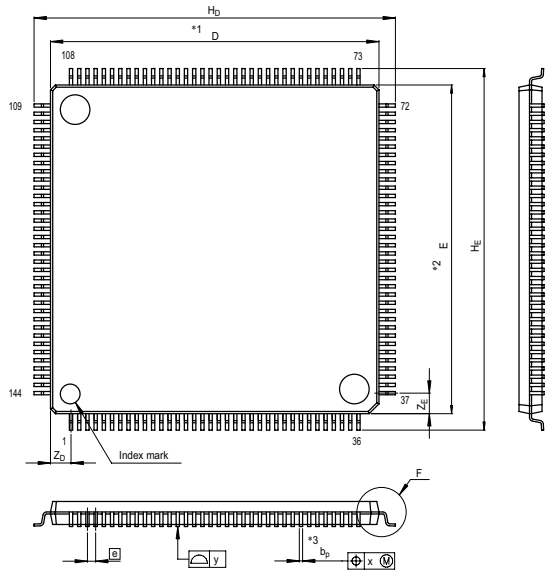
Table 5.40 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

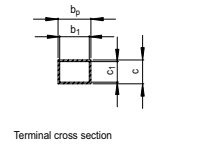
Symbol	Parameter	Standard		Unit
		Min.	Max.	
tw(TAH)	TAiIN input high (“H”) pulse width	100		ns
tw(TAL)	TAiIN input low (“L”) pulse width	100		ns

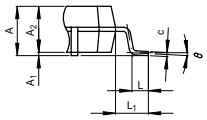
i = 0 to 4

Appendix 1. Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP144-20x20-0.50	PLQP0144KA-A	144P6Q-A / FP-144L / FP-144LV	1.2g



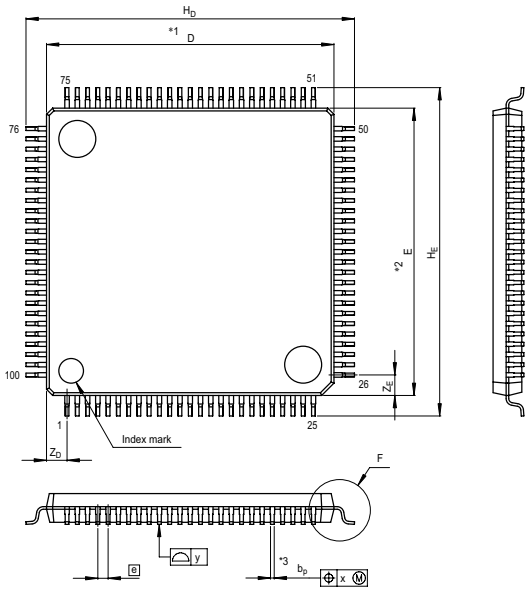


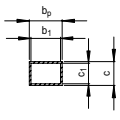


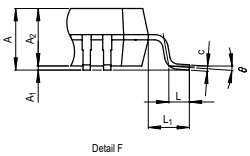
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.9	20.0	20.1
E	19.9	20.0	20.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g







NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.35	0.5	0.65
L_1	—	1.0	—

REVISION HISTORY	M32C/87 Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.50	Dec.16, 04	–	New Document
1.00	Jul.14, 05	–	**M32C/87A and M32C/87B** added
		–	Package code changed: 144P6Q-A to PLQP0144KA-A, 100P6Q-A to PLQP0100KB-A, 100P6S-A to PRQP0100JB-A
		–	"Low Voltage Detection Reset" changed to "Brown-out Detection Reset"
			Overview
		2	• **Table 1.2 M32C/87 Group Performance (144-Pin Package)** M32C/87A and M32C/87B performance added to the CAN module performance; Power Consumption performance released
		3	• **Table 1.2 M32C/87 Group Performance (100-Pin Package)** M32C/87A and M32C/87B performance added to the CAN module performance; Power Consumption performance released
		4	• **Figure 1.1 M32C/87 Group Block Diagram** Note 4 deleted; note 5 added
		7	• **Figure 1.3 Pin Assignment for 144-Pin Package** Note 15 added
		8	• **Table 1.4 Pin Characteristics for 144-Pin Package** Note 1 added
		11	• **Figure 1.4 Pin Assignment for 100-Pin Package** Note 19 added
		12	• **Figure 1.5 Pin Assignment for 100-Pin Package** Note 15 added
		13	• **Table 1.5 Pin Characteristics for 100-Pin Package** Note 1 added
		17	• **Table 1.6 Pin Description** Note 2 added
			Memory
		22	• **Figure 3.1 Memory Map** Note 3 changed
			Special Function Register (SFR)
		26	• The RLVL register Value after reset modified
		26	• The IIO0IR to IIO11IR registers Value after reset modified
		27 to 30	• Name of the registers assosiated to Intelligent I/O changed
		27	• The G0RB register Value after reset modified
		27	• The G1BCR0 and G1BCR1 registers Value after reset modified
		29	• The G0CR register Value after reset modified
		32 to 37	• Note added to the CAN-associated registers
		40	• The TCSPR register Value after reset modified; note 1 added
		41	• The AD00 register Value after reset modified
		42	• The PSC register Value after reset modified
		42	• The PS2 register Value after reset modified
		43	• The PCR register Value after reset modified
		44	• The PSD1 register Value after reset modified
		45	• The PCR register Value after reset modified
			Electrical Characteristics
		48	• **Table 5.2 Electrical Characteristics** Parameter f(BCLK) and its values added; min. and max. values for f(RING) added
		49	• **Table 5.3 Electrical Characteristics** V_{OH} values modified**;** R_{PULLUP} value modified
		50	• **Table 5.3 Electrical Characteristics (Continued)** Measurement Condition and standard values for ICC added and some released
		52	• **Table 5.6 Flash Memory Version Electrical Characteristics** Word Program Time and Lock bit Program Time values modified; parameter All-Unlocked-Block-Erase Time deleted; note 1 deleted
		54	• **Table 5.10 Memory Expansion Mode and Microprocessor Mode** *tac1(RD-DB)* expression on note 1 modified; *tac2(RD-DB)* expression on note 1 added

REVISION HISTORY	M32C/87 Group Datasheet

Rev.	Date	Description	
		Page	Summary
			SFR
		42	• [Register names changed] 0342h One-Shot Start Flag → One-Shot Start Register 0344h Up-Down Flag → Up/Down Select Register
			• [Value After Reset changed]
		27	000Fh WDC 000X XXX$_2$ → 00XX XXXXb
		27	002Fh D4INT 00$_{16}$ → XX00 0000b
		29	007Bh IIO6IC XX00 X000$_2$ → XXXX X000b
		31	00EFh G0CR XX00 X011$_2$ → 0000 X011b
		31	00FEh G0IRF 00$_{16}$ → 0000 XXXXb
		32	013Eh G1IRF 00$_{16}$ → 0000 XXXXb
		34	01C7h to 01C6h U5RB XXXX XXXX XXXX 0XXX$_2$ → XXXXh
		34	01CFh to 01CEh U6RB XXXX XXXX XXXX 0XXX$_2$ → XXXXh
		44	038Fh to 0382h AD07 to AD01 XXXX$_{16}$ → 00XXh
			Electrical Characteristics
			• [Term changed] Low Voltage Reset → Hardware Reset 2 Low Voltage Detection → Vdet3 and Vdet4 detection circuit
		47	• **Table 5.1** Description in Condition field of Pd (Power consumption) partially modified
		50-53	• **Tables 5.2** to **5.9** f(BCLK) is changed to f(CPU)
		50	• **Table 5.4** Description added in Parameter field of f(CPU); f(VCO) added
		51,69	• **Tables 5.5** to **5.7** and **Tables 5.31** to **5.33** Description in XCOUT and Hysteresis in Parameter fields partially modified
		53,71	• **Table 5.7** and **5.33** Structure and standard values revised; items in Measurement Condition and NOTE added
		54	• **Table 5.8** Description in Parameter field and NOTE partially modified
		54,55	• **Table 5.9** and **5.10** Description in Parameter field and NOTE partially modified
		56,73	• **Tables 5.11** and **5.36** Description in Parameter field and standard value partially modified
		58,74	• **Tables 5.19** and **5.42** added
		59	• **Table 5.24** Values revised; **Table 5.25** and **5.26 added**
		60	• **Table 5.27** Titles modified; NOTE added
		61	• **Table 5.28** moved to the last table in Timing Requirements
		62-63	• **Table 5.29** NOTE 3 added; **Table 26.30** NOTE 5 added
		65-68	• **Figures 5.3** to **5.6** Order rearranged; measurement condition modified
		69-72	• **Table 5.31** to **5.35** f(BCLK) revised to f(CPU)
		75	• **Table 5.47** Values revised; **Table5.48** and **5.49** added
		76	• **Table 5.50** Titles modified; NOTE added
		77	• **Table 5.51** Table moved to the last table in Timing Requirements
		78-79	• **Table 5.52** NOTE 3 added**; Table 5.53** NOTE 5 added
		80-83	• **Figures 5.7** to **5.10** Order rearranged
1.51	Jul 31, 2008	–	**All in this manual** [description modified] • Title of group tables “(current table number / total tables)” added
			Overview
		19	• **1.5 Pin Descriptions** Chapter and table title changed to **Pin Functions**
		21	• **Table 1.17** Supply voltage for AN0_0 to AN0_7, AN2_0 to AN2_7 modified

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