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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	M32C/80
Core Size	16/32-Bit
Speed	32MHz
Connectivity	CANbus, EBI/EMI, I ² C, IEBus, IrDA, SIO, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	85
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	31K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30876fjagp-u3

1. Overview

1.1 Features

The M32C/87 Group (M32C/87, M32C/87A, M32C/87B) is a single-chip control MCU, fabricated using high-performance silicon gate CMOS technology, embedding the M32C/80 Series CPU core. The M32C/87 Group (M32C/87, M32C/87A, M32C/87B) is housed in 144-pin and 100-pin plastic molded LQFP/QFP packages.

With a 16-Mbyte address space, this MCU combines advanced instruction manipulation capabilities to process complex instructions by less bytes and execute instructions at higher speed.

The M32C/87 Group (M32C/87, M32C/87A, M32C/87B) has a multiplier and DMAC adequate for office automation, communication devices and industrial equipment, and other high-speed processing applications.

1.1.1 Applications

Audio components, cameras, office equipment, communication devices, mobile devices, etc.

Table 1.2 Specifications (144-Pin Package) (2/2)

Item	Function	Specification
Serial Interface	UART0 to UART4	Clock synchronous/asynchronous × 5 I ² C bus, special mode 2, GCI mode, SIM mode, IrDA mode ⁽²⁾ , IEBus (optional) ⁽¹⁾⁽³⁾
	UART5, UART6	Clock synchronous/asynchronous × 2
A/D Converter		10-bit resolution × 34 channels (in single-chip mode) 10-bit resolution × 18 channels (in memory expansion mode and microprocessor mode) Including sample and hold function
D/A Converter		8-bit resolution × 2 channels
CRC Calculation Circuit		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) compliant
X/Y Converter		16 bits × 16 bits
Intelligent I/O		16-bit timer × 2 • Time measurement function (input capture): 8 channels • Waveform generation function (output compare): 16 channels • Communication function: Clock synchronous mode, clock asynchronous mode, HDLC data processing mode, IEBus (optional) ⁽¹⁾⁽³⁾ • 2-phase pulse signal processing (2-phase encoder input) × 1
ROM Correction Function		Address match interrupt × 8
CAN modules		Supporting CAN 2.0B specification M32C/87: 16 slots × 2 channels, M32C/87A: 16 slots × 1 channel M32C/87B: none
I/O Ports	Programmable I/O ports	• Input only: 1 • CMOS I/O: 121 with selectable pull-up resistor • N channel open drain ports: 2
Flash Memory		• Erase and program voltage: 3.3 V ± 0.3 V or 5.0 V ± 0.5 V • Erase and program endurance: 100 times (all areas) • Program security: ROM code protect and ID code check • Debug functions: On-chip debug and on-board flash reprogram
Operating Frequency/Supply Voltage		32 MHz: VCC1 = 4.2 to 5.5 V, VCC2 = 3.0 V to VCC1 24 MHz: VCC1 = 3.0 to 5.5 V, VCC2 = 3.0 V to VCC1
Current Consumption		32 mA (32 MHz, VCC1 = VCC2 = 5 V) 23 mA (24 MHz, VCC1 = VCC2 = 3.3 V) 45 μA (approx. 1 MHz, VCC1 = VCC2 = 3.3 V, on-chip oscillator low-power consumption mode → wait mode) 0.8 μA (VCC1 = VCC2 = 3.3 V, stop mode)
Operating Ambient Temperature (°C)		-20 to 85°C, -40 to 85°C (optional) ⁽³⁾
Package		144-pin LQFP (PLQP0144KA-A)

NOTES:

1. IEBus is a registered trademark of NEC Electronics Corporation.
2. Available in UART0.
3. Please contact a Renesas sales office for optional features.

1.2 Product List

Tables 1.5 to 1.7 list product information. Figure 1.1 shows product numbering system.

Table 1.5 M32C/87 Group (1) (M32C/87: 2-channel CAN module) Current as of Jul. 2008

Part Number	Package Code	ROM Capacity	RAM Capacity	Remarks
M3087BFLGP	PLQP0144KA-A (144P6Q-A)	1 MB + 4 KB ⁽¹⁾	48 KB	Flash memory
M30879FLFP	PRQP0100JB-A (100P6S-A)			
M30879FLGP	PLQP0100KB-A (100P6Q-A)			
M3087BFGKP	PLQP0144KA-A (144P6Q-A)	768 KB + 4 KB ⁽¹⁾		
M30879FKGP	PLQP0100KB-A (100P6Q-A)			
M30878FJGP	PLQP0144KA-A (144P6Q-A)	512 KB + 4 KB ⁽¹⁾	31 KB	
M30876FJGP	PLQP0100KB-A (100P6Q-A)			
M30875FHGP	PLQP0144KA-A (144P6Q-A)	384 KB + 4 KB ⁽¹⁾	24 KB	
M30873FHGP	PLQP0100KB-A (100P6Q-A)			
M30878MJ-XXXGP	PLQP0144KA-A (144P6Q-A)	512 KB	31 KB	Mask ROM
M30876MJ-XXXFP	PRQP0100JB-A (100P6S-A)			
M30876MJ-XXXGP	PLQP0100KB-A (100P6Q-A)			
M30875MH-XXXGP	PLQP0144KA-A (144P6Q-A)	384 KB	24 KB	
M30873MH-XXXGP	PLQP0100KB-A (100P6Q-A)			

NOTE:

1. Additional 4-Kbyte space is available for data flash memory.

Table 1.6 M32C/87 Group (2) (M32C/87A: 1-channel CAN module) Current as of Jul. 2008

Part Number	Package Code	ROM Capacity	RAM Capacity	Remarks
M3087BFLAGP	PLQP0144KA-A (144P6Q-A)	1 MB + 4 KB ⁽¹⁾	48 KB	Flash memory
M30879FLAFP	PRQP0100JB-A (100P6S-A)			
M30879FLAGP	PLQP0100KB-A (100P6Q-A)			
M3087BFKAGP	PLQP0144KA-A (144P6Q-A)	768 KB + 4 KB ⁽¹⁾		
M30879FKAGP	PLQP0100KB-A (100P6Q-A)			
M30878FJAGP	PLQP0144KA-A (144P6Q-A)	512 KB + 4 KB ⁽¹⁾	31 KB	
M30876FJAGP	PLQP0100KB-A (100P6Q-A)			
M30875FHAGP	PLQP0144KA-A (144P6Q-A)	384 KB + 4 KB ⁽¹⁾	24 KB	
M30873FHAGP	PLQP0100KB-A (100P6Q-A)			
M30878MJA-XXXGP	PLQP0144KA-A (144P6Q-A)	512 KB	31 KB	Mask ROM
M30876MJA-XXXFP	PRQP0100JB-A (100P6S-A)			
M30876MJA-XXXGP	PLQP0100KB-A (100P6Q-A)			
M30875MHA-XXXGP	PLQP0144KA-A (144P6Q-A)	384 KB	24 KB	
M30873MHA-XXXGP	PLQP0100KB-A (100P6Q-A)			

NOTE:

1. Additional 4-Kbyte space is available for data flash memory.

1.3 Block Diagram

Figure 1.2 shows a block diagram of the M32C/87 Group (M32C/87, M32C/87A, M32C/87B).

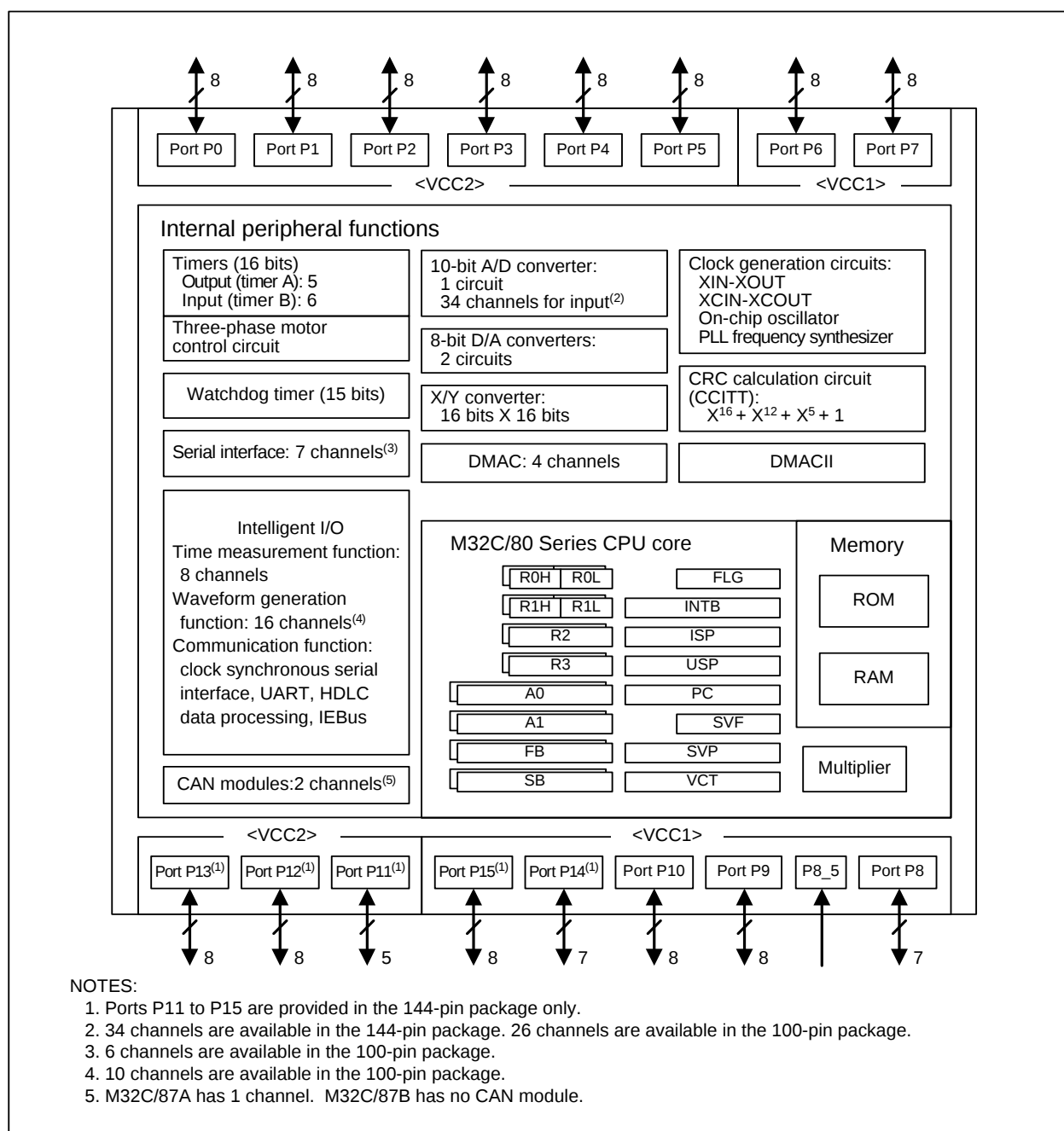


Figure 1.2 M32C/87 Group (M32C/87, M32C/87A, M32C/87B) Block Diagram

Table 1.9 144-Pin Package List of Pin Names (2/4)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
41	VSS							
42		P6_5			CLK1			
43		P6_4			CTS1/RTS1/SS1	OUTC2_1/ISCLK2		
44		P6_3			TXD0/SDA0/SRXD0/ IrDAOUT			
45		P6_2			RXD0/SCL0/STXD0/ IrDAIN			
46		P6_1		RTP0_1	CLK0			
47		P6_0		RTP0_0	CTS0/RTS0/SS0			
48		P13_7				OUTC2_7		
49		P13_6				OUTC2_1/ISCLK2		
50		P13_5				OUTC2_2/ISRXD2/ IEIN		
51		P13_4				OUTC2_0/ISTXD2/ IEOUT		
52		P5_7						RDY
53		P5_6						ALE
54		P5_5						HOLD
55		P5_4						HLDA/ALE
56		P13_3				OUTC2_3		
57	VSS							
58		P13_2				OUTC2_6		
59	VCC2							
60		P13_1				OUTC2_5		
61		P13_0				OUTC2_4		
62	CLKOUT	P5_3						BCLK/ALE
63		P5_2						RD
64		P5_1						WRH/BHE
65		P5_0						WRL/WR
66		P12_7						
67		P12_6						
68		P12_5						
69		P4_7						CS0/A23
70		P4_6						CS1/A22
71		P4_5						CS2/A21
72		P4_4						CS3/A20
73		P4_3						A19
74	VCC2							
75		P4_2						A18
76	VSS							
77		P4_1						A17
78		P4_0						A16
79		P3_7						A15,[A15/D15]
80		P3_6						A14,[A14/D14]

Table 1.11 144-Pin Package List of Pin Names (4/4)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
121		P0_1					AN0_1	D1
122		P0_0					AN0_0	D0
123		P15_7			CTS6/RTS6		AN15_7	
124		P15_6			CLK6		AN15_6	
125		P15_5			RXD6		AN15_5	
126		P15_4			TXD6		AN15_4	
127		P15_3			CTS5/RTS5		AN15_3	
128		P15_2			RXD5	ISRXD0	AN15_2	
129		P15_1			CLK5	ISCLK0	AN15_1	
130	VSS							
131		P15_0			TXD5	ISTXD0	AN15_0	
132	VCC1							
133		P10_7	KI3	RTP3_3			AN_7	
134		P10_6	KI2	RTP3_2			AN_6	
135		P10_5	KI1	RTP3_1			AN_5	
136		P10_4	KI0	RTP3_0			AN_4	
137		P10_3		RTP1_3			AN_3	
138		P10_2		RTP1_2			AN_2	
139		P10_1		RTP1_1			AN_1	
140	AVSS							
141		P10_0		RTP1_0			AN_0	
142	VREF							
143	AVCC							
144		P9_7			RXD4/SCL4/STXD4		ADTRG	

Table 1.14 100-Pin Package List of Pin Names (3/3)

Pin No.		Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
FP	GP								
73	71		P1_7	INT5					D15
74	72		P1_6	INT4					D14
75	73		P1_5	INT3					D13
76	74		P1_4						D12
77	75		P1_3						D11
78	76		P1_2						D10
79	77		P1_1						D9
80	78		P1_0						D8
81	79		P0_7					AN0_7	D7
82	80		P0_6					AN0_6	D6
83	81		P0_5					AN0_5	D5
84	82		P0_4					AN0_4	D4
85	83		P0_3					AN0_3	D3
86	84		P0_2					AN0_2	D2
87	85		P0_1					AN0_1	D1
88	86		P0_0					AN0_0	D0
89	87		P10_7	KI3	RTP3_3			AN_7	
90	88		P10_6	KI2	RTP3_2			AN_6	
91	89		P10_5	KI1	RTP3_1			AN_5	
92	90		P10_4	KI0	RTP3_0			AN_4	
93	91		P10_3		RTP1_3			AN_3	
94	92		P10_2		RTP1_2			AN_2	
95	93		P10_1		RTP1_1			AN_1	
96	94	AVSS							
97	95		P10_0		RTP1_0			AN_0	
98	96	VREF							
99	97	AVCC							
100	98		P9_7			RXD4/SCL4/STXD4		ADTRG	

Table 4.3 SFR Address Map (3/20)

Address	Register	Symbol	After Reset
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h	DMA0 Interrupt Control Register	DM0IC	XXXX X000b
0069h	Timer B5 Interrupt Control Register	TB5IC	XXXX X000b
006Ah	DMA2 Interrupt Control Register	DM2IC	XXXX X000b
006Bh	UART2 Receive/ACK Interrupt Control Register	S2RIC	XXXX X000b
006Ch	Timer A0 Interrupt Control Register	TA0IC	XXXX X000b
006Dh	UART3 Receive/ACK Interrupt Control Register	S3RIC	XXXX X000b
006Eh	Timer A2 Interrupt Control Register	TA2IC	XXXX X000b
006Fh	UART4 Receive/ACK Interrupt Control Register	S4RIC	XXXX X000b
0070h	Timer A4 Interrupt Control Register	TA4IC	XXXX X000b
0071h	UART0/UART3 Bus Conflict Detection Interrupt Control Register	BCN0IC/BCN3IC	XXXX X000b
0072h	UART0 Receive/ACK Interrupt Control Register	S0RIC	XXXX X000b
0073h	A/D0 Conversion Interrupt Control Register	AD0IC	XXXX X000b
0074h	UART1 Receive/ACK Interrupt Control Register	S1RIC	XXXX X000b
0075h	I/O Interrupt Control Register 0 / CAN1 interrupt Control Register 0	IIO0IC/CAN3IC	XXXX X000b
0076h	Timer B1 Interrupt Control Register	TB1IC	XXXX X000b
0077h	I/O Interrupt Control Register 2	IIO2IC	XXXX X000b
0078h	Timer B3 Interrupt Control Register	TB3IC	XXXX X000b
0079h	I/O Interrupt Control Register 4	IIO4IC	XXXX X000b
007Ah	INT5 Interrupt Control Register	INT5IC	XX00 X000b
007Bh	I/O Interrupt Control Register 6	IIO6IC	XXXX X000b
007Ch	INT3 Interrupt Control Register	INT3IC	XX00 X000b
007Dh	I/O Interrupt Control Register 8	IIO8IC	XXXX X000b
007Eh	INT1 Interrupt Control Register	INT1IC	XX00 X000b
007Fh	I/O Interrupt Control Register 10 / CAN0 Interrupt Control Register 1	IIO10IC/CAN1IC	XXXX X000b
0080h			
0081h	I/O Interrupt Control Register 11 / CAN0 Interrupt Control Register 2	IIO11IC/CAN2IC	XXXX X000b
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h	DMA1 Interrupt Control Register	DM1IC	XXXX X000b
0089h	UART2 Transmit/NACK Interrupt Control Register	S2TIC	XXXX X000b
008Ah	DMA3 Interrupt Control Register	DM3IC	XXXX X000b
008Bh	UART3 Transmit/NACK Interrupt Control Register	S3TIC	XXXX X000b
008Ch	Timer A1 Interrupt Control Register	TA1IC	XXXX X000b
008Dh	UART4 Transmit/NACK Interrupt Control Register	S4TIC	XXXX X000b
008Eh	Timer A3 Interrupt Control Register	TA3IC	XXXX X000b
008Fh	UART2 Bus Conflict Detection Interrupt Control Register	BCN2IC	XXXX X000b

X: Undefined

Blank spaces are all reserved. No access is allowed.

Table 4.7 SFR Address Map (7/20)

Address	Register	Symbol	After Reset
0150h	Group 2 Waveform Generation Control Register 0	G2POCR0	00h
0151h	Group 2 Waveform Generation Control Register 1	G2POCR1	00h
0152h	Group 2 Waveform Generation Control Register 2	G2POCR2	00h
0153h	Group 2 Waveform Generation Control Register 3	G2POCR3	00h
0154h	Group 2 Waveform Generation Control Register 4	G2POCR4	00h
0155h	Group 2 Waveform Generation Control Register 5	G2POCR5	00h
0156h	Group 2 Waveform Generation Control Register 6	G2POCR6	00h
0157h	Group 2 Waveform Generation Control Register 7	G2POCR7	00h
0158h			
0159h			
015Ah			
015Bh			
015Ch			
015Dh			
015Eh			
015Fh			
0160h	Group 2 Base Timer Register	G2BT	XXXXh
0161h			
0162h	Group 2 Base Timer Control Register 0	G2BCR0	00h
0163h	Group 2 Base Timer Control Register 1	G2BCR1	00h
0164h	Base Timer Start Register	BTSR	XXXX 0000b
0165h			
0166h	Group 2 Function Enable Register	G2FE	00h
0167h	Group 2 RTP Output Buffer Register	G2RTP	00h
0168h			
0169h			
016Ah	Group 2 SI/O Communication Mode Register	G2MR	00XX X000b
016Bh	Group 2 SI/O Communication Control Register	G2CR	0000 X000b
016Ch	Group 2 SI/O Transmit Buffer Register	G2TB	XXXXh
016Dh			
016Eh	Group 2 SI/O Receive Buffer Register	G2RB	XXXXh
016Fh			
0170h	Group 2 IEBus Address Register	IEAR	XXXXh
0171h			
0172h	Group 2 IEBus Control Register	IECR	00XX X000b
0173h	Group 2 IEBus Transmit Interrupt Source Detection Register	IETIF	XXX0 0000b
0174h	Group 2 IEBus Receive Interrupt Source Detection Register	IERIF	XXX0 0000b
0175h			
0176h			
0177h	Input Function Select Register B	IPSB	00h
0178h	Input Function Select Register	IPS	00h
0179h	Input Function Select Register A	IPSA	00h
017Ah			
017Bh			
017Ch			
017Dh to 01BFh			

X: Undefined

Blank spaces are all reserved. No access is allowed.

Table 4.10 SFR Address Map (10/20)

Address	Register ⁽³⁾⁽⁴⁾	Symbol	After Reset
0220h	CAN0 Single Shot Control Register	C0SCTLR	0000h ⁽¹⁾⁽²⁾
0221h			
0222h			
0223h			
0224h	CAN0 Single Shot Status Register	C0SSSTR	0000h ⁽¹⁾⁽²⁾
0225h			
0226h			
0227h			
0228h	CAN0 Global Mask Register Standard ID0	C0GMR0	XXX0 0000b ⁽¹⁾⁽²⁾
0229h	CAN0 Global Mask Register Standard ID1	C0GMR1	XX00 0000b ⁽¹⁾⁽²⁾
022Ah	CAN0 Global Mask Register Extended ID0	C0GMR2	XXXX 0000b ⁽¹⁾⁽²⁾
022Bh	CAN0 Global Mask Register Extended ID1	C0GMR3	00h ⁽¹⁾⁽²⁾
022Ch	CAN0 Global Mask Register Extended ID2	C0GMR4	XX00 0000b ⁽¹⁾⁽²⁾
022Dh			
022Eh			
022Fh			
0230h	CAN0 Message Slot 0 Control Register / CAN0 Local Mask Register A Standard ID0	C0MCTL0 / C0LMAR0	0000 0000b ⁽¹⁾⁽²⁾ / XXX0 0000b ⁽¹⁾⁽²⁾
0231h	CAN0 Message Slot 1 Control Register / CAN0 Local Mask Register A Standard ID1	C0MCTL1 / C0LMAR1	0000 0000b ⁽¹⁾⁽²⁾ / XX00 0000b ⁽¹⁾⁽²⁾
0232h	CAN0 Message Slot 2 Control Register / CAN0 Local Mask Register A Extended ID0	C0MCTL2 / C0LMAR2	0000 0000b ⁽¹⁾⁽²⁾ / XXXX 0000b ⁽¹⁾⁽²⁾
0233h	CAN0 Message Slot 3 Control Register / CAN0 Local Mask Register A Extended ID1	C0MCTL3 / C0LMAR3	00h ⁽¹⁾⁽²⁾ / 00h ⁽¹⁾⁽²⁾
0234h	CAN0 Message Slot 4 Control Register / CAN0 Local Mask Register A Extended ID2	C0MCTL4 / C0LMAR4	0000 0000b ⁽¹⁾⁽²⁾ / XX00 0000b ⁽¹⁾⁽²⁾
0235h	CAN0 Message Slot 5 Control Register	C0MCTL5	00h ⁽¹⁾⁽²⁾
0236h	CAN0 Message Slot 6 Control Register	C0MCTL6	00h ⁽¹⁾⁽²⁾
0237h	CAN0 Message Slot 7 Control Register	C0MCTL7	00h ⁽¹⁾⁽²⁾
0238h	CAN0 Message Slot 8 Control Register / CAN0 Local Mask Register B Standard ID0	C0MCTL8 / C0LMAR0	0000 0000b ⁽¹⁾⁽²⁾ / XXX0 0000b ⁽¹⁾⁽²⁾
0239h	CAN0 Message Slot 9 Control Register / CAN0 Local Mask Register B Standard ID1	C0MCTL9 / C0LMAR1	0000 0000b ⁽¹⁾⁽²⁾ / XX00 0000b ⁽¹⁾⁽²⁾
023Ah	CAN0 Message Slot 10 Control Register / CAN0 Local Mask Register B Extended ID0	C0MCTL10 / C0LMAR2	0000 0000b ⁽¹⁾⁽²⁾ / XXXX 0000b ⁽¹⁾⁽²⁾
023Bh	CAN0 Message Slot 11 Control Register / CAN0 Local Mask Register B Extended ID1	C0MCTL11 / C0LMAR3	00h ⁽¹⁾⁽²⁾ / 00h ⁽¹⁾⁽²⁾
023Ch	CAN0 Message Slot 12 Control Register / CAN0 Local Mask Register B Extended ID2	C0MCTL12 / C0LMAR4	0000 0000b ⁽¹⁾⁽²⁾ / XX00 0000b ⁽¹⁾⁽²⁾
023Dh	CAN0 Message Slot 13 Control Register	C0MCTL13	00h ⁽¹⁾⁽²⁾
023Eh	CAN0 Message Slot 14 Control Register	C0MCTL14	00h ⁽¹⁾⁽²⁾
023Fh	CAN0 Message Slot 15 Control Register	C0MCTL15	00h ⁽¹⁾⁽²⁾
0240h	CAN0 Slot Buffer Select Register	C0SBS	00h ⁽²⁾
0241h	CAN0 Control Register 1	C0CTLR1	X000 00XXb ⁽²⁾
0242h	CAN0 Sleep Control Register	C0SLPR	XXXX XXX0b
0243h			
0244h	CAN0 Acceptance Filter Support Register	C0AFS	0000 0000b ⁽²⁾ 0000 0001b ⁽²⁾
0245h			
0246h			
0247h			
0248h			
0249h			
024Ah to 024Fh			

X: Undefined

Blank spaces are all reserved. No access is allowed.

NOTES:

1. The BANKSEL bit in the C0CTLR1 register can switch functions for addresses 0220h to 023Fh.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) after reset and supplying a clock to the CAN module.
3. The CAN-associated registers (allocated in addresses 01E0h to 02BFh) cannot be used in M32C/87B. In M32C/87A, only CAN0-associated registers can be used.
4. Set the PM13 bit in the PM1 register to 1 (2 wait states for SFR area) before accessing the CAN-associated registers.

Table 4.12 SFR Address Map (12/20)

Address	Register ⁽³⁾ (4)	Symbol	After Reset
0280h	CAN1 Control Register 0	C1CTLR0	XX01 0X01b ⁽²⁾
0281h			XXXX 0000b ⁽²⁾
0282h	CAN1 Status Register	C1STR	0000 0000b ⁽²⁾
0283h			X000 0X01b ⁽²⁾
0284h	CAN1 Extended ID Register	C1IDR	0000h ⁽²⁾
0285h			
0286h	CAN1 Configuration Register	C1CONR	0000 XXXXb ⁽²⁾
0287h			0000 0000b ⁽²⁾
0288h	CAN1 Time Stamp Register	C1TSR	0000h ⁽²⁾
0289h			
028Ah	CAN1 Transmit Error Count Register	C1TEC	00h ⁽²⁾
028Bh	CAN1 Receive Error Count Register	C1REC	00h ⁽²⁾
028Ch	CAN1 Slot Interrupt Status Register	C1SISTR	0000h ⁽²⁾
028Dh			
028Eh			
028Fh			
0290h	CAN1 Slot Interrupt Mask Register	C1SIMKR	0000h ⁽²⁾
0291h			
0292h			
0293h			
0294h	CAN1 Error Interrupt Mask Register	C1EIMKR	XXXX X000b ⁽²⁾
0295h	CAN1 Error Interrupt Status Register	C1EISTR	XXXX X000b ⁽²⁾
0296h	CAN1 Error Source Register	C1EFR	00h ⁽²⁾
0297h	CAN1 Baud Rate Prescaler	C1BRP	0000 0001b ⁽²⁾
0298h			
0299h	CAN1 Mode Register	C1MDR	XXXX XX00b ⁽²⁾
029Ah			
029Bh			
029Ch			
029Dh			
029Eh			
029Fh			
02A0h	CAN1 Single Shot Control Register	C1SSCTLR	0000h ⁽¹⁾⁽²⁾
02A1h			
02A2h			
02A3h			
02A4h	CAN1 Single Shot Status Register	C1SSSTR	0000h ⁽¹⁾⁽²⁾
02A5h			
02A6h			
02A7h			
02A8h	CAN1 Global Mask Register Standard ID0	C1GMR0	XXX0 0000b ⁽¹⁾⁽²⁾
02A9h	CAN1 Global Mask Register Standard ID1	C1GMR1	XX00 0000b ⁽¹⁾⁽²⁾
02AAh	CAN1 Global Mask Register Extended ID0	C1GMR2	XXXX 0000b ⁽¹⁾⁽²⁾
02ABh	CAN1 Global Mask Register Extended ID1	C1GMR3	00h ⁽¹⁾⁽²⁾
02ACh	CAN1 Global Mask Register Extended ID2	C1GMR4	XX00 0000b ⁽¹⁾⁽²⁾
02ADh			
02AEh			
02AFh			

X: Undefined

Blank spaces are all reserved. No access is allowed.

NOTES:

1. The BANKSEL bit in the C0CTLR1 register can switch functions for addresses 02A0h to 02BFh.
2. Values are obtained by setting the SLEEP bit in the C1SLPR register to "1" (sleep mode exited) after reset and supplying a clock to the CAN module.
3. The CAN-associated registers (allocated in addresses 01E0h to 02BFh) cannot be used in M32C/87B. In M32C/87A, only CAN0-associated registers can be used.
4. Set the PM13 bit in the PM1 register to 1 (2 wait states for SFR area) before accessing the CAN-associated registers.

Table 4.20 SFR Address Map (20/20)

Address	Register	Symbol	After Reset
03D0h	Port P14 Register ⁽¹⁾	P14	XXh
03D1h	Port P15 Register ⁽¹⁾	P15	XXh
03D2h	Port P14 Direction Register ⁽¹⁾⁽²⁾	PD14	X000 0000b
03D3h	Port P15 Direction Register ⁽¹⁾⁽²⁾	PD15	00h
03D4h			
03D5h			
03D6h			
03D7h			
03D8h			
03D9h			
03DAh	Pull-Up Control Register 2	PUR2	00h
03DBh	Pull-Up Control Register 3	PUR3	00h
03DCh	Pull-Up Control Register 4 ⁽¹⁾⁽³⁾	PUR4	XXXX 0000b
03DDh			
03DEh			
03DFh			
03E0h	Port P0 Register	P0	XXh
03E1h	Port P1 Register	P1	XXh
03E2h	Port P0 Direction Register	PD0	00h
03E3h	Port P1 Direction Register	PD1	00h
03E4h	Port P2 Register	P2	XXh
03E5h	Port P3 Register	P3	XXh
03E6h	Port P2 Direction Register	PD2	00h
03E7h	Port P3 Direction Register	PD3	00h
03E8h	Port P4 Register	P4	XXh
03E9h	Port P5 Register	P5	XXh
03EAh	Port P4 Direction Register	PD4	00h
03EBh	Port P5 Direction Register	PD5	00h
03ECh			
03EDh			
03EEh			
03EFh			
03F0h	Pull-Up Control Register 0	PUR0	00h
03F1h	Pull-Up Control Register 1	PUR1	XXXX 0000b
03F2h			
03F3h			
03F4h			
03F5h			
03F6h			
03F7h			
03F8h			
03F9h			
03FAh			
03FBh			
03FCh			
03FDh			
03FEh			
03FFh	Port Control Register	PCR	XXXX X000b

X: Undefined

Blank spaces are all reserved. No access is allowed.

NOTES:

1. These registers cannot be used in the 100-pin package.
2. Set to FFh in the 100-pin package.
3. Set to 00h in the 100-pin package.

Table 5.2 Recommended Operating Conditions (1/3)
(VCC1 = VCC2 = 3.0 to 5.5 V, Topr = -20 to 85°C unless otherwise specified)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
VCC1, VCC2	Supply voltage (VCC1 ≥ VCC2)		3.0	5.0	5.5	V
AVCC	Analog supply voltage			VCC1		V
VSS	Supply voltage			0		V
AVSS	Analog supply voltage			0		V
VIH	Input high "H" voltage	P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7 ⁽²⁾	0.8VCC2		VCC2	V
		P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7 ⁽¹⁾ , P9_0 to P9_7, P10_0 to P10_7, P14_0 to P14_6, P15_0 to P15_7 ⁽²⁾ , XIN, RESET, CNVSS, BYTE	0.8VCC1		VCC1	
		P7_0, P7_1	0.8VCC1		6.0	
		P0_0 to P0_7, P1_0 to P1_7 (in single-chip mode)	0.8VCC2		VCC2	
		P0_0 to P0_7, P1_0 to P1_7 (in memory expansion mode and microprocessor mode)	0.5VCC2		VCC2	
VIL	Input low "L" voltage	P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7 ⁽²⁾	0		0.2VCC2	V
		P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7 ⁽¹⁾ , P9_0 to P9_7, P10_0 to P10_7, P14_0 to P14_6, P15_0 to P15_7 ⁽²⁾ , XIN, RESET, CNVSS, BYTE	0		0.2VCC1	
		P0_0 to P0_7, P1_0 to P1_7 (in single-chip mode)	0		0.2VCC2	
		P0_0 to P0_7, P1_0 to P1_7 (in memory expansion mode and microprocessor mode)	0		0.16VCC2	

NOTES:

1. VIH and VIL reference for P8_7 apply when P8_7 is used as a programmable input port. It does not apply when P8_7 is used as XCIN.
2. P11 to P15 are provided in the 144-pin package only.

$$VCC1 = VCC2 = 5V$$

Table 5.6 Electrical Characteristics (2/3)

(VCC1 = VCC2 = 4.2 to 5.5 V, VSS = 0 V, Topr = -20 to 85°C, f(CPU) = 32 MHz unless otherwise specified)

Symbol	Parameter		Measurement Condition	Standard			Unit
				Min.	Typ.	Max.	
I _{IH}	Input high "H" current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7 ⁽¹⁾ , XIN, RESET, CNVSS, BYTE	V _I = 5 V			5.0	μA
I _{IL}	Input low "L" current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7 ⁽¹⁾ , XIN, RESET, CNVSS, BYTE	V _I = 0V			-5.0	μA
RPULLUP	Pull-up resistance	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7 ⁽¹⁾	V _I = 0V	30	50	167	kΩ
R _{fXIN}	Feedback resistance	XIN			1.5		MΩ
R _{fXCIN}	Feedback resistance	XCIN			10		MΩ
VRAM	RAM data retention voltage	In stop mode		2.0			V

NOTE:

1. P11 to P15 are provided in the 144-pin package only.

$$VCC1 = VCC2 = 5V$$

Timing Requirements

(VCC1 = VCC2 = 4.2 to 5.5 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.13 External Clock Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc	External clock input cycle time	31.25		ns
tw(H)	External clock input high ("H") pulse width	13.75		ns
tw(L)	External clock input low ("L") pulse width	13.75		ns
tr	External clock rise time		5	ns
tf	External clock fall time		5	ns

Table 5.14 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	100		ns
tw(TAH)	TAiIN input high ("H") pulse width	40		ns
tw(TAL)	TAiIN input low ("L") pulse width	40		ns

i = 0 to 4

Table 5.15 Timer A Input (Gate Signal Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	400		ns
tw(TAH)	TAiIN input high ("H") pulse width	200		ns
tw(TAL)	TAiIN input low ("L") pulse width	200		ns

i = 0 to 4

Table 5.16 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	200		ns
tw(TAH)	TAiIN input high ("H") pulse width	100		ns
tw(TAL)	TAiIN input low ("L") pulse width	100		ns

i = 0 to 4

Table 5.17 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tw(TAH)	TAiIN input high ("H") pulse width	100		ns
tw(TAL)	TAiIN input low ("L") pulse width	100		ns

i = 0 to 4

$$VCC1 = VCC2 = 5V$$

Timing Requirements

(VCC1 = VCC2 = 4.2 to 5.5 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.28 Memory Expansion mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tac1(RD-DB)	Data input access time (RD standard)		(note 1)	ns
tac1(AD-DB)	Data input access time (AD standard, CS standard)		(note 1)	ns
tac2(RD-DB)	Data input access time (RD standard, when accessing a space with the multiplexed bus)		(note 1)	ns
tac2(AD-DB)	Data input access time (AD standard, when accessing a space with the multiplexed bus)		(note 1)	ns
tsu(DB-BCLK)	Data input setup time	26		ns
tsu(RDY-BCLK)	$\overline{RDY}$ input setup time	26		ns
tsu(HOLD-BCLK)	$\overline{HOLD}$ input setup time	30		ns
th(RD-DB)	Data input hold time	0		ns
th(BCLK-RDY)	$\overline{RDY}$ input hold time	0		ns
th(BCLK-HOLD)	$\overline{HOLD}$ input hold time	0		ns
td(BCLK-HLDA)	HLDA output delay time		25	ns

NOTE:

1. Values, which depend on BCLK frequency and external bus cycles, can be obtained from the following equations. Insert wait states or lower the operation frequency, f(BCLK), if the calculated value is negative.

$$tac1(RD-DB) = \frac{10^9 \times m}{f(BCLK) \times 2} - 35 \text{ [ns]} \text{ (if external bus cycle is } a\phi + b\phi, m = (b \times 2) + 1)$$

$$tac1(AD-DB) = \frac{10^9 \times n}{f(BCLK)} - 35 \text{ [ns]} \text{ (if external bus cycle is } a\phi + b\phi, n = a + b)$$

$$tac2(RD-DB) = \frac{10^9 \times m}{f(BCLK) \times 2} - 35 \text{ [ns]} \text{ (if external bus cycle is } a\phi + b\phi, m = (b \times 2) - 1)$$

$$tac2(AD-DB) = \frac{10^9 \times p}{f(BCLK) \times 2} - 35 \text{ [ns]} \text{ (if external bus cycle is } a\phi + b\phi, p = \{(a + b - 1) \times 2\} + 1)$$

$$VCC1 = VCC2 = 3.3 \text{ V}$$

Table 5.32 Electrical Characteristics (2/3)

(VCC1 = VCC2 = 3.0 to 3.6 V, VSS = 0 V, Topr = -20 to 85°C, f(CPU) = 24 MHz unless otherwise specified)

Symbol	Parameter		Measurement Condition	Standard			Unit
				Min.	Typ.	Max.	
IIH	Input high "H" current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7 ⁽¹⁾ , XIN, RESET, CNVSS, BYTE	VI = 3 V			4.0	μA
IIL	Input low "L" current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7 ⁽¹⁾ , XIN, RESET, CNVSS, BYTE	VI = 0V			-4.0	μA
RPULLUP	Pull-up resistance	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7 ⁽¹⁾	VI=0V	40	90	500	kΩ
RfXIN	Feedback resistance	XIN			3.0		MΩ
RfXCIN	Feedback resistance	XCIN			20.0		MΩ
VRAM	RAM data retention voltage	In stop mode		2.0			V

NOTE:

1. P11 to P15 are provided in the 144-pin package only.

$$VCC1 = VCC2 = 3.3 \text{ V}$$

Timing Requirements

(VCC1 = VCC2 = 3.0 to 3.6 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.41 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(UP)	TAiOUT input cycle time	2000		ns
tw(UPH)	TAiOUT input high ("H") pulse width	1000		ns
tw(UPL)	TAiOUT input low ("L") pulse width	1000		ns
tsu(UP-TIN)	TAiOUT input setup time	400		ns
th(TIN-UP)	TAiOUT input hold time	400		ns

i = 0 to 4

Table 5.42 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	2		μs
tsu(TAIN-TAOUT)	TAiOUT input setup time	500		ns
tsu(TAOUT-TAIN)	TAiIN input setup time	500		ns

i = 0 to 4

Table 5.43 Timer B Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TB)	TBiIN input cycle time (counted on one edge)	100		ns
tw(TBH)	TBiIN input high ("H") pulse width (counted on one edge)	40		ns
tw(TBL)	TBiIN input low ("L") pulse width (counted on one edge)	40		ns
tc(TB)	TBiIN input cycle time (counted on both edges)	200		ns
tw(TBH)	TBiIN input high ("H") pulse width (counted on both edges)	80		ns
tw(TBL)	TBiIN input low ("L") pulse width (counted on both edges)	80		ns

i = 0 to 5

Table 5.44 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TB)	TBiIN input cycle time	400		ns
tw(TBH)	TBiIN input high ("H") pulse width	200		ns
tw(TBL)	TBiIN input low ("L") pulse width	200		ns

i = 0 to 5

Table 5.45 Timer B Input (Pulse Width Measurement Mode)

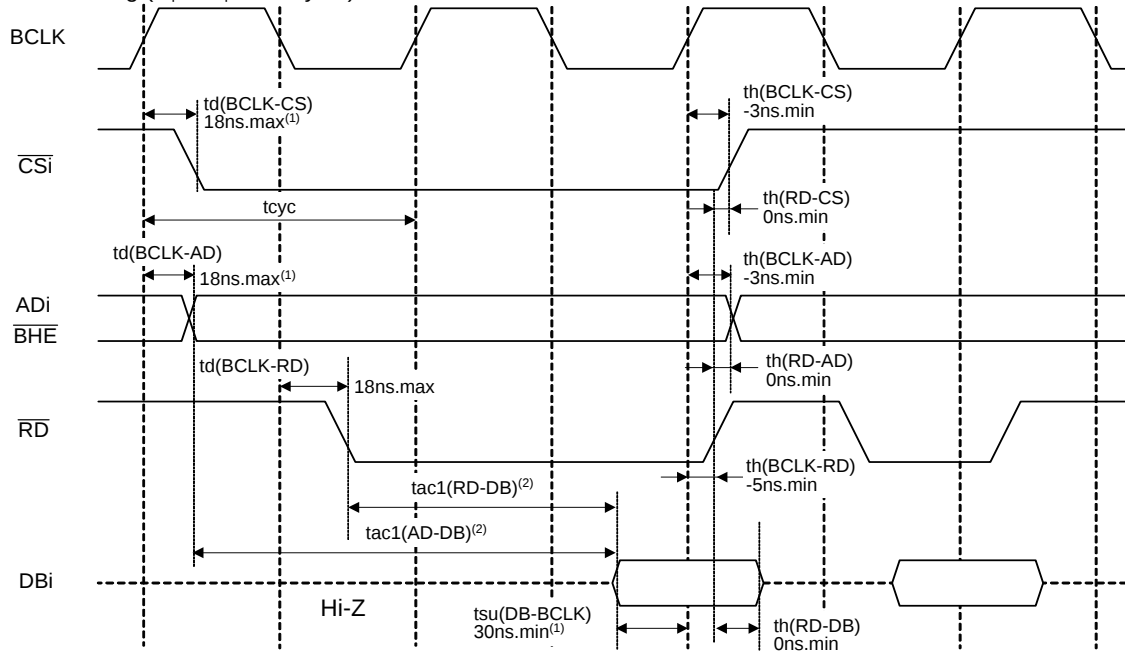
Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TB)	TBiIN input cycle time	400		ns
tw(TBH)	TBiIN input high ("H") pulse width	200		ns
tw(TBL)	TBiIN input low ("L") pulse width	200		ns

i = 0 to 5

Memory Expansion Mode and Microprocessor Mode (when accessing an external memory space)

VCC1=VCC2=3.3V

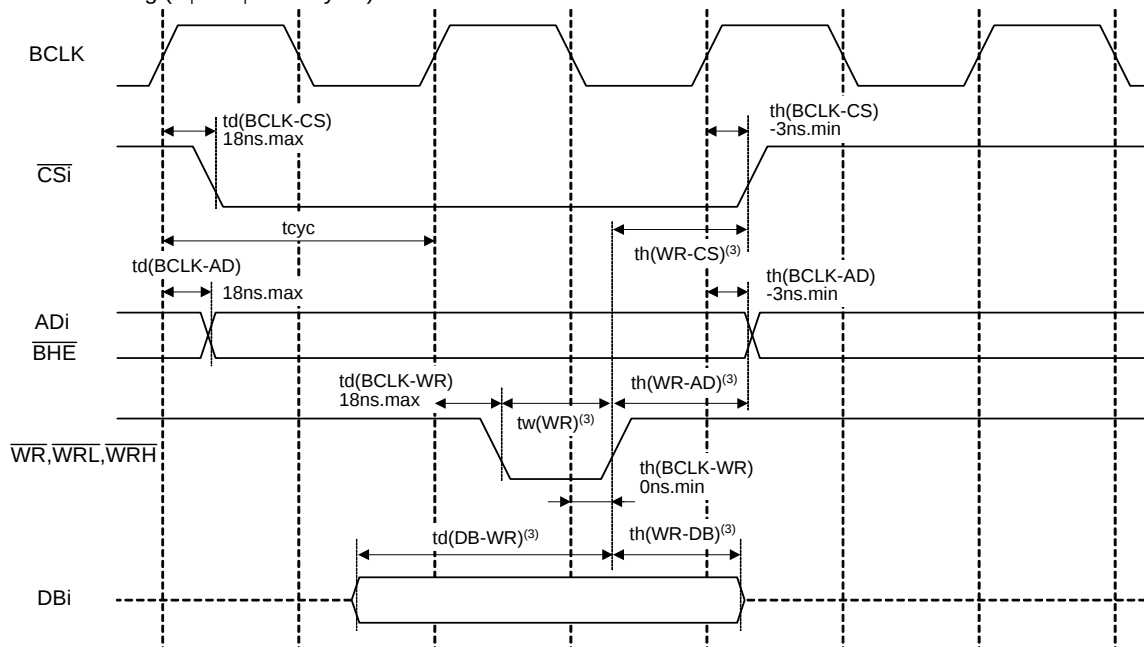
Read Timing (1φ + 1φ Bus Cycle)



NOTES:

- Values guaranteed only when the MCU is used stand-alone.
A maximum of 35 ns is guaranteed for $td(BCLK-AD) + tsu(DB-BCLK)$.
- Varies with operation frequency:
 $tac1(RD-DB) = (tcyc / 2 \times m - 35) \text{ ns.max}$ (if external bus cycle $a\phi + b\phi$, $m = (b \times 2) + 1$)
 $tac1(AD-DB) = (tcyc \times n - 35) \text{ ns.max}$ (if external bus cycle $a\phi + b\phi$, $n = a + b$)

Write Timing (1φ + 1φ Bus Cycle)



NOTES:

- Varies with operation frequency:
 $td(DB-WR) = (tcyc \times m - 20) \text{ ns.min}$ (if external bus cycle $a\phi + b\phi$, $m = b$)
 $th(WR-DB) = (tcyc / 2 - 20) \text{ ns.min}$
 $th(WR-AD) = (tcyc / 2 - 15) \text{ ns.min}$
 $th(WR-CS) = (tcyc / 2 - 10) \text{ ns.min}$
 $tw(WR) = (tcyc / 2 \times n - 15) \text{ ns.min}$ (if external bus cycle $a\phi + b\phi$, $n = (b \times 2) - 1$)

Measurement Conditions:

- VCC1 = VCC2 = 3.0 to 3.6 V
- Input high and low voltage: $V_{IH} = 1.5 \text{ V}$, $V_{IL} = 0.5 \text{ V}$
- Output high and low voltage: $V_{OH} = 1.5 \text{ V}$, $V_{OL} = 1.5 \text{ V}$

$$tcyc = \frac{10^9}{f(BCLK)}$$

Figure 5.9 VCC1 = VCC2 = 3.3 V Timing Diagram (3/4)

REVISION HISTORY		M32C/87 Group Datasheet	
Rev.	Date	Description	
		Page	Summary
		46	Special Function Registers (SFRs) • Table 4.20 A value of After Reset column in 03FFh modified

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