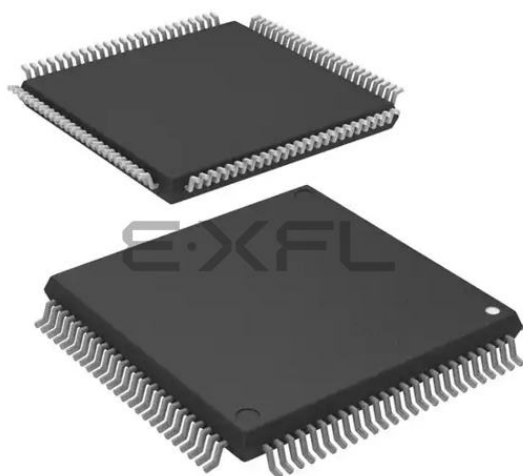




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Details

Product Status	Not For New Designs
Core Processor	M32C/80
Core Size	16/32-Bit
Speed	32MHz
Connectivity	CANbus, EBI/EMI, I ² C, IEBus, IrDA, SIO, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	85
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	31K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30876fjagp-u5

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Table 1.4 Specifications (100-Pin Package) (2/2)

Item	Function	Specification
Serial Interface	UART0 to UART4	Clock synchronous/asynchronous × 5 I ² C bus, special mode 2, GCI mode, SIM mode, IrDA mode ⁽²⁾ , IEBus (optional) ⁽¹⁾⁽³⁾
	UART5	Clock synchronous/asynchronous × 1
A/D Converter		10-bit resolution × 26 channels (in single-chip mode) 10-bit resolution × 10 channels (in memory expansion mode and microprocessor mode) Including sample and hold function
D/A Converter		8-bit resolution × 2 channels
CRC Calculation Circuit		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) compliant
X/Y Converter		16 bits × 16 bits
Intelligent I/O		16-bit timer × 2 • Time measurement function (input capture): 8 channels • Waveform generation function (output compare): 10 channels • Communication function: Clock synchronous mode, clock asynchronous mode, HDLC data processing mode, IEBus (optional) ⁽¹⁾⁽³⁾ • 2-phase pulse signal processing (2-phase encoder input) × 1
ROM Correction Function		Address match interrupt × 8
CAN modules		Supporting CAN 2.0B specification M32C/87: 16 slots × 2 channels, M32C/87A: 16 slots × 1 channel M32C/87B: none
I/O Ports	Programmable I/O ports	• Input only: 1 • CMOS I/O: 85, selectable pull-up resistor • N channel open drain ports: 2
Flash Memory		• Erase and program voltage: 3.3 V ± 0.3 V or 5.0 V ± 0.5 V • Erase and program endurance: 100 times (all areas) • Program security: ROM code protect and ID code check • Debug functions: On-chip debug and on-board flash reprogram
Operating Frequency/Supply Voltage		32 MHz: VCC1 = 4.2 to 5.5 V, VCC2 = 3.0 V to VCC1 24 MHz: VCC1 = 3.0 to 5.5 V, VCC2 = 3.0 V to VCC1
Current Consumption		32 mA (32 MHz, VCC1 = VCC2 = 5 V) 23 mA (24 MHz, VCC1 = VCC2 = 3.3 V) 45 μA (approx. 1 MHz, VCC1 = VCC2 = 3.3 V, on-chip oscillator low-power consumption mode → wait mode) 0.8 μA (VCC1 = VCC2 = 3.3 V, stop mode)
Operating Ambient Temperature (°C)		-20 to 85°C, -40 to 85°C (optional) ⁽³⁾
Package		100-pin LQFP (PLQP0100KB-A) 100-pin QFP (PRQP0100JB-A)

NOTES:

1. IEBus is a registered trademark of NEC Electronics Corporation.
2. Available in UART0.
3. Please contact a Renesas sales office for optional features.

Table 1.8 144-Pin Package List of Pin Names (1/4)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin ⁽¹⁾	Intelligent I/O Pin	Analog Pin	Bus Control Pin
1		P9_6			TXD4/SDA4/SRXD4/ CAN1OUT		ANEX1	
2		P9_5			CLK4/CAN1IN/ $\overline{\text{CAN1WU}}$		ANEX0	
3		P9_4		TB4IN	CTS4/RTS4/SS4		DA1	
4		P9_3		TB3IN	$\overline{\text{CTS3/RTS3/SS3}}$		DA0	
5		P9_2		TB2IN	TXD3/SDA3/SRXD3	OUTC2_0/IEOUT/ISTXD2		
6		P9_1		TB1IN	RXD3/SCL3/STXD3	IEIN/ISRXD2		
7		P9_0		TB0IN	CLK3			
8		P14_6	$\overline{\text{INT8}}$					
9		P14_5	$\overline{\text{INT7}}$					
10		P14_4	$\overline{\text{INT6}}$					
11		P14_3				INPC1_7/OUTC1_7		
12		P14_2				INPC1_6/OUTC1_6		
13		P14_1				INPC1_5/OUTC1_5		
14		P14_0				INPC1_4/OUTC1_4		
15	BYTE							
16	CNVSS							
17	XCIN	P8_7						
18	XCOUT	P8_6						
19	$\overline{\text{RESET}}$							
20	XOUT							
21	VSS							
22	XIN							
23	VCC1							
24		P8_5	$\overline{\text{NMI}}$					
25		P8_4	$\overline{\text{INT2}}$					
26		P8_3	$\overline{\text{INT1}}$		CAN0IN/CAN1IN			
27		P8_2	$\overline{\text{INT0}}$		CAN0OUT/CAN1OUT			
28		P8_1		TA4IN/ $\overline{\text{U}}$ /RTP2_3	$\overline{\text{CTS5/RTS5}}$	INPC1_5/OUTC1_5		
29		P8_0		TA4OUT/U	RXD5	ISRXD0		
30		P7_7		TA3IN/RTP2_2	CLK5/CAN0IN	INPC1_4/OUTC1_4/ ISCLK0		
31		P7_6		TA3OUT	TXD5/CAN0OUT	INPC1_3/OUTC1_3/ ISTXD0		
32		P7_5		TA2IN/ $\overline{\text{W}}$ /RTP2_1		INPC1_2/OUTC1_2/ ISRXD1		
33		P7_4		TA2OUT/ $\overline{\text{W}}$ / RTP2_0		INPC1_1/OUTC1_1/ ISCLK1		
34		P7_3		TA1IN/ $\overline{\text{V}}$	$\overline{\text{CTS2/RTS2/SS2}}$	INPC1_0/OUTC1_0/ ISTXD1		
35		P7_2		TA1OUT/V	CLK2			
36		P7_1		TA0IN/TB5IN/ RTP0_3	RXD2/SCL2/STXD2	INPC1_7/OUTC1_7/ OUTC2_2/ISRXD2/IEIN		
37		P7_0		TA0OUT/RTP0_2	TXD2/SDA2/SRXD2	INPC1_6/OUTC1_6/ OUTC2_0/ISTXD2/IEOUT		
38		P6_7			TXD1/SDA1/SRXD1			
39	VCC1							
40		P6_6			RXD1/SCL1/STXD1			

NOTE:

1. The CAN pins cannot be used in M32C/87B. Only CAN0 pins can be used in M32C/87A.

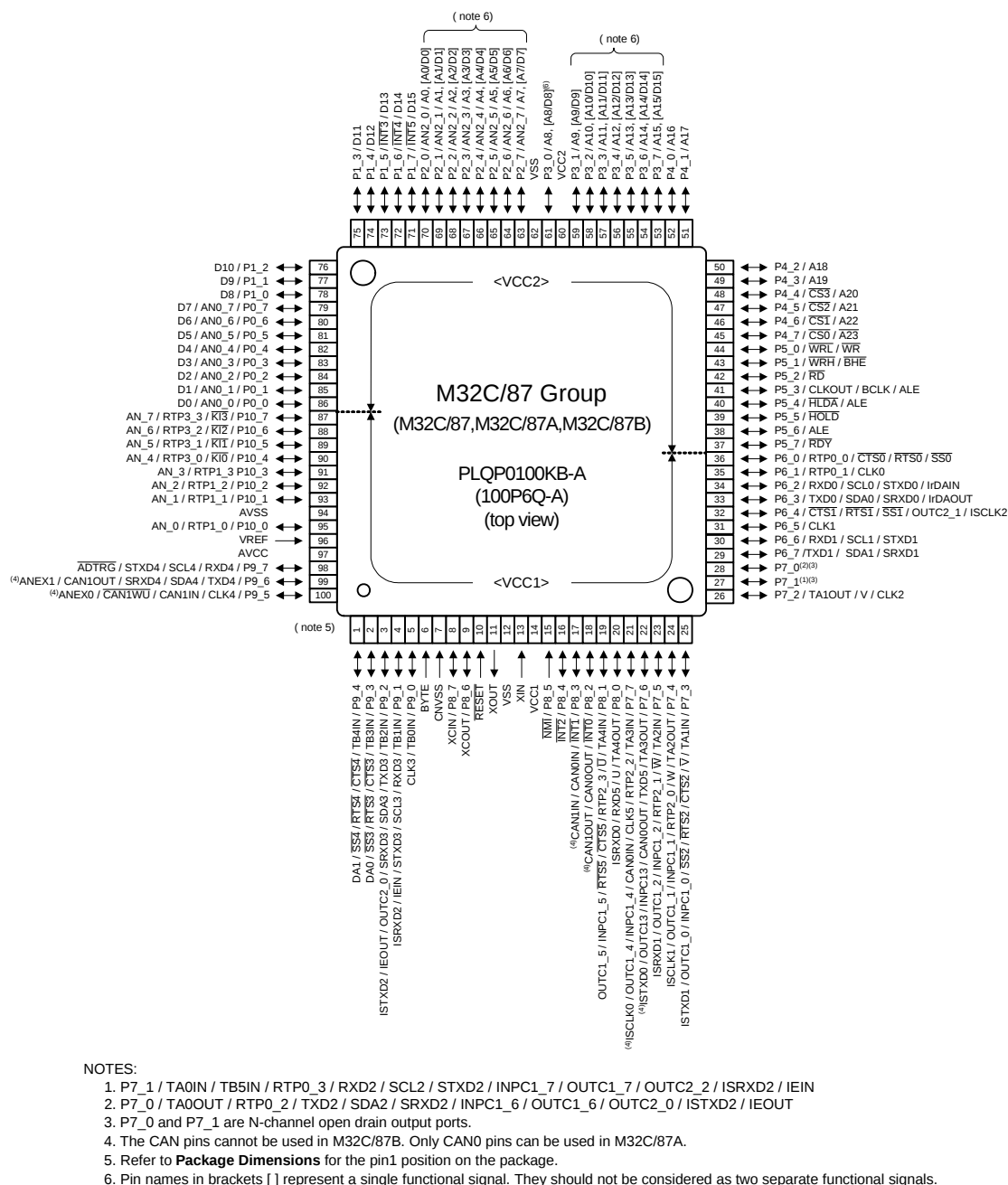


Figure 1.5 Pin Assignment for 100-Pin Package

Table 1.12 100-Pin Package List of Pin Names (1/3)

Pin No.		Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin ⁽¹⁾	Intelligent I/O Pin	Analog Pin	Bus Control Pin
FP	GP								
1	99		P9_6			TXD4/SDA4/SRXD4/ CAN1OUT		ANEX1	
2	100		P9_5			CLK4/CAN1IN/ CAN1WU		ANEX0	
3	1		P9_4		TB4IN	CTS4/RTS4/SS4		DA1	
4	2		P9_3		TB3IN	CTS3/RTS3/SS3		DA0	
5	3		P9_2		TB2IN	TXD3/SDA3/SRXD3	OUTC2_0/IEOUT/ISTXD2		
6	4		P9_1		TB1IN	RXD3/SCL3/STXD3	IEIN/ISRXD2		
7	5		P9_0		TB0IN	CLK3			
8	6	BYTE							
9	7	CNVSS							
10	8	XCIN	P8_7						
11	9	XCOUT	P8_6						
12	10	RESET							
13	11	XOUT							
14	12	VSS							
15	13	XIN							
16	14	VCC1							
17	15		P8_5	NMI					
18	16		P8_4	INT2					
19	17		P8_3	INT1		CAN0IN/CAN1IN			
20	18		P8_2	INT0		CAN0OUT/CAN1OUT			
21	19		P8_1		TA4IN/ $\bar{U}$ /RTP2_3	CTS5/RTS5	INPC1_5/OUTC1_5		
22	20		P8_0		TA4OUT/ $\bar{U}$	RXD5	ISRXD0		
23	21		P7_7		TA3IN/RTP2_2	CLK5/CAN0IN	INPC1_4/OUTC1_4/ ISCLK0		
24	22		P7_6		TA3OUT	TXD5/CAN0OUT	INPC1_3/OUTC1_3/ ISTXD0		
25	23		P7_5		TA2IN/ $\bar{W}$ /RTP2_1		INPC1_2/OUTC1_2 ISRXD1		
26	24		P7_4		TA2OUT/ $\bar{W}$ / RTP2_0		INPC1_1/OUTC1_1/ ISCLK1		
27	25		P7_3		TA1IN/ $\bar{V}$	CTS2/RTS2/SS2	INPC1_0/OUTC1_0/ ISTXD1		
28	26		P7_2		TA1OUT/ $\bar{V}$	CLK2			
29	27		P7_1		TA0IN/TB5IN/ RTP0_3	RXD2/SCL2/STXD2	INPC1_7/OUTC1_7/ OUTC2_2/ISRXD2/IEIN		
30	28		P7_0		TA0OUT/RTP0_2	TXD2/SDA2/SRXD2	INPC1_6/OUTC1_6/ OUTC2_0/ISTXD2/IEOUT		
31	29		P6_7			TXD1/SDA1/SRXD1			
32	30		P6_6			RXD1/SCL1/STXD1			
33	31		P6_5			CLK1			
34	32		P6_4			CTS1/RTS1/SS1	OUTC2_1/ISCLK2		
35	33		P6_3			TXD0/SDA0/SRXD0/ IrDAOUT			
36	34		P6_2			RXD0/SCL0/STXD0/ IrDAIN			
37	35		P6_1		RTP0_1	CLK0			
38	36		P6_0		RTP0_0	CTS0/RTS0/SS0			
39	37		P5_7						$\bar{RDY}$
40	38		P5_6						ALE

NOTE:

1. The CAN pins cannot be used in M32C/87B. Only CAN0 pins can be used in M32C/87A.

Table 1.14 100-Pin Package List of Pin Names (3/3)

Pin No.		Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
FP	GP								
73	71		P1_7	INT5					D15
74	72		P1_6	INT4					D14
75	73		P1_5	INT3					D13
76	74		P1_4						D12
77	75		P1_3						D11
78	76		P1_2						D10
79	77		P1_1						D9
80	78		P1_0						D8
81	79		P0_7					AN0_7	D7
82	80		P0_6					AN0_6	D6
83	81		P0_5					AN0_5	D5
84	82		P0_4					AN0_4	D4
85	83		P0_3					AN0_3	D3
86	84		P0_2					AN0_2	D2
87	85		P0_1					AN0_1	D1
88	86		P0_0					AN0_0	D0
89	87		P10_7	KI3	RTP3_3			AN_7	
90	88		P10_6	KI2	RTP3_2			AN_6	
91	89		P10_5	KI1	RTP3_1			AN_5	
92	90		P10_4	KI0	RTP3_0			AN_4	
93	91		P10_3		RTP1_3			AN_3	
94	92		P10_2		RTP1_2			AN_2	
95	93		P10_1		RTP1_1			AN_1	
96	94	AVSS							
97	95		P10_0		RTP1_0			AN_0	
98	96	VREF							
99	97	AVCC							
100	98		P9_7			RXD4/SCL4/STXD4		ADTRG	

2.1 General Registers

2.1.1 Data Registers (R0, R1, R2, and R3)

R0, R1, R2, and R3 are 16-bit registers for transfer, arithmetic and logic operations. R0 and R1 can be split into high-order (R0H/R1H) and low-order bits (R0L/R1L) to be used separately as 8-bit data registers. R0 can be combined with R2 and used as a 32-bit data register (R2R0). The same applies to R3R1.

2.1.2 Address Registers (A0 and A1)

A0 and A1 are 24-bit registers used for A0-/A1-indirect addressing, A0-/A1-relative addressing, transfer, arithmetic and logic operations.

2.1.3 Static Base Register (SB)

SB is a 24-bit register used for SB-relative addressing.

2.1.4 Frame Base Register (FB)

FB is a 24-bit register used for FB-relative addressing.

2.1.5 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are 24 bits wide each. The U flag is used to switch between USP and ISP. Refer to **2.1.8 Flag Register (FLG)** for details on the U flag. Set USP and ISP to even addresses to execute an interrupt sequence efficiently.

2.1.6 Interrupt Table Register (INTB)

INTB is a 24-bit register indicating the starting address of a relocatable interrupt vector table.

2.1.7 Program Counter (PC)

PC is 24 bits wide and indicates the address of the next instruction to be executed.

2.1.8 Flag Register (FLG)

FLG is a 16-bit register indicating the CPU state.

2.1.8.1 Carry Flag (C)

The C flag indicates whether or not carry or borrow has been generated after executing an instruction.

2.1.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.1.8.3 Zero Flag (Z)

The Z flag becomes 1 when an arithmetic operation results in 0; otherwise becomes 0.

2.1.8.4 Sign Flag (S)

The S flag becomes 1 when an arithmetic operation results in a negative value; otherwise becomes 0.

2.1.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is set to 0. Register bank 1 is selected when this flag is set to 1.

2.1.8.6 Overflow Flag (O)

The O flag becomes 1 when an arithmetic operation results in an overflow; otherwise becomes 0.

Table 4.2 SFR Address Map (2/20)

Address	Register	Symbol	After Reset
0030h			
0031h			
0032h			
0033h			
0034h			
0035h			
0036h			
0037h			
0038h	Address Match Interrupt Register 6	RMAD6	000000h
0039h			
003Ah			
003Bh	Address Match Interrupt Register 7	RMAD7	000000h
003Ch			
003Dh			
003Eh			
003Fh			
0040h			
0041h			
0042h			
0043h			
0044h			
0045h			
0046h			
0047h			
0048h	External Space Wait Control Register 0	EWCR0	X0X0 0011b
0049h	External Space Wait Control Register 1	EWCR1	X0X0 0011b
004Ah	External Space Wait Control Register 2	EWCR2	X0X0 0011b
004Bh	External Space Wait Control Register 3	EWCR3	X0X0 0011b
004Ch			
004Dh			
004Eh			
004Fh			
0050h			
0051h			
0052h			
0053h			
0054h			
0055h	Flash Memory Control Register 1	FMR1	0000 0X0Xb
0056h			
0057h	Flash Memory Control Register 0	FMR0	0000 0001b(Flash Memory) XXXX XXX0b(Mask ROM)
0058h			
0059h			
005Ah			
005Bh			
005Ch			
005Dh			
005Eh			
005Fh			

X: Undefined

Blank spaces are all reserved. No access is allowed.

Table 4.3 SFR Address Map (3/20)

Address	Register	Symbol	After Reset
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h	DMA0 Interrupt Control Register	DM0IC	XXXX X000b
0069h	Timer B5 Interrupt Control Register	TB5IC	XXXX X000b
006Ah	DMA2 Interrupt Control Register	DM2IC	XXXX X000b
006Bh	UART2 Receive/ACK Interrupt Control Register	S2RIC	XXXX X000b
006Ch	Timer A0 Interrupt Control Register	TA0IC	XXXX X000b
006Dh	UART3 Receive/ACK Interrupt Control Register	S3RIC	XXXX X000b
006Eh	Timer A2 Interrupt Control Register	TA2IC	XXXX X000b
006Fh	UART4 Receive/ACK Interrupt Control Register	S4RIC	XXXX X000b
0070h	Timer A4 Interrupt Control Register	TA4IC	XXXX X000b
0071h	UART0/UART3 Bus Conflict Detection Interrupt Control Register	BCN0IC/BCN3IC	XXXX X000b
0072h	UART0 Receive/ACK Interrupt Control Register	S0RIC	XXXX X000b
0073h	A/D0 Conversion Interrupt Control Register	AD0IC	XXXX X000b
0074h	UART1 Receive/ACK Interrupt Control Register	S1RIC	XXXX X000b
0075h	I/O Interrupt Control Register 0 / CAN1 interrupt Control Register 0	IIO0IC/CAN3IC	XXXX X000b
0076h	Timer B1 Interrupt Control Register	TB1IC	XXXX X000b
0077h	I/O Interrupt Control Register 2	IIO2IC	XXXX X000b
0078h	Timer B3 Interrupt Control Register	TB3IC	XXXX X000b
0079h	I/O Interrupt Control Register 4	IIO4IC	XXXX X000b
007Ah	INT5 Interrupt Control Register	INT5IC	XX00 X000b
007Bh	I/O Interrupt Control Register 6	IIO6IC	XXXX X000b
007Ch	INT3 Interrupt Control Register	INT3IC	XX00 X000b
007Dh	I/O Interrupt Control Register 8	IIO8IC	XXXX X000b
007Eh	INT1 Interrupt Control Register	INT1IC	XX00 X000b
007Fh	I/O Interrupt Control Register 10 / CAN0 Interrupt Control Register 1	IIO10IC/CAN1IC	XXXX X000b
0080h			
0081h	I/O Interrupt Control Register 11 / CAN0 Interrupt Control Register 2	IIO11IC/CAN2IC	XXXX X000b
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h	DMA1 Interrupt Control Register	DM1IC	XXXX X000b
0089h	UART2 Transmit/NACK Interrupt Control Register	S2TIC	XXXX X000b
008Ah	DMA3 Interrupt Control Register	DM3IC	XXXX X000b
008Bh	UART3 Transmit/NACK Interrupt Control Register	S3TIC	XXXX X000b
008Ch	Timer A1 Interrupt Control Register	TA1IC	XXXX X000b
008Dh	UART4 Transmit/NACK Interrupt Control Register	S4TIC	XXXX X000b
008Eh	Timer A3 Interrupt Control Register	TA3IC	XXXX X000b
008Fh	UART2 Bus Conflict Detection Interrupt Control Register	BCN2IC	XXXX X000b

X: Undefined

Blank spaces are all reserved. No access is allowed.

Table 4.8 SFR Address Map (8/20)

Address	Register	Symbol	After Reset
01C0h	UART5 Transmit/Receive Mode Register	U5MR	00h
01C1h	UART5 Baud Rate Register	U5BRG	XXh
01C2h	UART5 Transmit Buffer Register	U5TB	XXXXh
01C3h			
01C4h	UART5 Transmit/Receive Control Register 0	U5C0	0000 1000b
01C5h	UART5 Transmit/Receive Control Register 1	U5C1	XXXX 0010b
01C6h	UART5 Receive Buffer Register	U5RB	XXXXh
01C7h			
01C8h	UART6 Transmit/Receive Mode Register	U6MR	00h
01C9h	UART6 Baud Rate Register	U6BRG	XXh
01CAh	UART6 Transmit Buffer Register	U6TB	XXXXh
01CBh			
01CCh	UART6 Transmit/Receive Control Register 0	U6C0	0000 1000b
01CDh	UART6 Transmit/Receive Control Register 1	U6C1	XXXX 0010b
01CEh	UART6 Receive Buffer Register	U6RB	XXXXh
01CFh			
01D0h	UART5, UART6 Transmit/Receive Control Register	U56CON	X000 0000b
01D1h	UART5, UART6 Input Pin Function Select Register	U56IS	X000 X000b
01D2h			
01D3h			
01D4h			
01D5h			
01D6h			
01D7h			
01D8h	RTP Output Buffer Register 0	RTP0R	XXh
01D9h	RTP Output Buffer Register 1	RTP1R	XXh
01DAh	RTP Output Buffer Register 2	RTP2R	XXh
01DBh	RTP Output Buffer Register 3	RTP3R	XXh
01DCh			
01DDh			
01DEh			
01DFh			
01E0h	CAN0 Message Slot Buffer 0 Standard ID0 ⁽¹⁾⁽²⁾	C0SLOT0_0	XXh
01E1h	CAN0 Message Slot Buffer 0 Standard ID1 ⁽¹⁾⁽²⁾	C0SLOT0_1	XXh
01E2h	CAN0 Message Slot Buffer 0 Extended ID0 ⁽¹⁾⁽²⁾	C0SLOT0_2	XXh
01E3h	CAN0 Message Slot Buffer 0 Extended ID1 ⁽¹⁾⁽²⁾	C0SLOT0_3	XXh
01E4h	CAN0 Message Slot Buffer 0 Extended ID2 ⁽¹⁾⁽²⁾	C0SLOT0_4	XXh
01E5h	CAN0 Message Slot Buffer 0 Data Length Code ⁽¹⁾⁽²⁾	C0SLOT0_5	XXh
01E6h	CAN0 Message Slot Buffer 0 Data 0 ⁽¹⁾⁽²⁾	C0SLOT0_6	XXh
01E7h	CAN0 Message Slot Buffer 0 Data 1 ⁽¹⁾⁽²⁾	C0SLOT0_7	XXh
01E8h	CAN0 Message Slot Buffer 0 Data 2 ⁽¹⁾⁽²⁾	C0SLOT0_8	XXh
01E9h	CAN0 Message Slot Buffer 0 Data 3 ⁽¹⁾⁽²⁾	C0SLOT0_9	XXh
01EAh	CAN0 Message Slot Buffer 0 Data 4 ⁽¹⁾⁽²⁾	C0SLOT0_10	XXh
01EBh	CAN0 Message Slot Buffer 0 Data 5 ⁽¹⁾⁽²⁾	C0SLOT0_11	XXh
01ECh	CAN0 Message Slot Buffer 0 Data 6 ⁽¹⁾⁽²⁾	C0SLOT0_12	XXh
01EDh	CAN0 Message Slot Buffer 0 Data 7 ⁽¹⁾⁽²⁾	C0SLOT0_13	XXh
01EEh	CAN0 Message Slot Buffer 0 Time Stamp High-Order ⁽¹⁾⁽²⁾	C0SLOT0_14	XXh
01EFh	CAN0 Message Slot Buffer 0 Time Stamp Low-Order ⁽¹⁾⁽²⁾	C0SLOT0_15	XXh

X: Undefined

Blank spaces are all reserved. No access is allowed.

NOTES:

1. The CAN-associated registers (allocated in addresses 01E0h to 02BFh) cannot be used in M32C/87B. In M32C/87A, only CAN0-associated registers can be used.
2. Set the PM13 bit in the PM1 register to 1 (2 wait states for SFR area) before accessing the CAN-associated registers.

Table 4.13 SFR Address Map (13/20)

Address	Register ⁽³⁾⁽⁴⁾	Symbol	After Reset
02B0h	CAN1 Message Slot 0 Control Register / CAN1 Local Mask Register A Standard ID0	C1MCTL0 / C1LMAR0	0000 0000b ⁽¹⁾⁽²⁾ / XXX0 0000b ⁽¹⁾⁽²⁾
02B1h	CAN1 Message Slot 1 Control Register / CAN1 Local Mask Register A Standard ID1	C1MCTL1 / C1LMAR1	0000 0000b ⁽¹⁾⁽²⁾ / XX00 0000b ⁽¹⁾⁽²⁾
02B2h	CAN1 Message Slot 2 Control Register / CAN1 Local Mask Register A Extended ID0	C1MCTL2 / C1LMAR2	0000 0000b ⁽¹⁾⁽²⁾ / XXXX 0000b ⁽¹⁾⁽²⁾
02B3h	CAN1 Message Slot 3 Control Register / CAN1 Local Mask Register A Extended ID1	C1MCTL3 / C1LMAR3	00h ⁽¹⁾⁽²⁾ / 00h ⁽¹⁾⁽²⁾
02B4h	CAN1 Message Slot 4 Control Register / CAN1 Local Mask Register A Extended ID2	C1MCTL4 / C1LMAR4	0000 0000b ⁽¹⁾⁽²⁾ / XX00 0000b ⁽¹⁾⁽²⁾
02B5h	CAN1 Message Slot 5 Control Register	C1MCTL5	00h ⁽¹⁾⁽²⁾
02B6h	CAN1 Message Slot 6 Control Register	C1MCTL6	00h ⁽¹⁾⁽²⁾
02B7h	CAN1 Message Slot 7 Control Register	C1MCTL7	00h ⁽¹⁾⁽²⁾
02B8h	CAN1 Message Slot 8 Control Register / CAN1 Local Mask Register B Standard ID0	C1MCTL8 / C1LMBR0	0000 0000b ⁽¹⁾⁽²⁾ / XXX0 0000b ⁽¹⁾⁽²⁾
02B9h	CAN1 Message Slot 9 Control Register / CAN1 Local Mask Register B Standard ID1	C1MCTL9 / C1LMBR1	0000 0000b ⁽¹⁾⁽²⁾ / XX00 0000b ⁽¹⁾⁽²⁾
02BAh	CAN1 Message Slot 10 Control Register / CAN1 Local Mask Register B Extended ID0	C1MCTL10 / C1LMBR2	0000 0000b ⁽¹⁾⁽²⁾ / XXXX 0000b ⁽¹⁾⁽²⁾
02BBh	CAN1 Message Slot 11 Control Register / CAN1 Local Mask Register B Extended ID1	C1MCTL11 / C1LMBR3	00h ⁽¹⁾⁽²⁾ / 00h ⁽¹⁾⁽²⁾
02BCh	CAN1 Message Slot 12 Control Register / CAN1 Local Mask Register B Extended ID2	C1MCTL12 / C1LMBR4	0000 0000b ⁽¹⁾⁽²⁾ / XX00 0000b ⁽¹⁾⁽²⁾
02BDh	CAN1 Message Slot 13 Control Register	C1MCTL13	00h ⁽¹⁾⁽²⁾
02BEh	CAN1 Message Slot 14 Control Register	C1MCTL14	00h ⁽¹⁾⁽²⁾
02BFh	CAN1 Message Slot 15 Control Register	C1MCTL15	00h ⁽¹⁾⁽²⁾

X: Undefined

Blank spaces are all reserved. No access is allowed.

NOTES:

1. The BANKSEL bit in the C1CTLR1 register can switch functions for addresses 02A0h to 02BFh.
2. Values are obtained by setting the SLEEP bit in the C1SLPR register to "1" (sleep mode exited) after reset and supplying a clock to the CAN module.
3. The CAN-associated registers (allocated in addresses 01E0h to 02BFh) cannot be used in M32C/87B. In M32C/87A, only CAN0-associated registers can be used.
4. Set the PM13 bit in the PM1 register to 1 (2 wait states for SFR area) before accessing the CAN-associated registers.

Table 5.2 Recommended Operating Conditions (1/3)
(VCC1 = VCC2 = 3.0 to 5.5 V, Topr = -20 to 85°C unless otherwise specified)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
VCC1, VCC2	Supply voltage (VCC1 ≥ VCC2)		3.0	5.0	5.5	V
AVCC	Analog supply voltage			VCC1		V
VSS	Supply voltage			0		V
AVSS	Analog supply voltage			0		V
VIH	Input high "H" voltage	P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7 ⁽²⁾	0.8VCC2		VCC2	V
		P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7 ⁽¹⁾ , P9_0 to P9_7, P10_0 to P10_7, P14_0 to P14_6, P15_0 to P15_7 ⁽²⁾ , XIN, RESET, CNVSS, BYTE	0.8VCC1		VCC1	
		P7_0, P7_1	0.8VCC1		6.0	
		P0_0 to P0_7, P1_0 to P1_7 (in single-chip mode)	0.8VCC2		VCC2	
		P0_0 to P0_7, P1_0 to P1_7 (in memory expansion mode and microprocessor mode)	0.5VCC2		VCC2	
VIL	Input low "L" voltage	P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7 ⁽²⁾	0		0.2VCC2	V
		P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7 ⁽¹⁾ , P9_0 to P9_7, P10_0 to P10_7, P14_0 to P14_6, P15_0 to P15_7 ⁽²⁾ , XIN, RESET, CNVSS, BYTE	0		0.2VCC1	
		P0_0 to P0_7, P1_0 to P1_7 (in single-chip mode)	0		0.2VCC2	
		P0_0 to P0_7, P1_0 to P1_7 (in memory expansion mode and microprocessor mode)	0		0.16VCC2	

NOTES:

1. VIH and VIL reference for P8_7 apply when P8_7 is used as a programmable input port. It does not apply when P8_7 is used as XCIN.
2. P11 to P15 are provided in the 144-pin package only.

$$VCC1 = VCC2 = 5V$$

Table 5.8 A/D Conversion Characteristics

(VCC1 = VCC2 = AVCC = VREF = 4.2 to 5.5 V, VSS = AVSS = 0 V, Topr = -20 to 85°C, f(CPU) = 32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
–	Resolution	VREF = VCC1			10	Bits
INL	Integral nonlinearity error	VREF = VCC1 = VCC2 = 5 V			±3	LSB
		AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, AN15_0 to AN15_7, ANEX0, ANEX1 External op-amp connection mode			±7	LSB
DNL	Differential nonlinearity error				±1	LSB
–	Offset error				±3	LSB
–	Gain error				±3	LSB
RLADDER	Resistor ladder	VREF = VCC1	8		40	kΩ
tCONV	10-bit conversion time ⁽¹⁾⁽²⁾		2.06			μs
tCONV	8-bit conversion time ⁽¹⁾⁽²⁾		1.75			μs
tSAMP	Sampling time ⁽¹⁾		0.188			μs
VREF	Reference voltage		2		VCC1	V
VIA	Analog input voltage		0		VREF	V

NOTES:

1. The value is obtained when φAD frequency is at 16 MHz. Keep φAD frequency at 16 MHz or lower.
2. With using the sample and hold function

Table 5.9 D/A Conversion Characteristics

(VCC1 = VCC2 = VREF = 4.2 to 5.5 V, VSS = AVSS = 0 V, Topr = -20 to 85°C, f(CPU) = 32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
–	Resolution				8	Bits
–	Absolute accuracy				1.0	%
tsu	Setup time				3	μs
RO	Output resistance		4	10	20	kΩ
IVREF	Reference power supply input current	(note 1)			1.5	mA

NOTE:

1. Measured when one D/A converter is used, and the DAi register (i = 0, 1) of the unused D/A converter is set to 00h. The current flown into the resistor ladder in the A/D converter is excluded. IVREF flows even if the VCUT bit in the AD0CON1 register is set to 0 (VREF not connected)

$$VCC1 = VCC2 = 5V$$

**Table 5.10 Flash Memory Electrical Characteristics (VCC1 = 4.5 V to 5.5 V, 3.0 to 3.6 V,
Topr = 0 to 60°C unless otherwise specified)**

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
–	Erase and program endurance ⁽¹⁾		100			times
–	Word program time (16 bits) (VCC1 = 5.0 V, Topr = 25°C)			25	300	μs
–	Lock bit program time			25	300	μs
–	Block erase time (VCC1 = 5.0 V, Topr = 25°C)	4-Kbyte block		0.3	4	s
		8-Kbyte block		0.3	4	s
		32-Kbyte block		0.5	4	s
		64-Kbyte block		0.8	4	s
tps	Wait time to stabilize flash memory circuit				15	μs
–	Data hold time (Topr = -40 to 85°C)		10			years

NOTE:

1. If erase and program endurance is n times (n = 100), each block can be erased n times. For example, if a 4-Kbyte block A is erased after programming a word data 2,048 times, each to a different address, this counts as one erase and program time. Data can not be programmed to the same address more than once without erasing the block. (rewrite prohibited)

$$VCC1 = VCC2 = 5V$$

Timing Requirements

(VCC1 = VCC2 = 4.2 to 5.5 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.13 External Clock Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc	External clock input cycle time	31.25		ns
tw(H)	External clock input high ("H") pulse width	13.75		ns
tw(L)	External clock input low ("L") pulse width	13.75		ns
tr	External clock rise time		5	ns
tf	External clock fall time		5	ns

Table 5.14 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	100		ns
tw(TAH)	TAiIN input high ("H") pulse width	40		ns
tw(TAL)	TAiIN input low ("L") pulse width	40		ns

i = 0 to 4

Table 5.15 Timer A Input (Gate Signal Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	400		ns
tw(TAH)	TAiIN input high ("H") pulse width	200		ns
tw(TAL)	TAiIN input low ("L") pulse width	200		ns

i = 0 to 4

Table 5.16 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	200		ns
tw(TAH)	TAiIN input high ("H") pulse width	100		ns
tw(TAL)	TAiIN input low ("L") pulse width	100		ns

i = 0 to 4

Table 5.17 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tw(TAH)	TAiIN input high ("H") pulse width	100		ns
tw(TAL)	TAiIN input low ("L") pulse width	100		ns

i = 0 to 4

$$VCC1 = VCC2 = 3.3 \text{ V}$$

Timing Requirements

(VCC1 = VCC2 = 3.0 to 3.6 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.41 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(UP)	TAiOUT input cycle time	2000		ns
tw(UPH)	TAiOUT input high ("H") pulse width	1000		ns
tw(UPL)	TAiOUT input low ("L") pulse width	1000		ns
tsu(UP-TIN)	TAiOUT input setup time	400		ns
th(TIN-UP)	TAiOUT input hold time	400		ns

i = 0 to 4

Table 5.42 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	2		μs
tsu(TAIN-TAOUT)	TAiOUT input setup time	500		ns
tsu(TAOUT-TAIN)	TAiIN input setup time	500		ns

i = 0 to 4

Table 5.43 Timer B Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TB)	TBiIN input cycle time (counted on one edge)	100		ns
tw(TBH)	TBiIN input high ("H") pulse width (counted on one edge)	40		ns
tw(TBL)	TBiIN input low ("L") pulse width (counted on one edge)	40		ns
tc(TB)	TBiIN input cycle time (counted on both edges)	200		ns
tw(TBH)	TBiIN input high ("H") pulse width (counted on both edges)	80		ns
tw(TBL)	TBiIN input low ("L") pulse width (counted on both edges)	80		ns

i = 0 to 5

Table 5.44 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TB)	TBiIN input cycle time	400		ns
tw(TBH)	TBiIN input high ("H") pulse width	200		ns
tw(TBL)	TBiIN input low ("L") pulse width	200		ns

i = 0 to 5

Table 5.45 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TB)	TBiIN input cycle time	400		ns
tw(TBH)	TBiIN input high ("H") pulse width	200		ns
tw(TBL)	TBiIN input low ("L") pulse width	200		ns

i = 0 to 5

$$VCC1 = VCC2 = 3.3 \text{ V}$$

Switching Characteristics

(VCC1 = VCC2 = 3.0 to 3.6 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.53 Memory Expansion Mode and Microprocessor Mode (when accessing external memory space with multiplexed bus)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min.	Max.	
td(BCLK-AD)	Address output delay time	See Figure 5.2		18	ns
th(BCLK-AD)	Address output hold time (BCLK standard)		-3		ns
th(RD-AD)	Address output hold time (RD standard) ⁽⁵⁾		(note 1)		ns
th(WR-AD)	Address output hold time (WR standard) ⁽⁵⁾		(note 1)		ns
td(BCLK-CS)	Chip-select signal output delay time			18	ns
th(BCLK-CS)	Chip-select signal output hold time (BCLK standard)		-3		ns
th(RD-CS)	Chip-select signal output hold time (RD standard) ⁽⁵⁾		(note 1)		ns
th(WR-CS)	Chip-select signal output hold time (WR standard) ⁽⁵⁾		(note 1)		ns
td(BCLK-RD)	RD signal output delay time			18	ns
th(BCLK-RD)	RD signal output hold time		-5		ns
td(BCLK-WR)	WR signal output delay time			18	ns
th(BCLK-WR)	WR signal output hold time		0		ns
td(DB-WR)	Data output delay time (WR standard)		(note 2)		ns
th(WR-DB)	Data output hold time (WR standard) ⁽⁵⁾		(note 1)		ns
td(BCLK-ALE)	ALE signal output delay time (BCLK standard)			18	ns
th(BCLK-ALE)	ALE signal output hold time (BCLK standard)		-2		ns
td(AD-ALE)	ALE signal output delay time (address standard)		(note 3)		ns
th(ALE-AD)	ALE signal output hold time (address standard)		(note 4)		ns
tdz(RD-AD)	Address output float start time			8	ns

NOTES:

1. Values, which depend on BCLK frequency, can be obtained from the following equations.

$$th(RD-AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \text{ [ns]}$$

$$th(WR-AD) = \frac{10^9}{f(BCLK) \times 2} - 15 \text{ [ns]}$$

$$th(RD-CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \text{ [ns]}$$

$$th(WR-CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \text{ [ns]}$$

$$th(WR-DB) = \frac{10^9}{f(BCLK) \times 2} - 20 \text{ [ns]}$$

2. Values, which depend on BCLK frequency and external bus cycles, can be obtained from the following equation.

$$td(DB-WR) = \frac{10^9 \times m}{f(BCLK) \times 2} - 25 \text{ [ns]} \text{ (if external bus cycle is } a\phi + b\phi, m = (b \times 2) - 1)$$

3. Values, which depend on BCLK frequency and external bus cycles, can be obtained from the following equation.

$$td(AD-ALE) = \frac{10^9 \times n}{f(BCLK) \times 2} - 20 \text{ [ns]} \text{ (if external bus cycle is } a\phi + b\phi, n = a)$$

4. Values, which depend on BCLK frequency and external bus cycles, can be obtained from the following equation.

$$th(ALE-AD) = \frac{10^9 \times n}{f(BCLK) \times 2} - 20 \text{ [ns]} \text{ (if external bus cycle is } a\phi + b\phi, n = a)$$

5. tc [ns] is added when recovery cycle is inserted.

REVISION HISTORY	M32C/87 Group Datasheet
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Rev.	Date	Description	
		Page	Summary
0.50	Dec.16, 04	–	New Document
1.00	Jul.14, 05	–	M32C/87A and M32C/87B added
		–	Package code changed: 144P6Q-A to PLQP0144KA-A, 100P6Q-A to PLQP0100KB-A, 100P6S-A to PRQP0100JB-A
		–	“Low Voltage Detection Reset” changed to “Brown-out Detection Reset”
		2	Overview • Table 1.2 M32C/87 Group Performance (144-Pin Package) M32C/87A and M32C/87B performance added to the CAN module performance; Power Consumption performance released
		3	• Table 1.2 M32C/87 Group Performance (100-Pin Package) M32C/87A and M32C/87B performance added to the CAN module performance; Power Consumption performance released
		4	• Figure 1.1 M32C/87 Group Block Diagram Note 4 deleted; note 5 added
		7	• Figure 1.3 Pin Assignment for 144-Pin Package Note 15 added
		8	• Table 1.4 Pin Characteristics for 144-Pin Package Note 1 added
		11	• Figure 1.4 Pin Assignment for 100-Pin Package Note 19 added
		12	• Figure 1.5 Pin Assignment for 100-Pin Package Note 15 added
		13	• Table 1.5 Pin Characteristics for 100-Pin Package Note 1 added
		17	• Table 1.6 Pin Description Note 2 added
		22	Memory • Figure 3.1 Memory Map Note 3 changed
		26	Special Function Register (SFR) • The RLVL register Value after reset modified
		26	• The IIO0IR to IIO11IR registers Value after reset modified
		27 to 30	• Name of the registers associated to Intelligent I/O changed
		27	• The G0RB register Value after reset modified
		27	• The G1BCR0 and G1BCR1 registers Value after reset modified
		29	• The G0CR register Value after reset modified
		32 to 37	• Note added to the CAN-associated registers
		40	• The TCSPR register Value after reset modified; note 1 added
		41	• The AD00 register Value after reset modified
		42	• The PSC register Value after reset modified
		42	• The PS2 register Value after reset modified
		43	• The PCR register Value after reset modified
		44	• The PSD1 register Value after reset modified
		45	• The PCR register Value after reset modified
		48	Electrical Characteristics • Table 5.2 Electrical Characteristics Parameter f(BCLK) and its values added; min. and max. values for f(RING) added
		49	• Table 5.3 Electrical Characteristics V _{OH} values modified; R _{PULLUP} value modified
		50	• Table 5.3 Electrical Characteristics (Continued) Measurement Condition and standard values for I _{CC} added and some released
		52	• Table 5.6 Flash Memory Version Electrical Characteristics Word Program Time and Lock bit Program Time values modified; parameter All-Unlocked-Block-Erase Time deleted; note 1 deleted
		54	• Table 5.10 Memory Expansion Mode and Microprocessor Mode <i>tac1(RD-DB)</i> expression on note 1 modified; <i>tac2(RD-DB)</i> expression on note 1 added

REVISION HISTORY		M32C/87 Group Datasheet	
Rev.	Date	Description	
		Page	Summary
1.50	Oct 20, 2007	All	All in this manual • Descriptions and formats unified • Notation of numbers changed (e.g. 00₂ → 00_b, FF₁₆ → FF_h) • Notation of pin name changed (e.g. RTP00 → RTP_0, A15(/D15) → [A15/D15]) • [Term changed] - Serial I/O → Serial interface - Clock synchronous serial I/O mode → Clock synchronous mode - Clock asynchronous serial I/O mode → Clock asynchronous mode - Clock synchronous variable length → Variable data length clock synchronous - Voltage detection circuit → Power supply voltage detection function - Low voltage detection interrupt → Vdet4 detection interrupt - Brown-out detection reset → Vdet3 detection function
		1	Overview • Header SINGLE-CHIP 16/32-BIT CMOS MICROCOMPUTER → RENESAS MCU
		2	• 1.1 Features title added; 1.1 Applications changed to 1.1.1 Applications
		2-5	• 1.2 Performance Overview changed to 1.1.2 Specifications • Tables 1.1 to 1.4 Structure, descriptions in Specification field, NOTE, and value partially revised or deleted • Real-Time Port Item deleted; ROM Correction Function Item added
		8	• 1.3 Block Diagram moved following the 1.2 Product List
		6-7	• 1.2 Product List Tables revised; NOTE 1 added
1.50	Oct 20, 2007	9, 14, 15	• Figures 1.3 to 1.5 Arrows for VSS and VCC deleted; NOTES partially modified
		11,17	• Tables 1.9 and 1.13 CLKOUT pin moved from Bus Control Pin column to Control Pin column
		19-22	• Tables 1.15 to 1.19 Descriptions revised; NOTE 1 added
			Memory • Text partially modified
		26	
		34-39	SFR • Tables 4.8 to 4.13 NOTE “Set the PM13 bit in the PM1 register to 1 (2 wait states for SFR area) before accessing the CAN-associated registers.” added
1.50	Oct 20, 2007	45	• Table 4.19 The PSL5 register added to the Address field of 03BBh item; the PSL7 register added to the Address field of 03BFh item • [Register names changed]
		27	002Fh Low Voltage Detection Interrupt Register → Vdet4 Detection Interrupt Register
		34	01C1h UART5 Bit Rate Register → UART5 Baud Rate Register 01C9h UART6 Bit Rate Register → UART6 Baud Rate Register 01D0h UART5, UART6 Transmit/Receive Control Register 2 → UART5, UART6 Transmit/Receive Control Register 01DBh to 01D8h Pulse Output Data Register → RTP Output Buffer Register
		41	0303h to 0302h Timer A1-1 Register → Timer A11 Register 0305h to 0304h Timer A2-1 Register → Timer A21 Register 0307h to 0306h Timer A4-1 Register → Timer A41 Register
		42	0340h Count Start Flag → Count Start Register 0341h Clock Prescaler Reset Flag → Clock Prescaler Reset Register

REVISION HISTORY		M32C/87 Group Datasheet	
Rev.	Date	Description	
		Page	Summary
		42	SFR • [Register names changed] 0342h One-Shot Start Flag → One-Shot Start Register 0344h Up-Down Flag → Up/Down Select Register • [Value After Reset changed] 27 000Fh WDC 000X XXX2 → 00XX XXXXb 27 002Fh D4INT 0016 → XX00 0000b 29 007Bh IIO6IC XX00 X0002 → XXXX X000b 31 00EFh G0CR XX00 X0112 → 0000 X011b 31 00FEh G0IRF 0016 → 0000 XXXXb 32 013Eh G1IRF 0016 → 0000 XXXXb 34 01C7h to 01C6h U5RB XXXX XXXX XXXX 0XXX2 → XXXXh 34 01CFh to 01CEh U6RB XXXX XXXX XXXX 0XXX2 → XXXXh 44 038Fh to 0382h AD07 to AD01 XXXX16 → 00XXh
		47	Electrical Characteristics • [Term changed] Low Voltage Reset → Hardware Reset 2 Low Voltage Detection → Vdet3 and Vdet4 detection circuit • Table 5.1 Description in Condition field of Pd (Power consumption) partially modified • Tables 5.2 to 5.9 f(BCLK) is changed to f(CPU) • Table 5.4 Description added in Parameter field of f(CPU); f(VCO) added • Tables 5.5 to 5.7 and Tables 5.31 to 5.33 Description in XCOUT and Hysteresis in Parameter fields partially modified • Table 5.7 and 5.33 Structure and standard values revised; items in Measurement Condition and NOTE added • Table 5.8 Description in Parameter field and NOTE partially modified • Table 5.9 and 5.10 Description in Parameter field and NOTE partially modified • Tables 5.11 and 5.36 Description in Parameter field and standard value partially modified • Tables 5.19 and 5.42 added • Table 5.24 Values revised; Table 5.25 and 5.26 added • Table 5.27 Titles modified; NOTE added • Table 5.28 moved to the last table in Timing Requirements • Table 5.29 NOTE 3 added; Table 26.30 NOTE 5 added • Figures 5.3 to 5.6 Order rearranged; measurement condition modified • Table 5.31 to 5.35 f(BCLK) revised to f(CPU) • Table 5.47 Values revised; Table 5.48 and 5.49 added • Table 5.50 Titles modified; NOTE added • Table 5.51 Table moved to the last table in Timing Requirements • Table 5.52 NOTE 3 added; Table 5.53 NOTE 5 added • Figures 5.7 to 5.10 Order rearranged
1.51	Jul 31, 2008	–	All in this manual [description modified] • Title of group tables “(current table number / total tables)” added
		19 21	Overview • 1.5 Pin Descriptions Chapter and table title changed to Pin Functions • Table 1.17 Supply voltage for AN0_0 to AN0_7, AN2_0 to AN2_7 modified