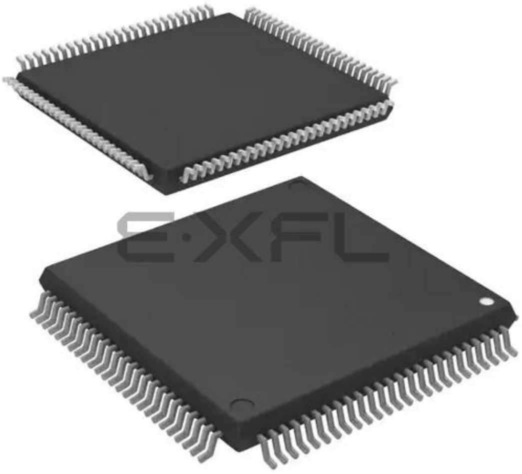
Renesas Electronics America Inc - M30876FJGP#U3 Datasheet



What is "Embedded - Microcontrollers"?

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M32C/80
Core Size	16/32-Bit
Speed	32MHz
Connectivity	CANbus, EBI/EMI, I²C, IEBus, IrDA, SIO, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	85
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	31K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30876fjgp-u3

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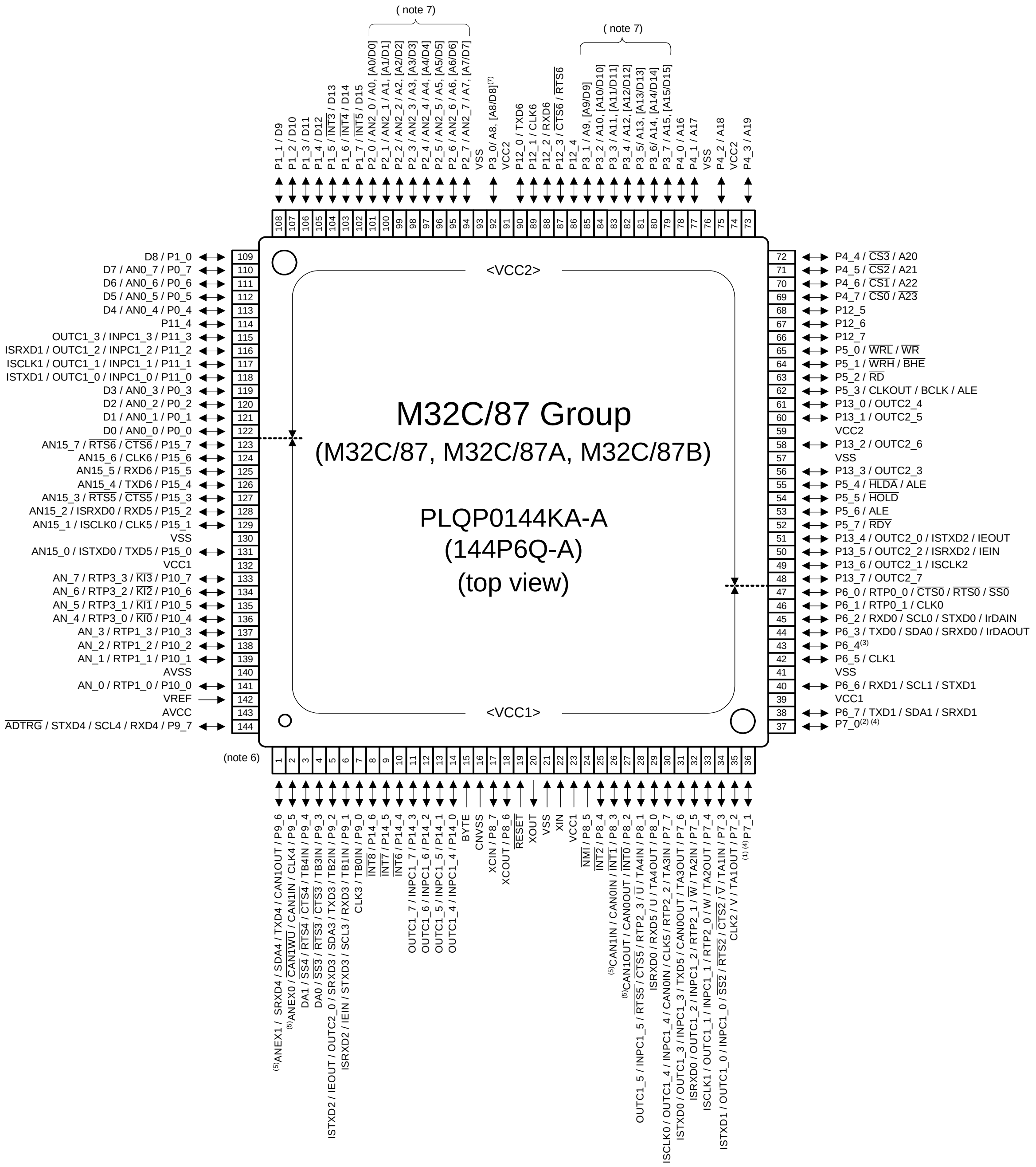
1.4 Pin Assignments

Figures 1.3 to 1.5 show pin assignments (top view).



NOTES:

1. P7_1 / TA0IN / TB5IN / RTP0_3 / RXD2 / SCL2 / STXD2 / INPC1_7 / OUTC1_7 / OUTC2_2 / ISRXD2 / IEIN
2. P7_0 / TA0OUT / RTP0_2 / TXD2 / SDA2 / SRXD2 / INPC1_6 / OUTC1_6 / OUTC2_0 / ISTXD2 / IEOUT
3. P6_4 / CTS1 / RTS1 / SS1 / OUTC2_1 / ISCLK2
4. P7_0 and P7_1 are N-channel open drain output ports.
5. The CAN pins cannot be used in M32C/87B. Only CAN0 pins can be used in M32C/87A.
6. Refer to **Package Dimensions** for the pin1 position on the package.
7. Pin names in brackets [ ] represent a single functional signal. They should not be considered as two separate functional signals.

Figure 1.3 Pin Assignment for 144-Pin Package

Table 1.14 100-Pin Package List of Pin Names (3/3)

Pin No.		Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
FP	GP								
73	71		P1_7	$\overline{\text{INT5}}$					D15
74	72		P1_6	$\overline{\text{INT4}}$					D14
75	73		P1_5	$\overline{\text{INT3}}$					D13
76	74		P1_4						D12
77	75		P1_3						D11
78	76		P1_2						D10
79	77		P1_1						D9
80	78		P1_0						D8
81	79		P0_7					AN0_7	D7
82	80		P0_6					AN0_6	D6
83	81		P0_5					AN0_5	D5
84	82		P0_4					AN0_4	D4
85	83		P0_3					AN0_3	D3
86	84		P0_2					AN0_2	D2
87	85		P0_1					AN0_1	D1
88	86		P0_0					AN0_0	D0
89	87		P10_7	$\overline{\text{KI3}}$	RTP3_3			AN_7	
90	88		P10_6	$\overline{\text{KI2}}$	RTP3_2			AN_6	
91	89		P10_5	$\overline{\text{KI1}}$	RTP3_1			AN_5	
92	90		P10_4	$\overline{\text{KI0}}$	RTP3_0			AN_4	
93	91		P10_3		RTP1_3			AN_3	
94	92		P10_2		RTP1_2			AN_2	
95	93		P10_1		RTP1_1			AN_1	
96	94	AVSS							
97	95		P10_0		RTP1_0			AN_0	
98	96	VREF							
99	97	AVCC							
100	98		P9_7			RXD4/SCL4/STXD4		$\overline{\text{ADTRG}}$	

Table 4.9 SFR Address Map (9/20)

Address	Register(2)(3)	Symbol	After Reset
01F0h	CAN0 Message Slot Buffer 1 Standard ID0	C0SLOT1_0	XXh
01F1h	CAN0 Message Slot Buffer 1 Standard ID1	C0SLOT1_1	XXh
01F2h	CAN0 Message Slot Buffer 1 Extended ID0	C0SLOT1_2	XXh
01F3h	CAN0 Message Slot Buffer 1 Extended ID1	C0SLOT1_3	XXh
01F4h	CAN0 Message Slot Buffer 1 Extended ID2	C0SLOT1_4	XXh
01F5h	CAN0 Message Slot Buffer 1 Data Length Code	C0SLOT1_5	XXh
01F6h	CAN0 Message Slot Buffer 1 Data 0	C0SLOT1_6	XXh
01F7h	CAN0 Message Slot Buffer 1 Data 1	C0SLOT1_7	XXh
01F8h	CAN0 Message Slot Buffer 1 Data 2	C0SLOT1_8	XXh
01F9h	CAN0 Message Slot Buffer 1 Data 3	C0SLOT1_9	XXh
01FAh	CAN0 Message Slot Buffer 1 Data 4	C0SLOT1_10	XXh
01FBh	CAN0 Message Slot Buffer 1 Data 5	C0SLOT1_11	XXh
01FCh	CAN0 Message Slot Buffer 1 Data 6	C0SLOT1_12	XXh
01FDh	CAN0 Message Slot Buffer 1 Data 7	C0SLOT1_13	XXh
01FEh	CAN0 Message Slot Buffer 1 Time Stamp High-Order	C0SLOT1_14	XXh
01FFh	CAN0 Message Slot Buffer 1 Time Stamp Low-Order	C0SLOT1_15	XXh
0200h	CAN0 Control Register 0	C0CTLR0	XX01 0X01b(1)
0201h			XXXX 0000b(1)
0202h	CAN0 Status Register	C0STR	0000 0000b(1)
0203h			X000 0X01b(1)
0204h	CAN0 Extended ID Register	C0IDR	0000h(1)
0205h			
0206h	CAN0 Configuration Register	C0CONR	0000 XXXXb(1)
0207h			0000 0000b(1)
0208h	CAN0 Time Stamp Register	C0TSR	0000h(1)
0209h			
020Ah	CAN0 Transmit Error Count Register	C0TEC	00h(1)
020Bh	CAN0 Receive Error Count Register	C0REC	00h(1)
020Ch	CAN0 Slot Interrupt Status Register	C0SISTR	0000h(1)
020Dh			
020Eh			
020Fh			
0210h	CAN0 Slot Interrupt Mask Register	C0SIMKR	0000h(1)
0211h			
0212h			
0213h			
0214h	CAN0 Error Interrupt Mask Register	C0EIMKR	XXXX X000b(1)
0215h	CAN0 Error Interrupt Status Register	C0EISTR	XXXX X000b(1)
0216h	CAN0 Error Source Register	C0EFR	00h(1)
0217h	CAN0 Baud Rate Prescaler	C0BRP	0000 0001b(1)
0218h			
0219h	CAN0 Mode Register	C0MDR	XXXX XX00b(1)
021Ah			
021Bh			
021Ch			
021Dh			
021Eh			
021Fh			

X: Undefined
Blank spaces are all reserved. No access is allowed.
NOTES:

1. Values are obtained by setting the SLEEP bit in the C0SLPR register to “1” (sleep mode exited) after reset and supplying a clock to the CAN module.
2. The CAN-associated registers (allocated in addresses 01E0h to 02BFh) cannot be used in M32C/87B. In M32C/87A, only CAN0-associated registers can be used.
3. Set the PM13 bit in the PM1 register to 1 (2 wait states for SFR area) before accessing the CAN-associated registers.

Table 4.13 SFR Address Map (13/20)

Address	Register(3)(4)	Symbol	After Reset
02B0h	CAN1 Message Slot 0 Control Register / CAN1 Local Mask Register A Standard ID0	C1MCTL0 / C1LMAR0	0000 0000b(1)(2)/ XXX0 0000b(1)(2)
02B1h	CAN1 Message Slot 1 Control Register / CAN1 Local Mask Register A Standard ID1	C1MCTL1 / C1LMAR1	0000 0000b(1)(2)/ XX00 0000b(1)(2)
02B2h	CAN1 Message Slot 2 Control Register / CAN1 Local Mask Register A Extended ID0	C1MCTL2 / C1LMAR2	0000 0000b(1)(2)/ XXXX 0000b(1)(2)
02B3h	CAN1 Message Slot 3 Control Register / CAN1 Local Mask Register A Extended ID1	C1MCTL3 / C1LMAR3	00h(1)(2)/ 00h(1)(2)
02B4h	CAN1 Message Slot 4 Control Register / CAN1 Local Mask Register A Extended ID2	C1MCTL4 / C1LMAR4	0000 0000b(1)(2)/ XX00 0000b(1)(2)
02B5h	CAN1 Message Slot 5 Control Register	C1MCTL5	00h(1)(2)
02B6h	CAN1 Message Slot 6 Control Register	C1MCTL6	00h(1)(2)
02B7h	CAN1 Message Slot 7 Control Register	C1MCTL7	00h(1)(2)
02B8h	CAN1 Message Slot 8 Control Register / CAN1 Local Mask Register B Standard ID0	C1MCTL8 / C1LMBR0	0000 0000b(1)(2)/ XXX0 0000b(1)(2)
02B9h	CAN1 Message Slot 9 Control Register / CAN1 Local Mask Register B Standard ID1	C1MCTL9 / C1LMBR1	0000 0000b(1)(2)/ XX00 0000b(1)(2)
02BAh	CAN1 Message Slot 10 Control Register / CAN1 Local Mask Register B Extended ID0	C1MCTL10 / C1LMBR2	0000 0000b(1)(2)/ XXXX 0000b(1)(2)
02BBh	CAN1 Message Slot 11 Control Register / CAN1 Local Mask Register B Extended ID1	C1MCTL11 / C1LMBR3	00h(1)(2)/ 00h(1)(2)
02BCh	CAN1 Message Slot 12 Control Register / CAN1 Local Mask Register B Extended ID2	C1MCTL12 / C1LMBR4	0000 0000b(1)(2)/ XX00 0000b(1)(2)
02BDh	CAN1 Message Slot 13 Control Register	C1MCTL13	00h(1)(2)
02BEh	CAN1 Message Slot 14 Control Register	C1MCTL14	00h(1)(2)
02BFh	CAN1 Message Slot 15 Control Register	C1MCTL15	00h(1)(2)

X: Undefined
Blank spaces are all reserved. No access is allowed.
NOTES:

1. The BANKSEL bit in the C1CTLR1 register can switch functions for addresses 02A0h to 02BFh.
2. Values are obtained by setting the SLEEP bit in the C1SLPR register to “1” (sleep mode exited) after reset and supplying a clock to the CAN module.
3. The CAN-associated registers (allocated in addresses 01E0h to 02BFh) cannot be used in M32C/87B. In M32C/87A, only CAN0-associated registers can be used.
4. Set the PM13 bit in the PM1 register to 1 (2 wait states for SFR area) before accessing the CAN-associated registers.

Table 4.14 SFR Address Map (14/20)

Address	Register	Symbol	After Reset
02C0h	X0 Register, Y0 Register	X0R, Y0R	XXXXh
02C1h			
02C2h	X1 Register, Y1 Register	X1R, Y1R	XXXXh
02C3h			
02C4h	X2 Register, Y2 Register	X2R, Y2R	XXXXh
02C5h			
02C6h	X3 Register, Y3 Register	X3R, Y3R	XXXXh
02C7h			
02C8h	X4 Register, Y4 Register	X4R, Y4R	XXXXh
02C9h			
02CAh	X5 Register, Y5 Register	X5R, Y5R	XXXXh
02CBh			
02CCh	X6 Register, Y6 Register	X6R, Y6R	XXXXh
02CDh			
02CEh	X7 Register, Y7 Register	X7R, Y7R	XXXXh
02CFh			
02D0h	X8 Register, Y8 Register	X8R, Y8R	XXXXh
02D1h			
02D2h	X9 Register, Y9 Register	X9R, Y9R	XXXXh
02D3h			
02D4h	X10 Register, Y10 Register	X10R, Y10R	XXXXh
02D5h			
02D6h	X11 Register, Y11 Register	X11R, Y11R	XXXXh
02D7h			
02D8h	X12 Register, Y12 Register	X12R, Y12R	XXXXh
02D9h			
02DAh	X13 Register, Y13 Register	X13R, Y13R	XXXXh
02DBh			
02DCh	X14 Register, Y14 Register	X14R, Y14R	XXXXh
02DDh			
02DEh	X15 Register, Y15 Register	X15R, Y15R	XXXXh
02DFh			
02E0h	X/Y Control Register	XYC	XXXX XX00b
02E1h			
02E2h			
02E3h			
02E4h	UART1 Special Mode Register 4	U1SMR4	00h
02E5h	UART1 Special Mode Register 3	U1SMR3	00h
02E6h	UART1 Special Mode Register 2	U1SMR2	00h
02E7h	UART1 Special Mode Register	U1SMR	00h
02E8h	UART1 Transmit/Receive Mode Register	U1MR	00h
02E9h	UART1 Baud Rate Register	U1BRG	XXh
02EAh	UART1 Transmit Buffer Register	U1TB	XXXXh
02EBh			
02ECh	UART1 Transmit/Receive Control Register 0	U1C0	0000 1000b
02EDh	UART1 Transmit/Receive Control Register 1	U1C1	0000 0010b
02EEh	UART1 Receive Buffer Register	U1RB	XXXXh
02EFh			

X: Undefined
Blank spaces are all reserved. No access is allowed.

Table 4.19 SFR Address Map (19/20)

Address	Register	Symbol	After Reset
03A0h	Function Select Register A8(1)	PS8	X000 0000b
03A1h	Function Select Register A9(1)	PS9	00h
03A2h			
03A3h	Function Select Register B9(1)	PSL9	XXX0 XX00b
03A4h	Function Select Register E2	PSE2	XXXX XX0Xb
03A5h			
03A6h			
03A7h	Function Select Register D1	PSD1	00X0 XX00b
03A8h	Function Select Register D2	PSD2	XXXX XX0Xb
03A9h			
03AAh	Function Select Register C6(1)	PSC6	XXXX 0X00b
03ABh	Function Select Register E1	PSE1	00XX XX00b
03ACh	Function Select Register C2	PSC2	XXXX X00Xb
03ADh	Function Select Register C3	PSC3	X0XX XXXXb
03AEh			
03AFh	Function Select Register C	PSC	00h
03B0h	Function Select Register A0	PS0	00h
03B1h	Function Select Register A1	PS1	00h
03B2h	Function Select Register B0	PSL0	00h
03B3h	Function Select Register B1	PSL1	00h
03B4h	Function Select Register A2	PS2	00X0 0000b
03B5h	Function Select Register A3	PS3	00h
03B6h	Function Select Register B2	PSL2	00X0 0000b
03B7h	Function Select Register B3	PSL3	00h
03B8h	Function Select Register A4	PS4	00h
03B9h	Function Select Register A5(1)	PS5	XXX0 0000b
03BAh			
03BBh	Function Select Register B5(1)	PSL5	XXX0 0000b
03BCh	Function Select Register A6(1)	PS6	00h
03BDh	Function Select Register A7(1)	PS7	00h
03BEh	Function Select Register B6(1)	PSL6	00h
03BFh	Function Select Register B7(1)	PSL7	00h
03C0h	Port P6 Register	P6	XXh
03C1h	Port P7 Register	P7	XXh
03C2h	Port P6 Direction Register	PD6	00h
03C3h	Port P7 Direction Register	PD7	00h
03C4h	Port P8 Register	P8	XXh
03C5h	Port P9 Register	P9	XXh
03C6h	Port P8 Direction Register	PD8	00X0 0000b
03C7h	Port P9 Direction Register	PD9	00h
03C8h	Port P10 Register	P10	XXh
03C9h	Port P11 Register(1)	P11	XXh
03CAh	Port P10 Direction Register	PD10	00h
03CBh	Port P11 Direction Register(1)(2)	PD11	XXX0 0000b
03CCh	Port P12 Register(1)	P12	XXh
03CDh	Port P13 Register(1)	P13	XXh
03CEh	Port P12 Direction Register(1)(2)	PD12	00h
03CFh	Port P13 Direction Register(1)(2)	PD13	00h

X: Undefined
Blank spaces are all reserved. No access is allowed.
NOTES:
1. These registers cannot be used in the 100-pin package.
2. Set to FFh in the 100-pin package.

Table 5.3 Recommended Operating Conditions (2/3)
(VCC1 = VCC2 = 3.0 to 5.5 V, Topr = -20 to 85°C unless otherwise specified

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
IOH(peak)	Peak output high "H" current(2)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7(3)			-10.0	mA
IOH(avg)	Average output high "H" current(1)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7(3)			-5.0	mA
IOL(peak)	Peak output low "L" current(2)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7(3)			10.0	mA
IOL(avg)	Average output low "L" current(1)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7(3)			5.0	mA

NOTES:

1. Average output current is the average value within 100 ms.
2. A total IOL(peak) of P0, P1, P2, P8_6, P8_7, P9, P10, P11, P14, and P15 must be 80 mA or less.
   A total IOL(peak) of P3, P4, P5, P6, P7,P8_0 to P8_4, P12, and P13 must be 80 mA or less.
   A total IOH(peak) of P0, P1, P2, and P11 must be -40 mA or less.
   A total IOH(peak) of P8_6 to P8_7, P9, P10, P14, and P15 must be -40 mA or less.
   A total IOH(peak) of P3, P4, P5, P12, and P13 must be -40 mA or less.
   A total IOH(peak) of P6, P7, and P8_0 to P8_4 must be -40 mA or less.
3. P11 to P15 are provided in the 144-pin package only.

VCC1 = VCC2 = 5V

Timing Requirements
(VCC1 = VCC2 = 4.2 to 5.5 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.18 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(UP)	TAiOUT input cycle time	2000		ns
tw(UPH)	TAiOUT input high (“H”) pulse width	1000		ns
tw(UPL)	TAiOUT input low (“L”) pulse width	1000		ns
tsu(UP-TIN)	TAiOUT input setup time	400		ns
th(TIN-UP)	TAiOUT input hold time	400		ns

i = 0 to 4

Table 5.19 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	800		ns
tsu(TAIN-TAOUT)	TAiOUT input setup time	200		ns
tsu(TAOUT-TAIN)	TAiIN input setup time	200		ns

i = 0 to 4

Table 5.20 Timer B Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TB)	TBiIN input cycle time (counted on one edge)	100		ns
tw(TBH)	TBiIN input high (“H”) pulse width (counted on one edge)	40		ns
tw(TBL)	TBiIN input low (“L”) pulse width (counted on one edge)	40		ns
tc(TB)	TBiIN input cycle time (counted on both edges)	200		ns
tw(TBH)	TBiIN input high (“H”) pulse width (counted on both edges)	80		ns
tw(TBL)	TBiIN input low (“L”) pulse width (counted on both edges)	80		ns

i = 0 to 5

Table 5.21 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TB)	TBiIN input cycle time	400		ns
tw(TBH)	TBiIN input high (“H”) pulse width	200		ns
tw(TBL)	TBiIN input low (“L”) pulse width	200		ns

i = 0 to 5

Table 5.22 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TB)	TBiIN input cycle time	400		ns
tw(TBH)	TBiIN input high (“H”) pulse width	200		ns
tw(TBL)	TBiIN input low (“L”) pulse width	200		ns

i = 0 to 5

VCC1 = VCC2 = 5V

Timing Requirements
(VCC1 = VCC2 = 4.2 to 5.5 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.28 Memory Expansion mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tac1(RD-DB)	Data input access time (RD standard)		(note 1)	ns
tac1(AD-DB)	Data input access time (AD standard, CS standard)		(note 1)	ns
tac2(RD-DB)	Data input access time (RD standard, when accessing a space with the multiplexed bus)		(note 1)	ns
tac2(AD-DB)	Data input access time (AD standard, when accessing a space with the multiplexed bus)		(note 1)	ns
tsu(DB-BCLK)	Data input setup time	26		ns
tsu(RDY-BCLK)	$\overline{\text{RDY}}$ input setup time	26		ns
tsu(HOLD-BCLK)	$\overline{\text{HOLD}}$ input setup time	30		ns
th(RD-DB)	Data input hold time	0		ns
th(BCLK-RDY)	$\overline{\text{RDY}}$ input hold time	0		ns
th(BCLK-HOLD)	$\overline{\text{HOLD}}$ input hold time	0		ns
td(BCLK-HLDA)	$\overline{\text{HLDA}}$ output delay time		25	ns

NOTE:

1. Values, which depend on BCLK frequency and external bus cycles, can be obtained from the following equations. Insert wait states or lower the operation frequency, f(BCLK), if the calculated value is negative.

$$\text{tac1(RD-DB)} = \frac{10^9 \times m}{f(\text{BCLK}) \times 2} - 35\ [\text{ns}]\ (\text{if external bus cycle is } a\phi + b\phi,\ m = (b \times 2) + 1)$$

$$\text{tac1(AD-DB)} = \frac{10^9 \times n}{f(\text{BCLK})} - 35\ [\text{ns}]\ (\text{if external bus cycle is } a\phi + b\phi,\ n = a + b)$$

$$\text{tac2(RD-DB)} = \frac{10^9 \times m}{f(\text{BCLK}) \times 2} - 35\ [\text{ns}]\ (\text{if external bus cycle is } a\phi + b\phi,\ m = (b \times 2) - 1)$$

$$\text{tac2(AD-DB)} = \frac{10^9 \times p}{f(\text{BCLK}) \times 2} - 35\ [\text{ns}]\ (\text{if external bus cycle is } a\phi + b\phi,\ p = \{(a + b - 1) \times 2\} + 1)$$

VCC1 = VCC2 = 5V

Switching Characteristics
(VCC1 = VCC2 = 4.2 to 5.5 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.30 Memory Expansion Mode and Microprocessor Mode (when accessing external memory space with multiplexed bus)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min.	Max.	
td(BCLK-AD)	Address output delay time	See Figure 5.2		18	ns
th(BCLK-AD)	Address output hold time (BCLK standard)		-3		ns
th(RD-AD)	Address output hold time (RD standard)(5)		(note 1)		ns
th(WR-AD)	Address output hold time (WR standard)(5)		(note 1)		ns
td(BCLK-CS)	Chip-select signal output delay time			18	ns
th(BCLK-CS)	Chip-select signal output hold time (BCLK standard)		-3		ns
th(RD-CS)	Chip-select signal output hold time (RD standard)(5)		(note 1)		ns
th(WR-CS)	Chip-select signal output hold time (WR standard)(5)		(note 1)		ns
td(BCLK-RD)	RD signal output delay time			18	ns
th(BCLK-RD)	RD signal output hold time		-5		ns
td(BCLK-WR)	WR signal output delay time			18	ns
th(BCLK-WR)	WR signal output hold time		-5		ns
td(DB-WR)	Data output delay time (WR standard)		(note 2)		ns
th(WR-DB)	Data output hold time (WR standard)(5)		(note 1)		ns
td(BCLK-ALE)	ALE signal output delay time (BCLK standard)			18	ns
th(BCLK-ALE)	ALE signal output hold time (BCLK standard)		-2		ns
td(AD-ALE)	ALE signal output delay time (address standard)		(note 3)		ns
th(ALE-AD)	ALE signal output hold time (address standard)		(note 4)		ns
tdz(RD-AD)	Address output float start time			8	ns

NOTES:

1. Values, which depend on BCLK frequency, can be obtained from the following equations.

$$th(RD\text{-}AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \text{ [ns]}$$

$$th(WR\text{-}AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \text{ [ns]}$$

$$th(RD\text{-}CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \text{ [ns]}$$

$$th(WR\text{-}CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \text{ [ns]}$$

$$th(WR\text{-}DB) = \frac{10^9}{f(BCLK) \times 2} - 15 \text{ [ns]}$$

2. Values, which depend on BCLK frequency and external bus cycles, can be obtained from the following equation.

$$td(DB\text{-}WR) = \frac{10^9 \times m}{f(BCLK) \times 2} - 25 \text{ [ns] (if external bus cycle is } a\phi + b\phi,\ m = (b \times 2) - 1)$$

3. Values, which depend on BCLK frequency and external bus cycles, can be obtained from the following equation.

$$td(AD\text{-}ALE) = \frac{10^9 \times n}{f(BCLK) \times 2} - 20 \text{ [ns] (if external bus cycle is } a\phi + b\phi,\ n = a)$$

4. Values, which depend on BCLK frequency and external bus cycles, can be obtained from the following equation.

$$th(ALE\text{-}AD) = \frac{10^9 \times n}{f(BCLK) \times 2} - 20 \text{ [ns] (if external bus cycle is } a\phi + b\phi,\ n = a)$$

5. tc [ns] is added when recovery cycle is inserted.

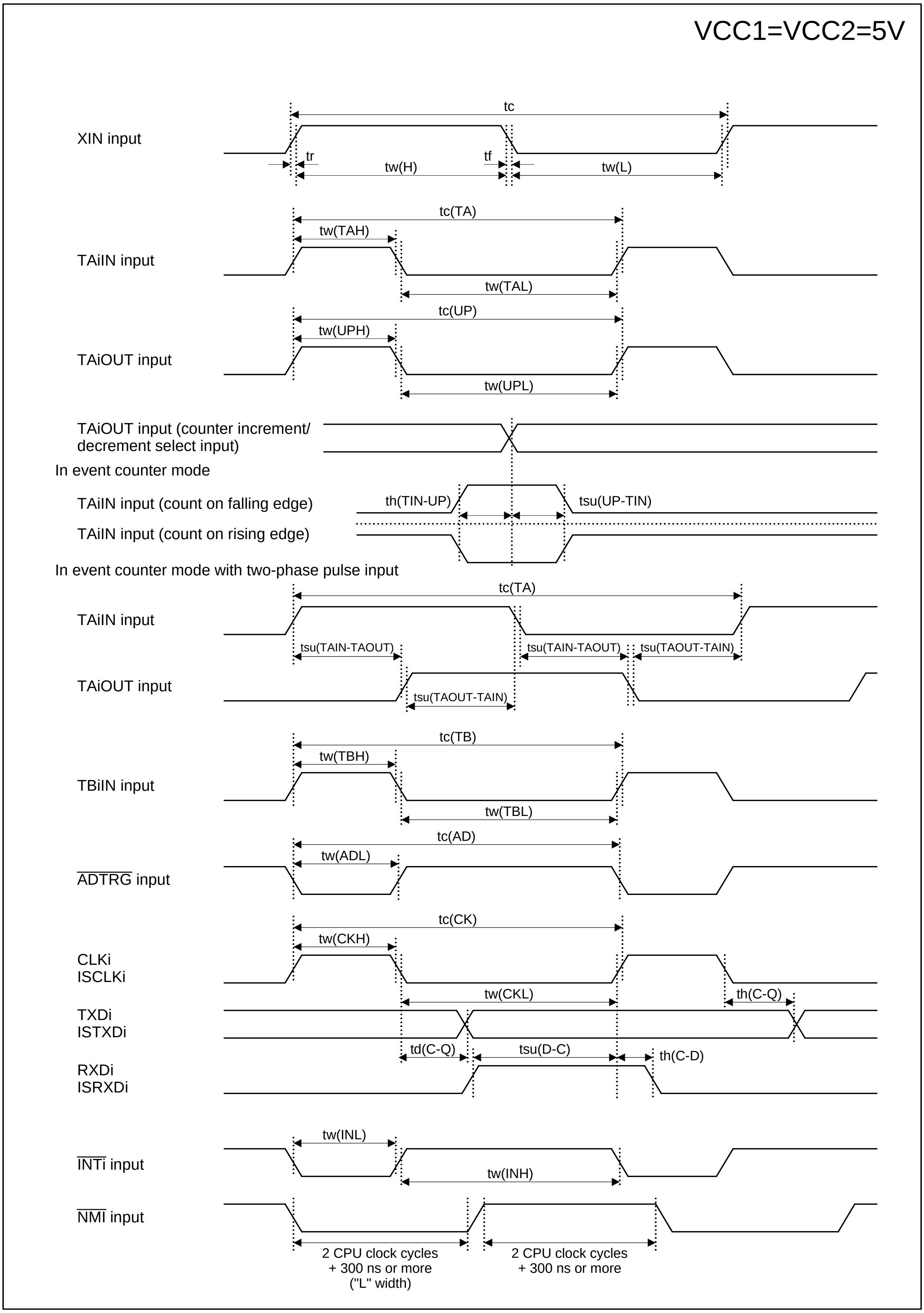


Figure 5.3 VCC1 = VCC2 = 5 V Timing Diagram (1/4)

VCC1 = VCC2 = 3.3 V

Table 5.33 Electrical Characteristics (3/3)
(VCC1 = VCC2 = 3.3 V, VSS = 0 V, Topr = 25°C)

Symbol	Parameter	Measurement Condition(1)		Standard			Unit
				Min.	Typ.	Max.	
ICC	Power supply current	Flash memory version	f(CPU) = 24 MHz		23	33	mA
			f(CPU) = 16 MHz		17		mA
			f(CPU) = 8 MHz		11		mA
			f(CPU) = f(Ring) In on-chip oscillator low-power consumption mode		2.6		mA
			f(CPU) = 32 kHz In low-power consumption mode While flash memory is operating		430		µA
			f(CPU) = 32 kHz In low-power consumption mode While flash memory is stopped(2)		30		µA
			Wait mode: f(CPU) = f(Ring) After entering wait mode from on-chip oscillator low-power consumption mode		45		µA
			Stop mode (while clock is stopped)		0.8	5	µA
			Stop mode (while clock is stopped) Topr = 85°C			50	µA
		Mask ROM version	f(CPU) = 24 MHz		23	33	mA
			f(CPU) = 16 MHz		17		mA
			f(CPU) = 8 MHz		11		mA
			f(CPU) = f(Ring) In on-chip oscillator low-power consumption mode		1		mA
			f(CPU) = 32 kHz In low-power consumption mode		30		µA
			Wait mode: f(CPU) = f(Ring) After entering wait mode from on-chip oscillator low-power consumption mode		45		µA
			Stop mode (while clock is stopped)		0.8	5	µA
			Stop mode (while clock is stopped) Topr = 85°C			50	µA

NOTES:
1. In single-chip mode, leave the output pins open and connect the input pins to VSS.
2. Value is obtained when setting the FMSTP bit in the FMR0 register to 1 (flash memory stopped) and running the program on RAM.

VCC1 = VCC2 = 3.3 V

Timing Requirements
(VCC1 = VCC2 = 3.0 to 3.6 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.41 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(UP)	TAiOUT input cycle time	2000		ns
tw(UPH)	TAiOUT input high (“H”) pulse width	1000		ns
tw(UPL)	TAiOUT input low (“L”) pulse width	1000		ns
tsu(UP-TIN)	TAiOUT input setup time	400		ns
th(TIN-UP)	TAiOUT input hold time	400		ns

i = 0 to 4

Table 5.42 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	2		µs
tsu(TAIN-TAOUT)	TAiOUT input setup time	500		ns
tsu(TAOUT-TAIN)	TAiIN input setup time	500		ns

i = 0 to 4

Table 5.43 Timer B Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TB)	TBiIN input cycle time (counted on one edge)	100		ns
tw(TBH)	TBiIN input high (“H”) pulse width (counted on one edge)	40		ns
tw(TBL)	TBiIN input low (“L”) pulse width (counted on one edge)	40		ns
tc(TB)	TBiIN input cycle time (counted on both edges)	200		ns
tw(TBH)	TBiIN input high (“H”) pulse width (counted on both edges)	80		ns
tw(TBL)	TBiIN input low (“L”) pulse width (counted on both edges)	80		ns

i = 0 to 5

Table 5.44 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TB)	TBiIN input cycle time	400		ns
tw(TBH)	TBiIN input high (“H”) pulse width	200		ns
tw(TBL)	TBiIN input low (“L”) pulse width	200		ns

i = 0 to 5

Table 5.45 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TB)	TBiIN input cycle time	400		ns
tw(TBH)	TBiIN input high (“H”) pulse width	200		ns
tw(TBL)	TBiIN input low (“L”) pulse width	200		ns

i = 0 to 5

VCC1 = VCC2 = 3.3 V

Timing Requirements
(VCC1 = VCC2 = 3.0 to 3.6 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.50 External Interrupt INTi Input (Edge Sensitive)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tw(INH)	INTi input high (“H”) pulse width	250		ns
tw(INL)	INTi input low (“L”) pulse width	250		ns

i = 0 to 8(1)
NOTE:
1. INT6 to INT8 are provided in the 144-pin package only.

VCC1 = VCC2 = 3.3 V

Switching Characteristics
(VCC1 = VCC2 = 3.0 to 3.6 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.52 Memory Expansion Mode and Microprocessor Mode (when accessing external memory space)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min.	Max.	
td(BCLK-AD)	Address output delay time	See Figure 5.2		18	ns
th(BCLK-AD)	Address output hold time (BCLK standard)		-3		ns
th(RD-AD)	Address output hold time (RD standard)(3)		0		ns
th(WR-AD)	Address output hold time (WR standard)(3)		(note 1)		ns
td(BCLK-CS)	Chip-select signal output delay time			18	ns
th(BCLK-CS)	Chip-select signal output hold time (BCLK standard)		-3		ns
th(RD-CS)	Chip-select signal output hold time (RD standard)(3)		0		ns
th(WR-CS)	Chip-select signal output hold time (WR standard)(3)		(note 1)		ns
td(BCLK-RD)	RD signal output delay time			18	ns
th(BCLK-RD)	RD signal output hold time		-5		ns
td(BCLK-WR)	WR signal output delay time			18	ns
th(BCLK-WR)	WR signal output hold time		0		ns
td(DB-WR)	Data output delay time (WR standard)		(note 2)		ns
th(WR-DB)	Data output hold time (WR standard)(3)		(note 1)		ns
tw(WR)	WR output width		(note 2)		ns

NOTES:

1. Values, which depend on BCLK frequency, can be obtained from the following equations.

$$th(WR\text{-}DB) = \frac{10^9}{f(BCLK) \times 2} - 20 \text{ [ns]}$$

$$th(WR\text{-}AD) = \frac{10^9}{f(BCLK) \times 2} - 15 \text{ [ns]}$$

$$th(WR\text{-}CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \text{ [ns]}$$

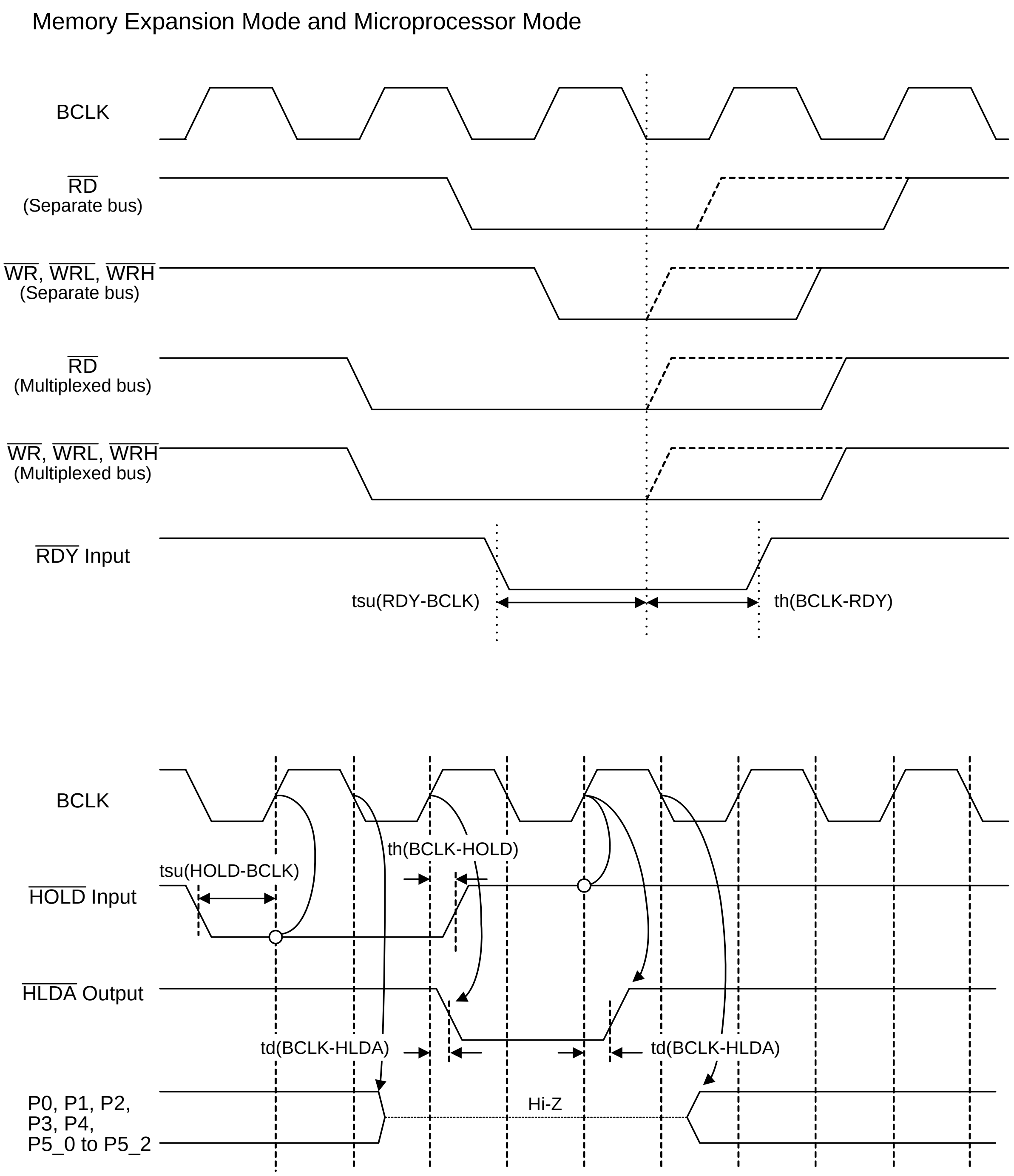
2. Values, which depend on BCLK frequency and external bus cycles, can be obtained from the following equations.

$$td(DB\text{-}WR) = \frac{10^9 \times m}{f(BCLK)} - 20 \text{ [ns] (if external bus cycle is } a\phi + b\phi,\ m = b)$$

$$tw(WR) = \frac{10^9 \times n}{f(BCLK) \times 2} - 15 \text{ [ns] (if external bus cycle is } a\phi + b\phi,\ n = (b \times 2) - 1)$$

3. tc [ns] is added when recovery cycle is inserted.

VCC1=VCC2=3.3V



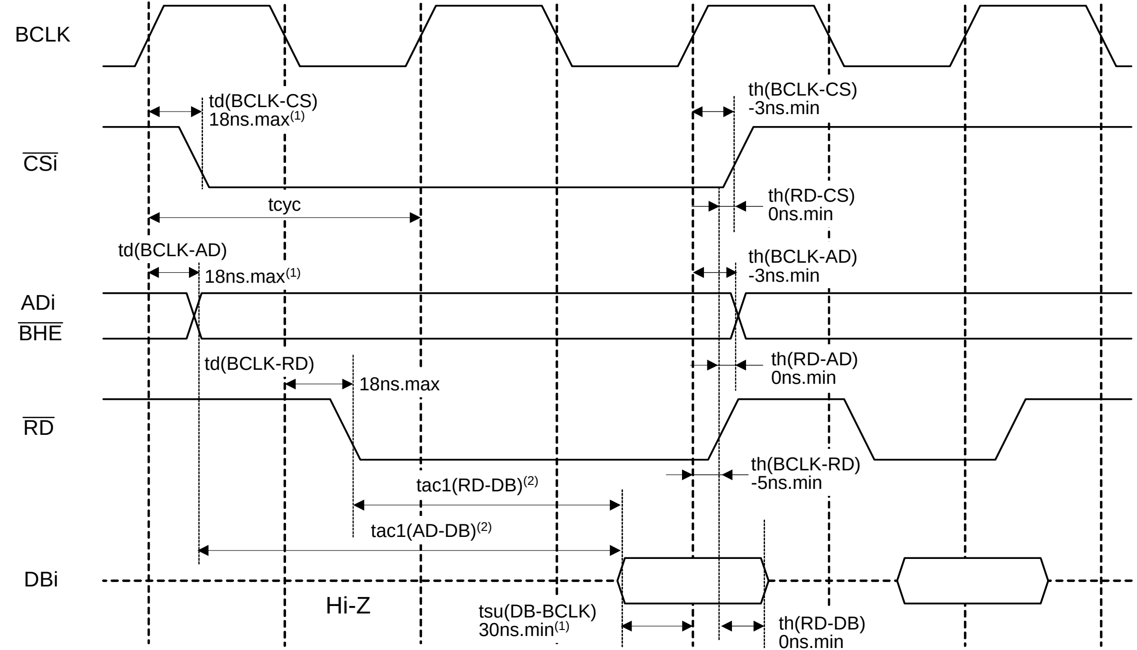
Measurement Conditions
-VCC1 = VCC2 = 3.0 to 3.6 V
-Input high and low voltage: VIH = 2.4 V, VIL = 0.6 V
-Output high and low voltage: VOH = 1.5 V, VOL = 1.5 V

Figure 5.8 VCC1 = VCC2 = 3.3 V Timing Diagram (2/4)

Memory Expansion Mode and Microprocessor Mode
(when accessing an external memory space)

VCC1=VCC2=3.3V

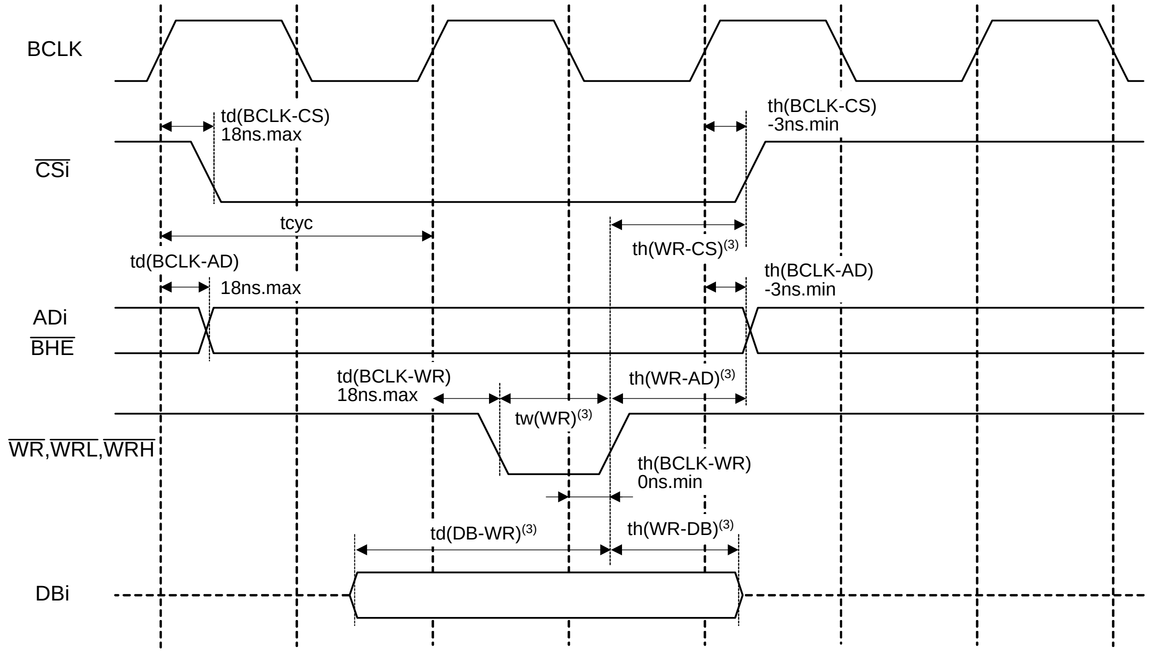
Read Timing (1ϕ + 1ϕ Bus Cycle)



NOTES:

1. Values guaranteed only when the MCU is used stand-alone.
   A maximum of 35 ns is guaranteed for td(BCLK-AD) + tsu(DB-BCLK).
2. Varies with operation frequency:
   tac1(RD-DB) = (tcyc / 2 x m - 35) ns.max (if external bus cycle aϕ + bϕ, m = (b x 2) + 1)
   tac1(AD-DB) = (tcyc x n - 35) ns.max (if external bus cycle aϕ + bϕ, n = a + b)

Write Timing (1ϕ + 1ϕ Bus Cycle)



NOTES:

3. Varies with operation frequency:
   td(DB-WR) = (tcyc x m - 20) ns.min
   (if external bus cycle aϕ + bϕ, m = b)
   th(WR-DB) = (tcyc / 2 - 20) ns.min
   th(WR-AD) = (tcyc / 2 - 15) ns.min
   th(WR-CS) = (tcyc / 2 - 10) ns.min
   tw(WR) = (tcyc / 2 x n - 15) ns.min
   (if external bus cycle aϕ + bϕ, n = (b x 2) - 1)

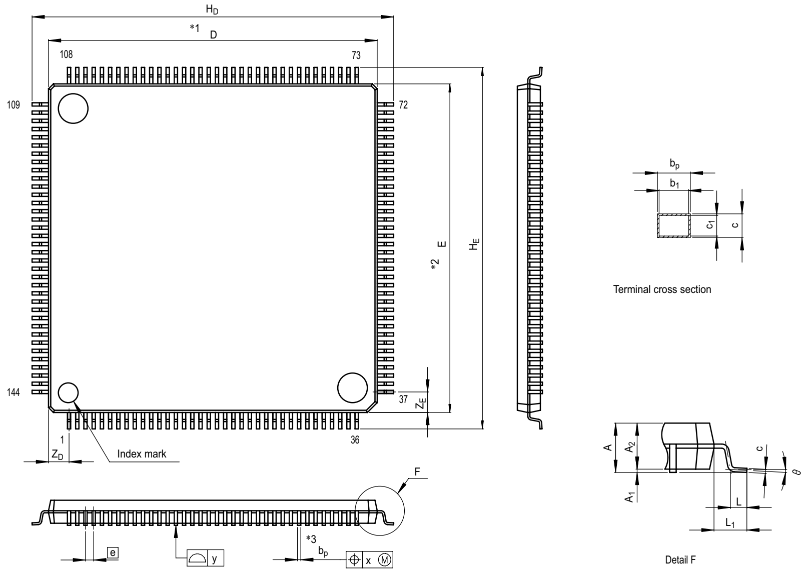
Measurement Conditions:
- VCC1 = VCC2 = 3.0 to 3.6 V
- Input high and low voltage: VIH = 1.5 V, VIL = 0.5 V
- Output high and low voltage: VOH = 1.5 V, VOL = 1.5 V

$$\text{tcyc}= \frac{10^9}{\text{f(BCLK)}}$$

Figure 5.9 VCC1 = VCC2 = 3.3 V Timing Diagram (3/4)

Appendix 1. Package Dimensions

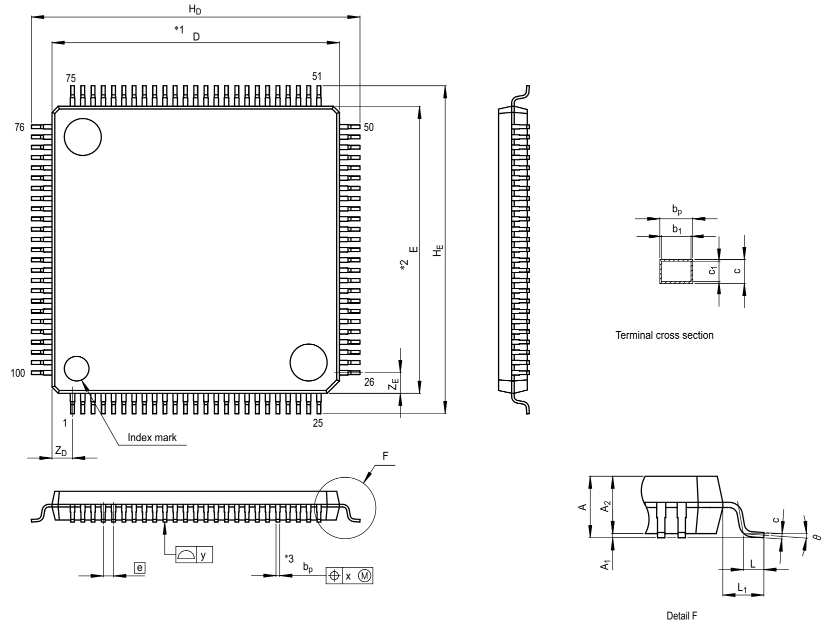
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP144-20x20-0.50	PLQP0144KA-A	144P6Q-A / FP-144L / FP-144LV	1.2g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.9	20.0	20.1
E	19.9	20.0	20.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.35	0.5	0.65
L_1	—	1.0	—

REVISION HISTORY

M32C/87 Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.50	Dec.16, 04	–	New Document
1.00	Jul.14, 05	–	**M32C/87A and M32C/87B** added
		–	Package code changed: 144P6Q-A to PLQP0144KA-A, 100P6Q-A to PLQP0100KB-A, 100P6S-A to PRQP0100JB-A
		–	“Low Voltage Detection Reset” changed to “Brown-out Detection Reset”
			Overview
		2	• **Table 1.2 M32C/87 Group Performance (144-Pin Package)** M32C/87A and M32C/87B performance added to the CAN module performance; Power Consumption performance released
		3	• **Table 1.2 M32C/87 Group Performance (100-Pin Package)** M32C/87A and M32C/87B performance added to the CAN module performance; Power Consumption performance released
		4	• **Figure 1.1 M32C/87 Group Block Diagram** Note 4 deleted; note 5 added
		7	• **Figure 1.3 Pin Assignment for 144-Pin Package** Note 15 added
		8	• **Table 1.4 Pin Characteristics for 144-Pin Package** Note 1 added
		11	• **Figure 1.4 Pin Assignment for 100-Pin Package** Note 19 added
		12	• **Figure 1.5 Pin Assignment for 100-Pin Package** Note 15 added
		13	• **Table 1.5 Pin Characteristics for 100-Pin Package** Note 1 added
		17	• **Table 1.6 Pin Description** Note 2 added
			Memory
		22	• **Figure 3.1 Memory Map** Note 3 changed
			Special Function Register (SFR)
		26	• The RLVL register Value after reset modified
		26	• The IIO0IR to IIO11IR registers Value after reset modified
		27 to 30	• Name of the registers assosiated to Intelligent I/O changed
		27	• The G0RB register Value after reset modified
		27	• The G1BCR0 and G1BCR1 registers Value after reset modified
		29	• The G0CR register Value after reset modified
		32 to 37	• Note added to the CAN-associated registers
		40	• The TCSPR register Value after reset modified; note 1 added
		41	• The AD00 register Value after reset modified
		42	• The PSC register Value after reset modified
		42	• The PS2 register Value after reset modified
		43	• The PCR register Value after reset modified
		44	• The PSD1 register Value after reset modified
		45	• The PCR register Value after reset modified
			Electrical Characteristics
		48	• **Table 5.2 Electrical Characteristics** Parameter f(BCLK) and its values added; min. and max. values for f(RING) added
		49	• **Table 5.3 Electrical Characteristics** V_{OH} values modified**;** R_{PULLUP} value modified
		50	• **Table 5.3 Electrical Characteristics (Continued)** Measurement Condition and standard values for ICC added and some released
		52	• **Table 5.6 Flash Memory Version Electrical Characteristics** Word Program Time and Lock bit Program Time values modified; parameter All-Unlocked-Block-Erase Time deleted; note 1 deleted
		54	• **Table 5.10 Memory Expansion Mode and Microprocessor Mode** *tac1(RD-DB)* expression on note 1 modified; *tac2(RD-DB)* expression on note 1 added