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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	M32C/80
Core Size	16/32-Bit
Speed	32MHz
Connectivity	CANbus, EBI/EMI, I ² C, IEBus, IrDA, SIO, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	121
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	31K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 34x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30878fjagp-u5

Table 1.3 Specifications (100-Pin Package) (1/2)

Item	Function	Specification
CPU	Central processing unit	M32C/80 core (multiplier: 16 bits × 16 bits → 32 bits multiply-addition operation instructions: 16 × 16 + 48 → 48 bits) • Basic instructions: 108 • Minimum instruction execution time: 31.3 ns (f(CPU) = 32 MHz, VCC1 = 4.2 to 5.5 V) 41.7 ns (f(CPU) = 24 MHz, VCC1 = 3.0 to 5.5 V) • Operating mode: Single-chip mode, memory expansion mode, and microprocessor mode
Memory	ROM, RAM, data flash	See Tables 1.5 to 1.7 Product List .
Power Supply Voltage Detection		Vdet3 detection function, Vdet4 detection function, cold start/warm start determination function
External Bus Expansion	Bus/memory expansion function	• Address space: 16 Mbytes • External bus interface: 1 to 7 wait states can be inserted, 4 chip select outputs, 3 V and 5 V interfaces • Bus format: Switchable between separate bus and multiplexed bus formats, switchable data bus width (8-bit or 16-bit)
Clock	Clock generation circuits	• 4 circuits: Main clock, sub clock, on-chip oscillator, PLL frequency synthesizer • Oscillation stop detection: Main clock oscillation stop detection function • Frequency divider circuit: Dividing ratio selectable among 1, 2, 3, 4, 6, 8, 10, 12, 14, 16 • Low power consumption features: Wait mode, stop mode
Interrupts		• Interrupt vectors: 70 • External interrupt inputs: 11 ($\overline{\text{NMI}}$, $\overline{\text{INT}} \times 6$, key input × 4) • Interrupt priority levels: 7
Watchdog Timer		15-bit × 1 channel (with prescaler)
DMA	DMAC	• 4 channels, cycle steal method • Trigger sources: 43 • Transfer modes: 2 (single transfer and repeat transfer)
	DMACII	• Can be activated by all peripheral function interrupt sources • Transfer modes: 2 (single transfer and burst transfer) • Immediate transfer, calculation transfer, and chain transfer functions
Timer	Timer A	16-bit timer × 5 Timer mode, event counter mode, one-shot timer mode, pulse width modulation (PWM) mode, Event counter 2-phase pulse signal processing (2-phase encoder input) × 3
	Timer B	16-bit timer × 6 Timer mode, event counter mode, pulse period measurement mode, pulse width measurement mode
	Timer function for 3-phase motor control	3-phase inverter control × 1 (using timer A1, timer A2, timer A4, and timer B2) On-chip dead time timer

Table 1.4 Specifications (100-Pin Package) (2/2)

Item	Function	Specification
Serial Interface	UART0 to UART4	Clock synchronous/asynchronous × 5 I ² C bus, special mode 2, GCI mode, SIM mode, IrDA mode ⁽²⁾ , IEBus (optional) ⁽¹⁾⁽³⁾
	UART5	Clock synchronous/asynchronous × 1
A/D Converter		10-bit resolution × 26 channels (in single-chip mode) 10-bit resolution × 10 channels (in memory expansion mode and microprocessor mode) Including sample and hold function
D/A Converter		8-bit resolution × 2 channels
CRC Calculation Circuit		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) compliant
X/Y Converter		16 bits × 16 bits
Intelligent I/O		16-bit timer × 2 • Time measurement function (input capture): 8 channels • Waveform generation function (output compare): 10 channels • Communication function: Clock synchronous mode, clock asynchronous mode, HDLC data processing mode, IEBus (optional) ⁽¹⁾⁽³⁾ • 2-phase pulse signal processing (2-phase encoder input) × 1
ROM Correction Function		Address match interrupt × 8
CAN modules		Supporting CAN 2.0B specification M32C/87: 16 slots × 2 channels, M32C/87A: 16 slots × 1 channel M32C/87B: none
I/O Ports	Programmable I/O ports	• Input only: 1 • CMOS I/O: 85, selectable pull-up resistor • N channel open drain ports: 2
Flash Memory		• Erase and program voltage: 3.3 V ± 0.3 V or 5.0 V ± 0.5 V • Erase and program endurance: 100 times (all areas) • Program security: ROM code protect and ID code check • Debug functions: On-chip debug and on-board flash reprogram
Operating Frequency/Supply Voltage		32 MHz: VCC1 = 4.2 to 5.5 V, VCC2 = 3.0 V to VCC1 24 MHz: VCC1 = 3.0 to 5.5 V, VCC2 = 3.0 V to VCC1
Current Consumption		32 mA (32 MHz, VCC1 = VCC2 = 5 V) 23 mA (24 MHz, VCC1 = VCC2 = 3.3 V) 45 μA (approx. 1 MHz, VCC1 = VCC2 = 3.3 V, on-chip oscillator low-power consumption mode → wait mode) 0.8 μA (VCC1 = VCC2 = 3.3 V, stop mode)
Operating Ambient Temperature (°C)		-20 to 85°C, -40 to 85°C (optional) ⁽³⁾
Package		100-pin LQFP (PLQP0100KB-A) 100-pin QFP (PRQP0100JB-A)

NOTES:

1. IEBus is a registered trademark of NEC Electronics Corporation.
2. Available in UART0.
3. Please contact a Renesas sales office for optional features.

Table 1.13 100-Pin Package List of Pin Names (2/3)

Pin No.		Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
FP	GP								
41	39		P5_5						HOLD
42	40		P5_4						HLD $\overline{\text{A}}$ /ALE
43	41	CLKOUT	P5_3						BCLK/ALE
44	42		P5_2						RD
45	43		P5_1						WRH/BHE
46	44		P5_0						WRL/WR
47	45		P4_7						CS0/A23
48	46		P4_6						CS1/A22
49	47		P4_5						CS2/A21
50	48		P4_4						CS3/A20
51	49		P4_3						A19
52	50		P4_2						A18
53	51		P4_1						A17
54	52		P4_0						A16
55	53		P3_7						A15,[A15/D15]
56	54		P3_6						A14,[A14/D14]
57	55		P3_5						A13,[A13/D13]
58	56		P3_4						A12,[A12/D12]
59	57		P3_3						A11,[A11/D11]
60	58		P3_2						A10,[A10/D10]
61	59		P3_1						A9,[A9/D9]
62	60	VCC2							
63	61		P3_0						A8,[A8/D8]
64	62	VSS							
65	63		P2_7					AN2_7	A7,[A7/D7]
66	64		P2_6					AN2_6	A6,[A6/D6]
67	65		P2_5					AN2_5	A5,[A5/D5]
68	66		P2_4					AN2_4	A4,[A4/D4]
69	67		P2_3					AN2_3	A3,[A3/D3]
70	68		P2_2					AN2_2	A2,[A2/D2]
71	69		P2_1					AN2_1	A1,[A1/D1]
72	70		P2_0					AN2_0	A0,[A0/D0]

2.1.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.

Interrupts are disabled when the I flag is set to 0 and enabled when it is set to 1. The I flag becomes 0 when an interrupt request is acknowledged.

2.1.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0. USP is selected when the U flag is set to 1.

The U flag becomes 0 when a hardware interrupt request is acknowledged or the INT instruction specifying software interrupt numbers 0 to 31 is executed.

2.1.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has higher priority level than IPL, the interrupt is enabled.

2.1.8.10 Reserved Space

Only write 0 to bits assigned to the reserved space. When read, the bits return undefined values.

2.2 High-Speed Interrupt Registers

Registers associated with the high-speed interrupt are as follows:

- Flag save register (SVF)
- PC save register (SVP)
- Vector register (VCT)

2.3 DMAC-Associated Registers

Registers associated with the DMAC are as follows:

- DMA mode register (DMD0, DMD1)
- DMA transfer count register (DCT0, DCT1)
- DMA transfer count reload register (DRC0, DRC1)
- DMA memory address register (DMA0, DMA1)
- DMA memory address reload register (DRA0, DRA1)
- DMA SFR address register (DSA0, DSA1)

Table 4.2 SFR Address Map (2/20)

Address	Register	Symbol	After Reset
0030h			
0031h			
0032h			
0033h			
0034h			
0035h			
0036h			
0037h			
0038h	Address Match Interrupt Register 6	RMAD6	000000h
0039h			
003Ah			
003Bh	Address Match Interrupt Register 7	RMAD7	000000h
003Ch			
003Dh			
003Eh			
003Fh			
0040h			
0041h			
0042h			
0043h			
0044h			
0045h			
0046h			
0047h			
0048h	External Space Wait Control Register 0	EWCR0	X0X0 0011b
0049h	External Space Wait Control Register 1	EWCR1	X0X0 0011b
004Ah	External Space Wait Control Register 2	EWCR2	X0X0 0011b
004Bh	External Space Wait Control Register 3	EWCR3	X0X0 0011b
004Ch			
004Dh			
004Eh			
004Fh			
0050h			
0051h			
0052h			
0053h			
0054h			
0055h	Flash Memory Control Register 1	FMR1	0000 0X0Xb
0056h			
0057h	Flash Memory Control Register 0	FMR0	0000 0001b(Flash Memory) XXXX XXX0b(Mask ROM)
0058h			
0059h			
005Ah			
005Bh			
005Ch			
005Dh			
005Eh			
005Fh			

X: Undefined

Blank spaces are all reserved. No access is allowed.

Table 4.11 SFR Address Map (11/20)

Address	Register ⁽²⁾⁽³⁾	Symbol	After Reset
0250h	CAN1 Slot Buffer Select Register	C1SBS	00h ⁽¹⁾
0251h	CAN1 Control Register 1	C1CTLR1	X000 00XXb ⁽¹⁾
0252h	CAN1 Sleep Control Register	C1SLPR	XXXX XXX0b ⁽¹⁾
0253h			
0254h	CAN1 Acceptance Filter Support Register	C1AFS	0000 0000b ⁽¹⁾
0255h			0000 0001b ⁽¹⁾
0256h			
0257h			
0258h			
0259h			
025Ah			
025Bh			
025Ch			
025Dh			
025Eh			
025Fh			
0260h	CAN1 Message Slot Buffer 0 Standard ID0	C1SLOT0_0	XXh
0261h	CAN1 Message Slot Buffer 0 Standard ID1	C1SLOT0_1	XXh
0262h	CAN1 Message Slot Buffer 0 Extended ID0	C1SLOT0_2	XXh
0263h	CAN1 Message Slot Buffer 0 Extended ID1	C1SLOT0_3	XXh
0264h	CAN1 Message Slot Buffer 0 Extended ID2	C1SLOT0_4	XXh
0265h	CAN1 Message Slot Buffer 0 Data Length Code	C1SLOT0_5	XXh
0266h	CAN1 Message Slot Buffer 0 Data 0	C1SLOT0_6	XXh
0267h	CAN1 Message Slot Buffer 0 Data 1	C1SLOT0_7	XXh
0268h	CAN1 Message Slot Buffer 0 Data 2	C1SLOT0_8	XXh
0269h	CAN1 Message Slot Buffer 0 Data 3	C1SLOT0_9	XXh
026Ah	CAN1 Message Slot Buffer 0 Data 4	C1SLOT0_10	XXh
026Bh	CAN1 Message Slot Buffer 0 Data 5	C1SLOT0_11	XXh
026Ch	CAN1 Message Slot Buffer 0 Data 6	C1SLOT0_12	XXh
026Dh	CAN1 Message Slot Buffer 0 Data 7	C1SLOT0_13	XXh
026Eh	CAN1 Message Slot Buffer 0 Time Stamp High-Order	C1SLOT0_14	XXh
026Fh	CAN1 Message Slot Buffer 0 Time Stamp Low-Order	C1SLOT0_15	XXh
0270h	CAN1 Message Slot Buffer 1 Standard ID0	C1SLOT1_0	XXh
0271h	CAN1 Message Slot Buffer 1 Standard ID1	C1SLOT1_1	XXh
0272h	CAN1 Message Slot Buffer 1 Extended ID0	C1SLOT1_2	XXh
0273h	CAN1 Message Slot Buffer 1 Extended ID1	C1SLOT1_3	XXh
0274h	CAN1 Message Slot Buffer 1 Extended ID2	C1SLOT1_4	XXh
0275h	CAN1 Message Slot Buffer 1 Data Length Code	C1SLOT1_5	XXh
0276h	CAN1 Message Slot Buffer 1 Data 0	C1SLOT1_6	XXh
0277h	CAN1 Message Slot Buffer 1 Data 1	C1SLOT1_7	XXh
0278h	CAN1 Message Slot Buffer 1 Data 2	C1SLOT1_8	XXh
0279h	CAN1 Message Slot Buffer 1 Data 3	C1SLOT1_9	XXh
027Ah	CAN1 Message Slot Buffer 1 Data 4	C1SLOT1_10	XXh
027Bh	CAN1 Message Slot Buffer 1 Data 5	C1SLOT1_11	XXh
027Ch	CAN1 Message Slot Buffer 1 Data 6	C1SLOT1_12	XXh
027Dh	CAN1 Message Slot Buffer 1 Data 7	C1SLOT1_13	XXh
027Eh	CAN1 Message Slot Buffer 1 Time Stamp High-Order	C1SLOT1_14	XXh
027Fh	CAN1 Message Slot Buffer 1 Time Stamp Low-Order	C1SLOT1_15	XXh

X: Undefined

Blank spaces are all reserved. No access is allowed.

NOTES:

1. Values are obtained by setting the SLEEP bit in the C1SLPR register to "1" (sleep mode exited) after reset and supplying a clock to the CAN module.
2. The CAN-associated registers (allocated in addresses 01E0h to 02BFh) cannot be used in M32C/87B. In M32C/87A, only CAN0-associated registers can be used.
3. Set the PM13 bit in the PM1 register to 1 (2 wait states for SFR area) before accessing the CAN-associated registers.

Table 4.12 SFR Address Map (12/20)

Address	Register ⁽³⁾⁽⁴⁾	Symbol	After Reset
0280h	CAN1 Control Register 0	C1CTLR0	XX01 0X01b ⁽²⁾
0281h			XXXX 0000b ⁽²⁾
0282h	CAN1 Status Register	C1STR	0000 0000b ⁽²⁾
0283h			X000 0X01b ⁽²⁾
0284h	CAN1 Extended ID Register	C1IDR	0000h ⁽²⁾
0285h			
0286h	CAN1 Configuration Register	C1CONR	0000 XXXXb ⁽²⁾
0287h			0000 0000b ⁽²⁾
0288h	CAN1 Time Stamp Register	C1TSR	0000h ⁽²⁾
0289h			
028Ah	CAN1 Transmit Error Count Register	C1TEC	00h ⁽²⁾
028Bh	CAN1 Receive Error Count Register	C1REC	00h ⁽²⁾
028Ch	CAN1 Slot Interrupt Status Register	C1SISTR	0000h ⁽²⁾
028Dh			
028Eh			
028Fh			
0290h	CAN1 Slot Interrupt Mask Register	C1SIMKR	0000h ⁽²⁾
0291h			
0292h			
0293h			
0294h	CAN1 Error Interrupt Mask Register	C1EIMKR	XXXX X000b ⁽²⁾
0295h	CAN1 Error Interrupt Status Register	C1EISTR	XXXX X000b ⁽²⁾
0296h	CAN1 Error Source Register	C1EFR	00h ⁽²⁾
0297h	CAN1 Baud Rate Prescaler	C1BRP	0000 0001b ⁽²⁾
0298h			
0299h	CAN1 Mode Register	C1MDR	XXXX XX00b ⁽²⁾
029Ah			
029Bh			
029Ch			
029Dh			
029Eh			
029Fh			
02A0h	CAN1 Single Shot Control Register	C1SSCTLR	0000h ⁽¹⁾⁽²⁾
02A1h			
02A2h			
02A3h			
02A4h	CAN1 Single Shot Status Register	C1SSSTR	0000h ⁽¹⁾⁽²⁾
02A5h			
02A6h			
02A7h			
02A8h	CAN1 Global Mask Register Standard ID0	C1GMR0	XXX0 0000b ⁽¹⁾⁽²⁾
02A9h	CAN1 Global Mask Register Standard ID1	C1GMR1	XX00 0000b ⁽¹⁾⁽²⁾
02AAh	CAN1 Global Mask Register Extended ID0	C1GMR2	XXXX 0000b ⁽¹⁾⁽²⁾
02ABh	CAN1 Global Mask Register Extended ID1	C1GMR3	00h ⁽¹⁾⁽²⁾
02ACh	CAN1 Global Mask Register Extended ID2	C1GMR4	XX00 0000b ⁽¹⁾⁽²⁾
02ADh			
02AEh			
02AFh			

X: Undefined

Blank spaces are all reserved. No access is allowed.

NOTES:

1. The BANKSEL bit in the C0CTLR1 register can switch functions for addresses 02A0h to 02BFh.
2. Values are obtained by setting the SLEEP bit in the C1SLPR register to "1" (sleep mode exited) after reset and supplying a clock to the CAN module.
3. The CAN-associated registers (allocated in addresses 01E0h to 02BFh) cannot be used in M32C/87B. In M32C/87A, only CAN0-associated registers can be used.
4. Set the PM13 bit in the PM1 register to 1 (2 wait states for SFR area) before accessing the CAN-associated registers.

Table 4.20 SFR Address Map (20/20)

Address	Register	Symbol	After Reset
03D0h	Port P14 Register ⁽¹⁾	P14	XXh
03D1h	Port P15 Register ⁽¹⁾	P15	XXh
03D2h	Port P14 Direction Register ⁽¹⁾⁽²⁾	PD14	X000 0000b
03D3h	Port P15 Direction Register ⁽¹⁾⁽²⁾	PD15	00h
03D4h			
03D5h			
03D6h			
03D7h			
03D8h			
03D9h			
03DAh	Pull-Up Control Register 2	PUR2	00h
03DBh	Pull-Up Control Register 3	PUR3	00h
03DCh	Pull-Up Control Register 4 ⁽¹⁾⁽³⁾	PUR4	XXXX 0000b
03DDh			
03DEh			
03DFh			
03E0h	Port P0 Register	P0	XXh
03E1h	Port P1 Register	P1	XXh
03E2h	Port P0 Direction Register	PD0	00h
03E3h	Port P1 Direction Register	PD1	00h
03E4h	Port P2 Register	P2	XXh
03E5h	Port P3 Register	P3	XXh
03E6h	Port P2 Direction Register	PD2	00h
03E7h	Port P3 Direction Register	PD3	00h
03E8h	Port P4 Register	P4	XXh
03E9h	Port P5 Register	P5	XXh
03EAh	Port P4 Direction Register	PD4	00h
03EBh	Port P5 Direction Register	PD5	00h
03ECh			
03EDh			
03EEh			
03EFh			
03F0h	Pull-Up Control Register 0	PUR0	00h
03F1h	Pull-Up Control Register 1	PUR1	XXXX 0000b
03F2h			
03F3h			
03F4h			
03F5h			
03F6h			
03F7h			
03F8h			
03F9h			
03FAh			
03FBh			
03FCh			
03FDh			
03FEh			
03FFh	Port Control Register	PCR	XXXX X000b

X: Undefined

Blank spaces are all reserved. No access is allowed.

NOTES:

1. These registers cannot be used in the 100-pin package.
2. Set to FFh in the 100-pin package.
3. Set to 00h in the 100-pin package.

$$VCC1 = VCC2 = 5V$$

Table 5.6 Electrical Characteristics (2/3)

(VCC1 = VCC2 = 4.2 to 5.5 V, VSS = 0 V, Topr = -20 to 85°C, f(CPU) = 32 MHz unless otherwise specified)

Symbol	Parameter		Measurement Condition	Standard			Unit
				Min.	Typ.	Max.	
I _{IH}	Input high "H" current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7 ⁽¹⁾ , XIN, RESET, CNVSS, BYTE	V _I = 5 V			5.0	μA
I _{IL}	Input low "L" current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7 ⁽¹⁾ , XIN, RESET, CNVSS, BYTE	V _I = 0V			-5.0	μA
RPULLUP	Pull-up resistance	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7 ⁽¹⁾	V _I = 0V	30	50	167	kΩ
R _{fXIN}	Feedback resistance	XIN			1.5		MΩ
R _{fXCIN}	Feedback resistance	XCIN			10		MΩ
VRAM	RAM data retention voltage	In stop mode		2.0			V

NOTE:

1. P11 to P15 are provided in the 144-pin package only.

$$VCC1 = VCC2 = 5V$$

**Table 5.10 Flash Memory Electrical Characteristics (VCC1 = 4.5 V to 5.5 V, 3.0 to 3.6 V,
Topr = 0 to 60°C unless otherwise specified)**

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
–	Erase and program endurance ⁽¹⁾		100			times
–	Word program time (16 bits) (VCC1 = 5.0 V, Topr = 25°C)			25	300	μs
–	Lock bit program time			25	300	μs
–	Block erase time (VCC1 = 5.0 V, Topr = 25°C)	4-Kbyte block		0.3	4	s
		8-Kbyte block		0.3	4	s
		32-Kbyte block		0.5	4	s
		64-Kbyte block		0.8	4	s
tps	Wait time to stabilize flash memory circuit				15	μs
–	Data hold time (Topr = -40 to 85°C)		10			years

NOTE:

1. If erase and program endurance is n times (n = 100), each block can be erased n times. For example, if a 4-Kbyte block A is erased after programming a word data 2,048 times, each to a different address, this counts as one erase and program time. Data can not be programmed to the same address more than once without erasing the block. (rewrite prohibited)

$$VCC1 = VCC2 = 5V$$

Timing Requirements

(VCC1 = VCC2 = 4.2 to 5.5 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.13 External Clock Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc	External clock input cycle time	31.25		ns
tw(H)	External clock input high ("H") pulse width	13.75		ns
tw(L)	External clock input low ("L") pulse width	13.75		ns
tr	External clock rise time		5	ns
tf	External clock fall time		5	ns

Table 5.14 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	100		ns
tw(TAH)	TAiIN input high ("H") pulse width	40		ns
tw(TAL)	TAiIN input low ("L") pulse width	40		ns

i = 0 to 4

Table 5.15 Timer A Input (Gate Signal Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	400		ns
tw(TAH)	TAiIN input high ("H") pulse width	200		ns
tw(TAL)	TAiIN input low ("L") pulse width	200		ns

i = 0 to 4

Table 5.16 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	200		ns
tw(TAH)	TAiIN input high ("H") pulse width	100		ns
tw(TAL)	TAiIN input low ("L") pulse width	100		ns

i = 0 to 4

Table 5.17 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tw(TAH)	TAiIN input high ("H") pulse width	100		ns
tw(TAL)	TAiIN input low ("L") pulse width	100		ns

i = 0 to 4

$$VCC1 = VCC2 = 5V$$

Timing Requirements

(VCC1 = VCC2 = 4.2 to 5.5 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.18 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(UP)	TAiOUT input cycle time	2000		ns
tw(UPH)	TAiOUT input high ("H") pulse width	1000		ns
tw(UPL)	TAiOUT input low ("L") pulse width	1000		ns
tsu(UP-TIN)	TAiOUT input setup time	400		ns
th(TIN-UP)	TAiOUT input hold time	400		ns

i = 0 to 4

Table 5.19 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	800		ns
tsu(TAIN-TAOUT)	TAiOUT input setup time	200		ns
tsu(TAOUT-TAIN)	TAiIN input setup time	200		ns

i = 0 to 4

Table 5.20 Timer B Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TB)	TBiIN input cycle time (counted on one edge)	100		ns
tw(TBH)	TBiIN input high ("H") pulse width (counted on one edge)	40		ns
tw(TBL)	TBiIN input low ("L") pulse width (counted on one edge)	40		ns
tc(TB)	TBiIN input cycle time (counted on both edges)	200		ns
tw(TBH)	TBiIN input high ("H") pulse width (counted on both edges)	80		ns
tw(TBL)	TBiIN input low ("L") pulse width (counted on both edges)	80		ns

i = 0 to 5

Table 5.21 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TB)	TBiIN input cycle time	400		ns
tw(TBH)	TBiIN input high ("H") pulse width	200		ns
tw(TBL)	TBiIN input low ("L") pulse width	200		ns

i = 0 to 5

Table 5.22 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TB)	TBiIN input cycle time	400		ns
tw(TBH)	TBiIN input high ("H") pulse width	200		ns
tw(TBL)	TBiIN input low ("L") pulse width	200		ns

i = 0 to 5

$$VCC1 = VCC2 = 5V$$

Timing Requirements

(VCC1 = VCC2 = 4.2 to 5.5 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.27 External Interrupt $\overline{INTi}$ Input (Edge Sensitive)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tw(INH)	$\overline{INTi}$ input high ("H") pulse width	250		ns
tw(INL)	$\overline{INTi}$ input low ("L") pulse width	250		ns

i = 0 to 8⁽¹⁾

NOTE:

1. $\overline{INT6}$ to $\overline{INT8}$ are provided in the 144-pin package only.

$$VCC1 = VCC2 = 5V$$

Switching Characteristics

(VCC1 = VCC2 = 4.2 to 5.5 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.29 Memory Expansion Mode and Microprocessor Mode (when accessing external memory space)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min.	Max.	
td(BCLK-AD)	Address output delay time	See Figure 5.2		18	ns
th(BCLK-AD)	Address output hold time (BCLK standard)		-3		ns
th(RD-AD)	Address output hold time (RD standard) ⁽³⁾		0		ns
th(WR-AD)	Address output hold time (WR standard) ⁽³⁾		(note 1)		ns
td(BCLK-CS)	Chip-select signal output delay time			18	ns
th(BCLK-CS)	Chip-select signal output hold time (BCLK standard)		-3		ns
th(RD-CS)	Chip-select signal output hold time (RD standard) ⁽³⁾		0		ns
th(WR-CS)	Chip-select signal output hold time (WR standard) ⁽³⁾		(note 1)		ns
td(BCLK-RD)	RD signal output delay time			18	ns
th(BCLK-RD)	RD signal output hold time		-5		ns
td(BCLK-WR)	WR signal output delay time			18	ns
th(BCLK-WR)	WR signal output hold time		-5		ns
td(DB-WR)	Data output delay time (WR standard)		(note 2)		ns
th(WR-DB)	Data output hold time (WR standard) ⁽³⁾		(note 1)		ns
tw(WR)	WR output width		(note 2)		ns

NOTES:

- Values, which depend on BCLK frequency, can be obtained from the following equations.

$$th(WR-DB) = \frac{10^9}{f(BCLK) \times 2} - 15 \text{ [ns]}$$

$$th(WR-AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \text{ [ns]}$$

$$th(WR-CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \text{ [ns]}$$

- Values, which depend on BCLK frequency and external bus cycles, can be obtained from the following equations.

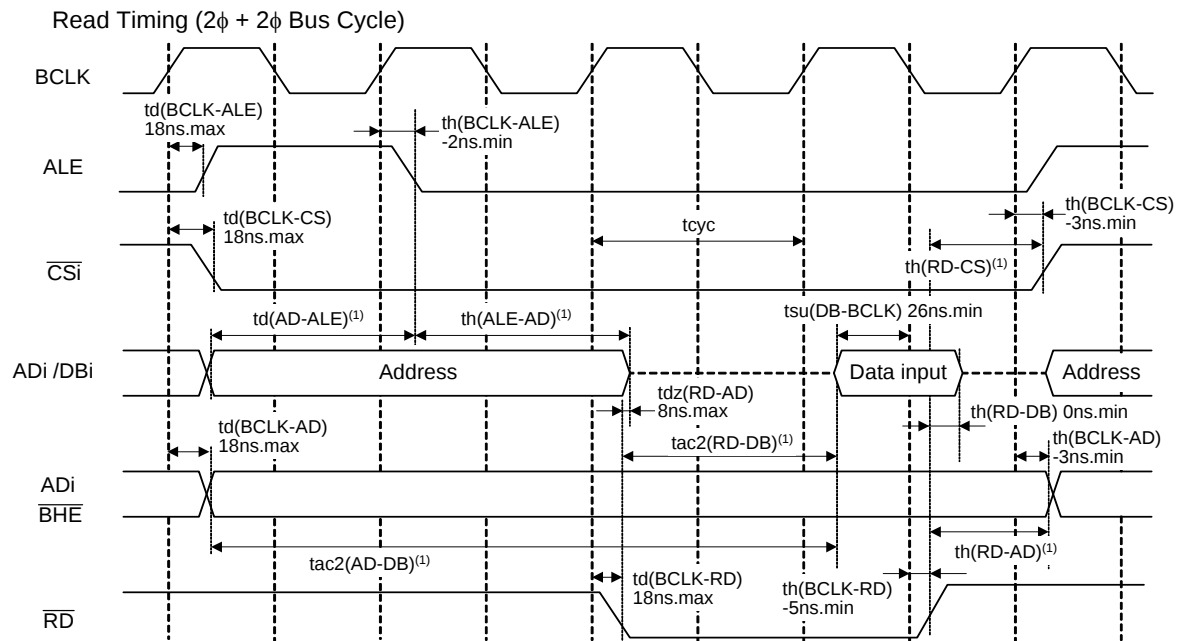
$$td(DB-WR) = \frac{10^9 \times m}{f(BCLK)} - 20 \text{ [ns]} \text{ (if external bus cycle is } a\phi + b\phi, m = b)$$

$$tw(WR) = \frac{10^9 \times n}{f(BCLK) \times 2} - 15 \text{ [ns]} \text{ (if external bus cycle is } a\phi + b\phi, n = (b \times 2) - 1)$$

- tc [ns] is added when recovery cycle is inserted.

Memory Expansion Mode and Microprocessor Mode (when accessing an external memory space with the multiplexed bus)

VCC1=VCC2=5V



NOTES:

1. Varies with operation frequency:

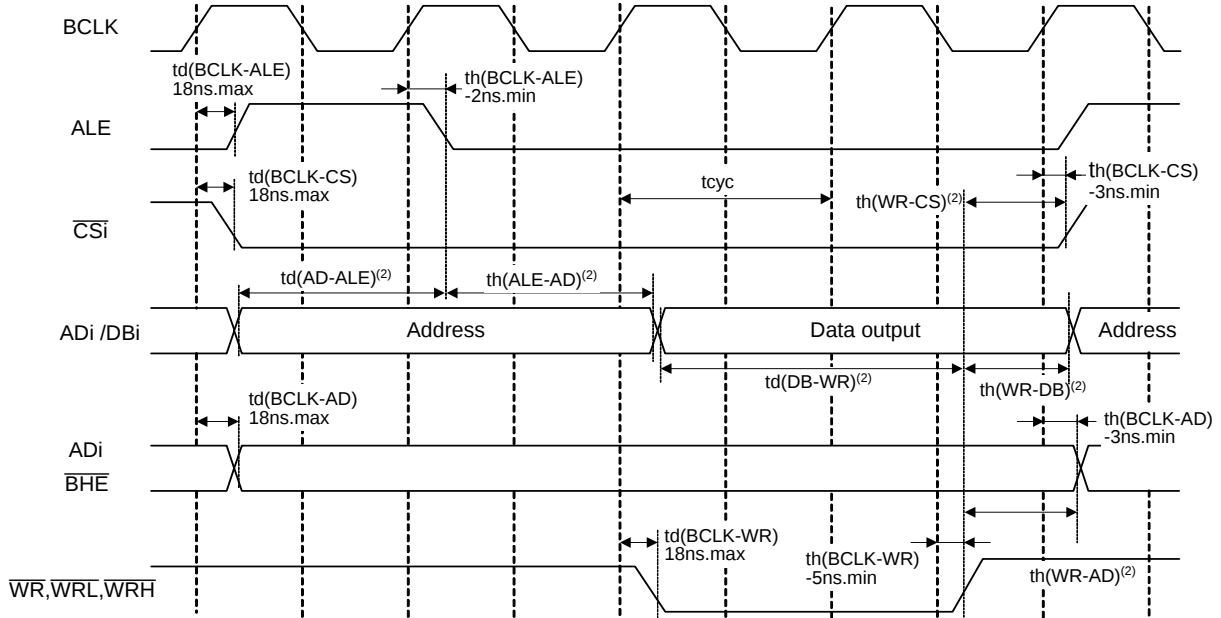
$$td(AD-ALE) = (tcyc / 2 \times n - 20) \text{ ns.min (if external bus cycle } a\phi + b\phi, n = a)$$

$$th(ALE-AD) = (tcyc / 2 \times n - 20) \text{ ns.min (if external bus cycle } a\phi + b\phi, n = a)$$

$$th(RD-AD) = (tcyc / 2 - 10) \text{ ns.min, } th(RD-CS) = (tcyc / 2 - 10) \text{ ns.min}$$

$$tac2(RD-DB) = (tcyc / 2 \times m - 35) \text{ ns.max (if external bus cycle } a\phi + b\phi, m = (b \times 2) - 1)$$

$$tac2(AD-DB) = (tcyc / 2 \times p - 35) \text{ ns.max (if external bus cycle } a\phi + b\phi, p = \{(a + b - 1) \times 2\} + 1)$$

Write Timing ($2\phi + 2\phi$ Bus Cycle)

NOTES:

1. Varies with operation frequency:

$$td(AD-ALE) = (tcyc / 2 \times n - 20) \text{ ns.min (if external bus cycle } a\phi + b\phi, n = a)$$

$$th(ALE-AD) = (tcyc / 2 \times n - 20) \text{ ns.min (if external bus cycle } a\phi + b\phi, n = a)$$

$$th(WR-AD) = (tcyc / 2 - 10) \text{ ns.min, } th(WR-CS) = (tcyc / 2 - 10) \text{ ns.min}$$

$$th(WR-DB) = (tcyc / 2 - 15) \text{ ns.min}$$

$$td(DB-WR) = (tcyc / 2 \times m - 25) \text{ ns.min (if external bus cycle } a\phi + b\phi, m = (b \times 2) - 1)$$

$$tcyc = \frac{10^9}{f(BCLK)}$$

Measurement Conditions:

- VCC1 = VCC2 = 4.2 to 5.5 V

- Input high and low voltage $V_{IH} = 2.5 \text{ V}$, $V_{IL} = 0.8 \text{ V}$ - Output high and low voltage $V_{OH} = 2.0 \text{ V}$, $V_{OL} = 0.8 \text{ V}$

Figure 5.6 VCC1 = VCC2 = 5 V Timing Diagram (4/4)

$$VCC1 = VCC2 = 3.3\text{ V}$$

Timing Requirements

(VCC1 = VCC2 = 3.0 to 3.6 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.46 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(AD)	ADTRG input cycle time (required for trigger)	1000		ns
tw(ADL)	ADTRG input low ("L") pulse width	125		ns

Table 5.47 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CK)	CLKi input cycle time	200		ns
tw(CKH)	CLKi input high ("H") pulse width	100		ns
tw(CKL)	CLKi input low ("L") pulse width	100		ns
td(C-Q)	TXDi output delay time		80	ns
th(C-Q)	TXDi output hold time	0		ns
tsu(D-C)	RXDi input setup time	70		ns
th(C-D)	RXDi input hold time	90		ns

i = 0 to 6

Table 5.48 Intelligent I/O Communication Function (Groups 0 and 1)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CK)	ISCLKi input cycle time	600		ns
tw(CKH)	ISCLKi input high ("H") pulse width	300		ns
tw(CKL)	ISCLKi input low ("L") pulse width	300		ns
td(C-Q)	ISTXDi output delay time		100	ns
th(C-Q)	ISTXDi output hold time	0		ns
tsu(D-C)	ISRXDi input setup time	100		ns
th(C-D)	ISRXDi input hold time	100		ns

i = 0, 1

Table 5.49 Intelligent I/O Communication Function (Group 2)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CK)	ISCLK2 input cycle time	600		ns
tw(CKH)	ISCLK2 input high ("H") pulse width	300		ns
tw(CKL)	ISCLK2 input low ("L") pulse width	300		ns
td(C-Q)	ISTXD2 output delay time		180	ns
th(C-Q)	ISTXD2 output hold time	0		ns
tsu(D-C)	ISRXD2 input setup time	150		ns
th(C-D)	ISRXD2 input hold time	100		ns

$$VCC1 = VCC2 = 3.3 \text{ V}$$

Timing Requirements

(VCC1 = VCC2 = 3.0 to 3.6 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.50 External Interrupt $\overline{INTi}$ Input (Edge Sensitive)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tw(INH)	$\overline{INTi}$ input high ("H") pulse width	250		ns
tw(INL)	$\overline{INTi}$ input low ("L") pulse width	250		ns

i = 0 to 8⁽¹⁾

NOTE:

1. $\overline{INT6}$ to $\overline{INT8}$ are provided in the 144-pin package only.

$$VCC1 = VCC2 = 3.3 \text{ V}$$

Switching Characteristics

(VCC1 = VCC2 = 3.0 to 3.6 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.52 Memory Expansion Mode and Microprocessor Mode (when accessing external memory space)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min.	Max.	
td(BCLK-AD)	Address output delay time	See Figure 5.2		18	ns
th(BCLK-AD)	Address output hold time (BCLK standard)		-3		ns
th(RD-AD)	Address output hold time (RD standard) ⁽³⁾		0		ns
th(WR-AD)	Address output hold time (WR standard) ⁽³⁾		(note 1)		ns
td(BCLK-CS)	Chip-select signal output delay time			18	ns
th(BCLK-CS)	Chip-select signal output hold time (BCLK standard)		-3		ns
th(RD-CS)	Chip-select signal output hold time (RD standard) ⁽³⁾		0		ns
th(WR-CS)	Chip-select signal output hold time (WR standard) ⁽³⁾		(note 1)		ns
td(BCLK-RD)	RD signal output delay time			18	ns
th(BCLK-RD)	RD signal output hold time		-5		ns
td(BCLK-WR)	WR signal output delay time			18	ns
th(BCLK-WR)	WR signal output hold time		0		ns
td(DB-WR)	Data output delay time (WR standard)		(note 2)		ns
th(WR-DB)	Data output hold time (WR standard) ⁽³⁾		(note 1)		ns
tw(WR)	WR output width		(note 2)		ns

NOTES:

- Values, which depend on BCLK frequency, can be obtained from the following equations.

$$th(WR-DB) = \frac{10^9}{f(BCLK) \times 2} - 20 \text{ [ns]}$$

$$th(WR-AD) = \frac{10^9}{f(BCLK) \times 2} - 15 \text{ [ns]}$$

$$th(WR-CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \text{ [ns]}$$

- Values, which depend on BCLK frequency and external bus cycles, can be obtained from the following equations.

$$td(DB-WR) = \frac{10^9 \times m}{f(BCLK)} - 20 \text{ [ns]} \text{ (if external bus cycle is } a\phi + b\phi, m = b)$$

$$tw(WR) = \frac{10^9 \times n}{f(BCLK) \times 2} - 15 \text{ [ns]} \text{ (if external bus cycle is } a\phi + b\phi, n = (b \times 2) - 1)$$

- tc [ns] is added when recovery cycle is inserted.

Appendix 1. Package Dimensions

