Renesas Electronics America Inc - M30878FJBGP#U3 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	M32C/80
Core Size	16/32-Bit
Speed	32MHz
Connectivity	EBI/EMI, I²C, IEBus, IrDA, SIO, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	121
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	31K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 34x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30878fjbgp-u3

Table 1.2 Specifications (144-Pin Package) (2/2)

Item	Function	Specification
Serial Interface	UART0 to UART4	Clock synchronous/asynchronous × 5 I^2C bus, special mode 2, GCI mode, SIM mode, IrDA mode(2), IEBus (optional)(1)(3)
	UART5, UART6	Clock synchronous/asynchronous × 2
A/D Converter		10-bit resolution × 34 channels (in single-chip mode) 10-bit resolution × 18 channels (in memory expansion mode and microprocessor mode) Including sample and hold function
D/A Converter		8-bit resolution × 2 channels
CRC Calculation Circuit		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) compliant
X/Y Converter		16 bits x 16 bits
Intelligent I/O		16-bit timer × 2 • Time measurement function (input capture): 8 channels • Waveform generation function (output compare): 16 channels • Communication function: Clock synchronous mode, clock asynchronous mode, HDLC data processing mode, IEBus (optional)(1)(3) • 2-phase pulse signal processing (2-phase encoder input) × 1
ROM Correction Function		Address match interrupt × 8
CAN modules		Supporting CAN 2.0B specification M32C/87: 16 slots × 2 channels, M32C/87A: 16 slots × 1 channel M32C/87B: none
I/O Ports	Programmable I/O ports	• Input only: 1 • CMOS I/O: 121 with selectable pull-up resistor • N channel open drain ports: 2
Flash Memory		• Erase and program voltage: 3.3 V ± 0.3 V or 5.0 V ± 0.5 V • Erase and program endurance: 100 times (all areas) • Program security: ROM code protect and ID code check • Debug functions: On-chip debug and on-board flash reprogram
Operating Frequency/Supply Voltage		32 MHz: VCC1 = 4.2 to 5.5 V, VCC2 = 3.0 V to VCC1 24 MHz: VCC1 = 3.0 to 5.5 V, VCC2 = 3.0 V to VCC1
Current Consumption		32 mA (32 MHz, VCC1 = VCC2 = 5 V) 23 mA (24 MHz, VCC1 = VCC2 = 3.3 V) 45 μA (approx. 1 MHz, VCC1 = VCC2 = 3.3 V, on-chip oscillator low-power consumption mode → wait mode) 0.8 μA (VCC1 = VCC2 = 3.3 V, stop mode)
Operating Ambient Temperature (°C)		-20 to 85°C, -40 to 85°C (optional)(3)
Package		144-pin LQFP (PLQP0144KA-A)

NOTES:
1. IEBus is a registered trademark of NEC Electronics Corporation.
2. Available in UART0.
3. Please contact a Renesas sales office for optional features.

Table 1.3 Specifications (100-Pin Package) (1/2)

Item	Function	Specification
CPU	Central processing unit	M32C/80 core (multiplier: 16 bits × 16 bits → 32 bits multiply-addition operation instructions: 16 × 16 + 48 → 48 bits) • Basic instructions: 108 • Minimum instruction execution time: 31.3 ns (f(CPU) = 32 MHz, VCC1 = 4.2 to 5.5 V) 41.7 ns (f(CPU) = 24 MHz, VCC1 = 3.0 to 5.5 V) • Operating mode: Single-chip mode, memory expansion mode, and microprocessor mode
Memory	ROM, RAM, data flash	See **Tables 1.5 to 1.7 Product List**.
Power Supply Voltage Detection		Vdet3 detection function, Vdet4 detection function, cold start/warm start determination function
External Bus Expansion	Bus/memory expansion function	• Address space: 16 Mbytes • External bus interface: 1 to 7 wait states can be inserted, 4 chip select outputs, 3 V and 5 V interfaces • Bus format: Switchable between separate bus and multiplexed bus formats, switchable data bus width (8-bit or 16-bit)
Clock	Clock generation circuits	• 4 circuits: Main clock, sub clock, on-chip oscillator, PLL frequency synthesizer • Oscillation stop detection: Main clock oscillation stop detection function • Frequency divider circuit: Dividing ratio selectable among 1, 2, 3, 4, 6, 8, 10, 12, 14, 16 • Low power consumption features: Wait mode, stop mode
Interrupts		• Interrupt vectors: 70 • External interrupt inputs: 11 ($\overline{\text{NMI}}$, $\overline{\text{INT}}$ × 6, key input × 4) • Interrupt priority levels: 7
Watchdog Timer		15-bit × 1 channel (with prescaler)
DMA	DMAC	• 4 channels, cycle steal method • Trigger sources: 43 • Transfer modes: 2 (single transfer and repeat transfer)
	DMACII	• Can be activated by all peripheral function interrupt sources • Transfer modes: 2 (single transfer and burst transfer) • Immediate transfer, calculation transfer, and chain transfer functions
Timer	Timer A	16-bit timer × 5 Timer mode, event counter mode, one-shot timer mode, pulse width modulation (PWM) mode, Event counter 2-phase pulse signal processing (2-phase encoder input) × 3
	Timer B	16-bit timer × 6 Timer mode, event counter mode, pulse period measurement mode, pulse width measurement mode
	Timer function for 3-phase motor control	3-phase inverter control × 1 (using timer A1, timer A2, timer A4, and timer B2) On-chip dead time timer

Table 1.4 Specifications (100-Pin Package) (2/2)

Item	Function	Specification
Serial Interface	UART0 to UART4	Clock synchronous/asynchronous × 5 I^2C bus, special mode 2, GCI mode, SIM mode, IrDA mode(2), IEBus (optional)(1)(3)
	UART5	Clock synchronous/asynchronous × 1
A/D Converter		10-bit resolution × 26 channels (in single-chip mode) 10-bit resolution × 10 channels (in memory expansion mode and microprocessor mode) Including sample and hold function
D/A Converter		8-bit resolution × 2 channels
CRC Calculation Circuit		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) compliant
X/Y Converter		16 bits x 16 bits
Intelligent I/O		16-bit timer × 2 • Time measurement function (input capture): 8 channels • Waveform generation function (output compare): 10 channels • Communication function: Clock synchronous mode, clock asynchronous mode, HDLC data processing mode, IEBus (optional)(1)(3) • 2-phase pulse signal processing (2-phase encoder input) × 1
ROM Correction Function		Address match interrupt × 8
CAN modules		Supporting CAN 2.0B specification M32C/87: 16 slots × 2 channels, M32C/87A: 16 slots × 1 channel M32C/87B: none
I/O Ports	Programmable I/O ports	• Input only: 1 • CMOS I/O: 85, selectable pull-up resistor • N channel open drain ports: 2
Flash Memory		• Erase and program voltage: 3.3 V ± 0.3 V or 5.0 V ± 0.5 V • Erase and program endurance: 100 times (all areas) • Program security: ROM code protect and ID code check • Debug functions: On-chip debug and on-board flash reprogram
Operating Frequency/Supply Voltage		32 MHz: VCC1 = 4.2 to 5.5 V, VCC2 = 3.0 V to VCC1 24 MHz: VCC1 = 3.0 to 5.5 V, VCC2 = 3.0 V to VCC1
Current Consumption		32 mA (32 MHz, VCC1 = VCC2 = 5 V) 23 mA (24 MHz, VCC1 = VCC2 = 3.3 V) 45 μA (approx. 1 MHz, VCC1 = VCC2 = 3.3 V, on-chip oscillator low-power consumption mode → wait mode) 0.8 μA (VCC1 = VCC2 = 3.3 V, stop mode)
Operating Ambient Temperature (°C)		-20 to 85°C, -40 to 85°C (optional)(3)
Package		100-pin LQFP (PLQP0100KB-A) 100-pin QFP (PRQP0100JB-A)

NOTES:
1. IEBus is a registered trademark of NEC Electronics Corporation.
2. Available in UART0.
3. Please contact a Renesas sales office for optional features.

Table 1.7 M32C/87 Group (3) (M32C/87B: no CAN module) Current as of Jul. 2008

Part Number	Package Code	ROM Capacity	RAM Capacity	Remarks
M3087BFLBGP	PLQP0144KA-A (144P6Q-A)	1 MB + 4 KB(1)	48 KB	Flash memory
M30879FLBFP	PRQP0100JB-A (100P6S-A)			
M30879FLBGP	PLQP0100KB-A (100P6Q-A)			
M3087BFKBGP	PLQP0144KA-A (144P6Q-A)	768 KB + 4 KB(1)		
M30879FKBGP	PLQP0100KB-A (100P6Q-A)			
M30878FJBGP	PLQP0144KA-A (144P6Q-A)	512 KB + 4 KB(1)	31 KB	
M30876FJBGP	PLQP0100KB-A (100P6Q-A)			
M30875FHBGP	PLQP0144KA-A (144P6Q-A)	384 KB + 4 KB(1)	24 KB	
M30873FHBGP	PLQP0100KB-A (100P6Q-A)			
M30878MJB-XXXGP	PLQP0144KA-A (144P6Q-A)	512 KB	31 KB	Mask ROM
M30876MJB-XXXFP	PRQP0100JB-A (100P6S-A)			
M30876MJB-XXXGP	PLQP0100KB-A (100P6Q-A)			
M30875MHB-XXXGP	PLQP0144KA-A (144P6Q-A)	384 KB	24 KB	
M30873MHB-XXXGP	PLQP0100KB-A (100P6Q-A)			

NOTE:
1. Additional 4-Kbyte space is available for data flash memory.

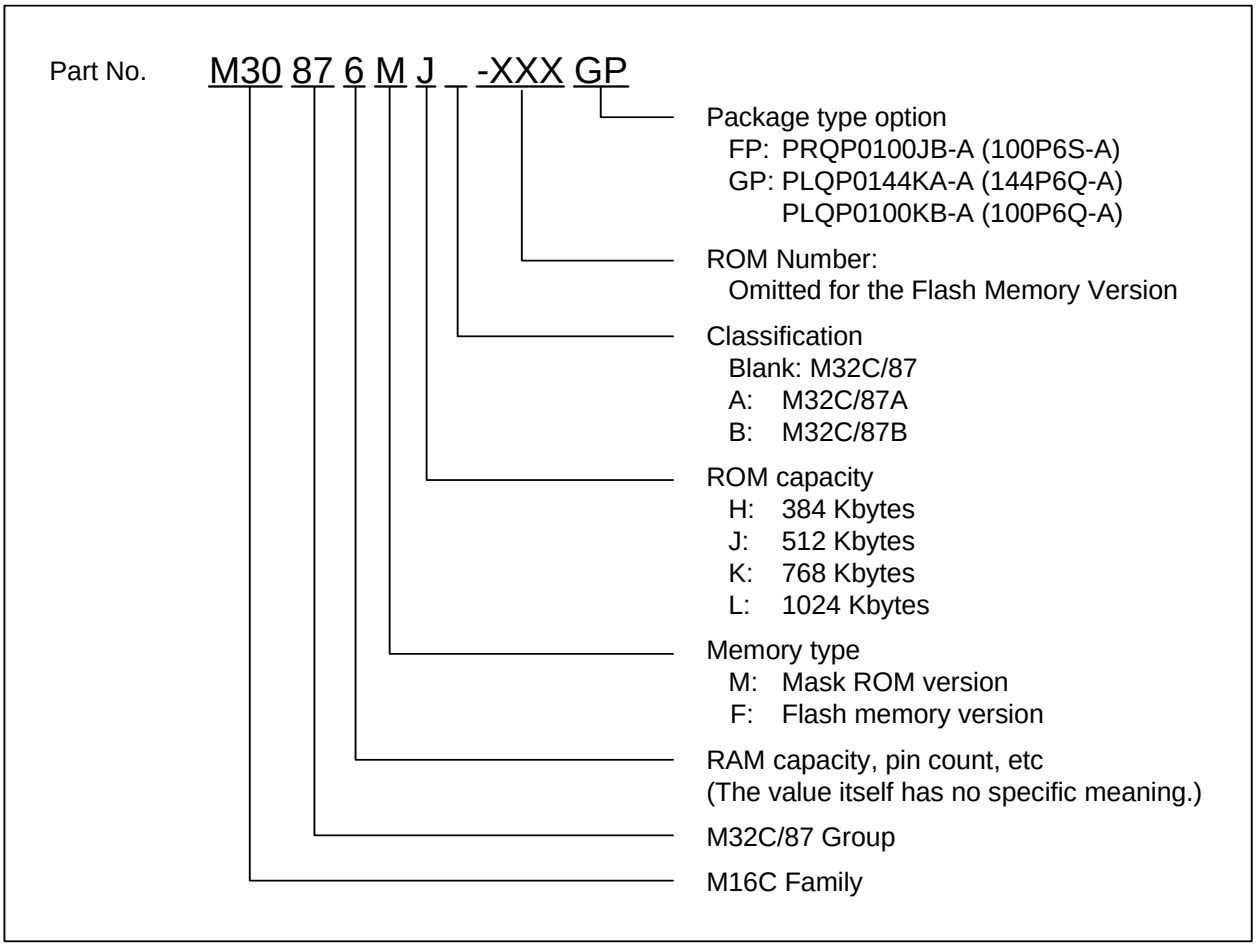


Figure 1.1 Product Numbering System

Table 1.8 144-Pin Package List of Pin Names (1/4)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin(1)	Intelligent I/O Pin	Analog Pin	Bus Control Pin
1		P9_6			TXD4/SDA4/SRXD4/ CAN1OUT		ANEX1	
2		P9_5			CLK4/CAN1IN/$\overline{\text{CAN1WU}}$		ANEX0	
3		P9_4		TB4IN	$\overline{\text{CTS4}}$/$\overline{\text{RTS4}}$/$\overline{\text{SS4}}$		DA1	
4		P9_3		TB3IN	$\overline{\text{CTS3}}$/$\overline{\text{RTS3}}$/$\overline{\text{SS3}}$		DA0	
5		P9_2		TB2IN	TXD3/SDA3/SRXD3	OUTC2_0/IEOUT/ISTXD2		
6		P9_1		TB1IN	RXD3/SCL3/STXD3	IEIN/ISRXD2		
7		P9_0		TB0IN	CLK3			
8		P14_6	$\overline{\text{INT8}}$					
9		P14_5	$\overline{\text{INT7}}$					
10		P14_4	$\overline{\text{INT6}}$					
11		P14_3				INPC1_7/OUTC1_7		
12		P14_2				INPC1_6/OUTC1_6		
13		P14_1				INPC1_5/OUTC1_5		
14		P14_0				INPC1_4/OUTC1_4		
15	BYTE							
16	CNVSS							
17	XCIN	P8_7						
18	XCOUT	P8_6						
19	$\overline{\text{RESET}}$							
20	XOUT							
21	VSS							
22	XIN							
23	VCC1							
24		P8_5	$\overline{\text{NMI}}$					
25		P8_4	$\overline{\text{INT2}}$					
26		P8_3	$\overline{\text{INT1}}$		CAN0IN/CAN1IN			
27		P8_2	$\overline{\text{INT0}}$		CAN0OUT/CAN1OUT			
28		P8_1		TA4IN/$\overline{\text{U}}$/RTP2_3	$\overline{\text{CTS5}}$/$\overline{\text{RTS5}}$	INPC1_5/OUTC1_5		
29		P8_0		TA4OUT/U	RXD5	ISRXD0		
30		P7_7		TA3IN/RTP2_2	CLK5/CAN0IN	INPC1_4/OUTC1_4/ ISCLK0		
31		P7_6		TA3OUT	TXD5/CAN0OUT	INPC1_3/OUTC1_3/ ISTXD0		
32		P7_5		TA2IN/$\overline{\text{W}}$/RTP2_1		INPC1_2/OUTC1_2/ ISRXD1		
33		P7_4		TA2OUT/W/ RTP2_0		INPC1_1/OUTC1_1/ ISCLK1		
34		P7_3		TA1IN/$\overline{\text{V}}$	$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$/$\overline{\text{SS2}}$	INPC1_0/OUTC1_0/ ISTXD1		
35		P7_2		TA1OUT/V	CLK2			
36		P7_1		TA0IN/TB5IN/ RTP0_3	RXD2/SCL2/STXD2	INPC1_7/OUTC1_7/ OUTC2_2/ISRXD2/IEIN		
37		P7_0		TA0OUT/RTP0_2	TXD2/SDA2/SRXD2	INPC1_6/OUTC1_6/ OUTC2_0/ISTXD2/IEOUT		
38		P6_7			TXD1/SDA1/SRXD1			
39	VCC1							
40		P6_6			RXD1/SCL1/STXD1			

NOTE:
1. The CAN pins cannot be used in M32C/87B. Only CAN0 pins can be used in M32C/87A.

Table 1.12 100-Pin Package List of Pin Names (1/3)

Pin No.		Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin(1)	Intelligent I/O Pin	Analog Pin	Bus Control Pin
FP	GP								
1	99		P9_6			TXD4/SDA4/SRXD4/ CAN1OUT		ANEX1	
2	100		P9_5			CLK4/CAN1IN/ CAN1WU		ANEX0	
3	1		P9_4		TB4IN	CTS4/RTS4/SS4		DA1	
4	2		P9_3		TB3IN	CTS3/RTS3/SS3		DA0	
5	3		P9_2		TB2IN	TXD3/SDA3/SRXD3	OUTC2_0/IEOUT/ISTXD2		
6	4		P9_1		TB1IN	RXD3/SCL3/STXD3	IEIN/ISRXD2		
7	5		P9_0		TB0IN	CLK3			
8	6	BYTE							
9	7	CNVSS							
10	8	XCIN	P8_7						
11	9	XCOUT	P8_6						
12	10	RESET							
13	11	XOUT							
14	12	VSS							
15	13	XIN							
16	14	VCC1							
17	15		P8_5	NMI					
18	16		P8_4	INT2					
19	17		P8_3	INT1		CAN0IN/CAN1IN			
20	18		P8_2	INT0		CAN0OUT/CAN1OUT			
21	19		P8_1		TA4IN/U/RTP2_3	CTS5/RTS5	INPC1_5/OUTC1_5		
22	20		P8_0		TA4OUT/U	RXD5	ISRXD0		
23	21		P7_7		TA3IN/RTP2_2	CLK5/CAN0IN	INPC1_4/OUTC1_4/ ISCLK0		
24	22		P7_6		TA3OUT	TXD5/CAN0OUT	INPC1_3/OUTC1_3/ ISTXD0		
25	23		P7_5		TA2IN/W/RTP2_1		INPC1_2/OUTC1_2 ISRXD1		
26	24		P7_4		TA2OUT/W/ RTP2_0		INPC1_1/OUTC1_1/ ISCLK1		
27	25		P7_3		TA1IN/V	CTS2/RTS2/SS2	INPC1_0/OUTC1_0/ ISTXD1		
28	26		P7_2		TA1OUT/V	CLK2			
29	27		P7_1		TA0IN/TB5IN/ RTP0_3	RXD2/SCL2/STXD2	INPC1_7/OUTC1_7/ OUTC2_2/ISRXD2/IEIN		
30	28		P7_0		TA0OUT/RTP0_2	TXD2/SDA2/SRXD2	INPC1_6/OUTC1_6/ OUTC2_0/ISTXD2/IEOUT		
31	29		P6_7			TXD1/SDA1/SRXD1			
32	30		P6_6			RXD1/SCL1/STXD1			
33	31		P6_5			CLK1			
34	32		P6_4			CTS1/RTS1/SS1	OUTC2_1/ISCLK2		
35	33		P6_3			TXD0/SDA0/SRXD0/ IrDAOUT			
36	34		P6_2			RXD0/SCL0/STXD0/ IrDAIN			
37	35		P6_1		RTP0_1	CLK0			
38	36		P6_0		RTP0_0	CTS0/RTS0/SS0			
39	37		P5_7						RDY
40	38		P5_6						ALE

NOTE:
1. The CAN pins cannot be used in M32C/87B. Only CAN0 pins can be used in M32C/87A.

Table 1.18 Pin Functions (100-Pin and 144-Pin Package) (4/4)

Type	Symbol	I/O Type	Supply Voltage	Description
I/O port	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7	I/O	VCC2	8-bit CMOS I/O ports. The Port Pi Direction Register (i = 0 to 15) determines if each pin is used as an input port or an output port. The Pull-Up Control Registers determine if the input ports, divided into groups of four, are pulled up or not.
	P6_0 to P6_7, P7_0 to P7_7, P9_0 to P9_7, P10_0 to P10_7	I/O	VCC1	These 8-bit I/O ports are functionally equivalent to P0. (P7_0 and P7_1 are N-channel open drain output.)
	P8_0 to P8_4 P8_6, P8_7	I/O	VCC1	These I/O ports are functionally equivalent to P0.
Input port	P8_5	I	VCC1	Shares the pin with $\overline{\text{NMI}}$. Input port to read $\overline{\text{NMI}}$ pin level.
Key input interrupt input	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	VCC1	Key input interrupt input pins.

I: Input O: Output I/O: Input and output

Table 1.19 Pin Functions (144-Pin Package Only)

Type	Symbol	I/O Type	Supply Voltage	Description
$\overline{\text{INT}}$ Interrupt Input	$\overline{\text{INT6}}$ to $\overline{\text{INT8}}$	I	VCC1	$\overline{\text{INT}}$ interrupt input pins.
Serial interface	$\overline{\text{CTS6}}$	I	VCC1/ VCC2	Input pin to control data transmission.
	$\overline{\text{RTS6}}$	O	VCC1/ VCC2	Output pin to control data reception.
	CLK6	I/O	VCC1/ VCC2	Serial clock input/output pin.
	RXD6	I	VCC1/ VCC2	Serial data input pin.
	TXD6	O	VCC1/ VCC2	Serial data output pin.
Intelligent I/O	OUTC2_3 to OUTC2_7	O	VCC2	Output pins for the waveform generation function.
A/D converter	AN15_0 to AN15_7	I	VCC1	Analog input pins for the A/D converter.
I/O port	P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7	I/O	VCC2	These I/O ports are functionally equivalent to P0.
	P14_0 to P14_6, P15_0 to P15_7	I/O	VCC1	These I/O ports are functionally equivalent to P0.

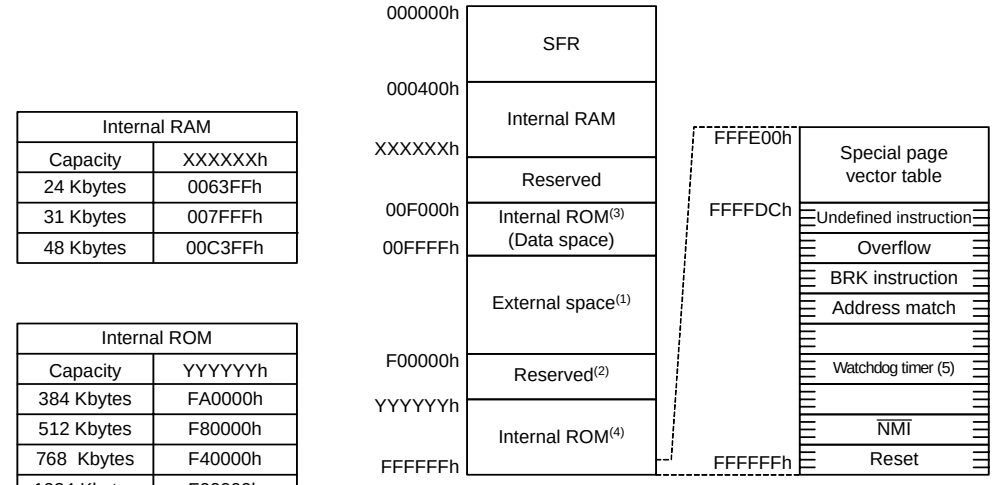
I: Input O: Output I/O: Input and output

3. Memory

Figure 3.1 shows a memory map of the M32C/87 Group (M32C/87, M32C/87A, M32C/87B).
The M32C/87 Group (M32C/87, M32C/87A, M32C/87B) has 16-Mbyte address space from addresses 000000h to FFFFFFh.
The internal ROM is allocated in lower addresses, beginning with address FFFFFFh. For example, a 512-Kbyte internal ROM area is allocated in addresses F80000h to FFFFFFh.
The fixed interrupt vectors are allocated in addresses FFFFDCh to FFFFFFh. They store the starting address of each interrupt routine.
The internal RAM is allocated higher addresses, beginning with address 000400h. For example, a 48-Kbyte internal RAM area is allocated in addresses 000400h to 00C3FFh. The internal RAM is used not only for storing data but for the stacks when subroutines are called or when interrupt requests are acknowledged.
SFRs are allocated in addresses 000000h to 0003FFh. The peripheral function control registers such as for I/O ports, A/D converters, serial interfaces, timers are allocated here. All blank spaces within SFRs are reserved and cannot be accessed by users.
The special page vectors are allocated addresses FFFE00h to FFFFDBh. They are used for the JMPS instruction and JSRS instruction. Refer to the Renesas publication **M32C/80 Series Software Manual** for details.

Internal RAM	
Capacity	XXXXXXh
24 Kbytes	0063FFh
31 Kbytes	007FFFh
48 Kbytes	00C3FFh

Internal ROM	
Capacity	YYYYYYh
384 Kbytes	FA0000h
512 Kbytes	F80000h
768 Kbytes	F40000h
1024 Kbytes	F00000h



NOTES:
1. The space is used as the external space in memory expansion mode and in microprocessor mode. It is reserved in single-ship mode.
2. The space is reserved in memory expansion mode. It is used as the external space in microprocessor mode.
3. Additional 4-Kbyte space is provided in the flash memory version to store data. This space is used in single-chip mode and memory expansion mode. It is reserved in microprocessor mode.
4. This space is used in single-chip mode and memory expansion mode. It is used as the external space in microprocessor mode.
5. The watchdog timer interrupt, oscillation stop detection interrupt, and Vdet4 detection interrupt use the same vector.

Figure 3.1 Memory Map

4. Special Function Registers (SFRs)

Special Function Registers (SFRs) are the control registers of peripheral functions. Tables 4.1 to 4.20 list SFR address maps.

Table 4.1 SFR Address Map (1/20)

Address	Register	Symbol	After Reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0(1)	PM0	1000 0000b(CNVSS="L") 0000 0011b(CNVSS="H")
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	0000 1000b
0007h	System Clock Control Register 1	CM1	0010 0000b
0008h			
0009h	Address Match Interrupt Enable Register	AIER	00h
000Ah	Protect Register	PRCR	XXXX 0000b
000Bh	External Data Bus Width Control Register	DS	XXXX 1000b(BYTE="L") XXXX 0000b(BYTE="H")
000Ch	Main Clock Division Register	MCD	XXX0 1000b
000Dh	Oscillation Stop Detection Register	CM2	00h
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDC	00XX XXXXb
0010h	Address Match Interrupt Register 0	RMAD0	000000h
0011h			
0012h			
0013h	Processor Mode Register 2	PM2	00h
0014h	Address Match Interrupt Register 1	RMAD1	000000h
0015h			
0016h			
0017h	Voltage Detection Register 2	VCR2	00h
0018h	Address Match Interrupt Register 2	RMAD2	000000h
0019h			
001Ah			
001Bh	Voltage Detection Register 1	VCR1	0000 1000b
001Ch	Address Match Interrupt Register 3	RMAD3	000000h
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h			
0024h			
0025h			
0026h	PLL Control Register 0	PLC0	0001 X010b
0027h	PLL Control Register 1	PLC1	000X 0000b
0028h	Address Match Interrupt Register 4	RMAD4	000000h
0029h			
002Ah			
002Bh			
002Ch	Address Match Interrupt Register 5	RMAD5	000000h
002Dh			
002Eh			
002Fh	Vdet4 Detection Interrupt Register	D4INT	XX00 0000b

X: Undefined
Blank spaces are all reserved. No access is allowed.
NOTE:
1. Bits PM01 and PM00 in the PM0 register maintain values set before reset, even after software reset or watchdog timer reset has been performed.

Table 4.3 SFR Address Map (3/20)

Address	Register	Symbol	After Reset
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h	DMA0 Interrupt Control Register	DM0IC	XXXX X000b
0069h	Timer B5 Interrupt Control Register	TB5IC	XXXX X000b
006Ah	DMA2 Interrupt Control Register	DM2IC	XXXX X000b
006Bh	UART2 Receive/ACK Interrupt Control Register	S2RIC	XXXX X000b
006Ch	Timer A0 Interrupt Control Register	TA0IC	XXXX X000b
006Dh	UART3 Receive/ACK Interrupt Control Register	S3RIC	XXXX X000b
006Eh	Timer A2 Interrupt Control Register	TA2IC	XXXX X000b
006Fh	UART4 Receive/ACK Interrupt Control Register	S4RIC	XXXX X000b
0070h	Timer A4 Interrupt Control Register	TA4IC	XXXX X000b
0071h	UART0/UART3 Bus Conflict Detection Interrupt Control Register	BCN0IC/BCN3IC	XXXX X000b
0072h	UART0 Receive/ACK Interrupt Control Register	S0RIC	XXXX X000b
0073h	A/D0 Conversion Interrupt Control Register	AD0IC	XXXX X000b
0074h	UART1 Receive/ACK Interrupt Control Register	S1RIC	XXXX X000b
0075h	II/O Interrupt Control Register 0 / CAN1 interrupt Control Register 0	IIO0IC/CAN3IC	XXXX X000b
0076h	Timer B1 Interrupt Control Register	TB1IC	XXXX X000b
0077h	II/O Interrupt Control Register 2	IIO2IC	XXXX X000b
0078h	Timer B3 Interrupt Control Register	TB3IC	XXXX X000b
0079h	II/O Interrupt Control Register 4	IIO4IC	XXXX X000b
007Ah	$\overline{\text{INT5}}$ Interrupt Control Register	INT5IC	XX00 X000b
007Bh	II/O Interrupt Control Register 6	IIO6IC	XXXX X000b
007Ch	$\overline{\text{INT3}}$ Interrupt Control Register	INT3IC	XX00 X000b
007Dh	II/O Interrupt Control Register 8	IIO8IC	XXXX X000b
007Eh	$\overline{\text{INT1}}$ Interrupt Control Register	INT1IC	XX00 X000b
007Fh	II/O Interrupt Control Register 10 / CAN0 Interrupt Control Register 1	IIO10IC/CAN1IC	XXXX X000b
0080h			
0081h	II/O Interrupt Control Register 11 / CAN0 Interrupt Control Register 2	IIO11IC/CAN2IC	XXXX X000b
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h	DMA1 Interrupt Control Register	DM1IC	XXXX X000b
0089h	UART2 Transmit/NACK Interrupt Control Register	S2TIC	XXXX X000b
008Ah	DMA3 Interrupt Control Register	DM3IC	XXXX X000b
008Bh	UART3 Transmit/NACK Interrupt Control Register	S3TIC	XXXX X000b
008Ch	Timer A1 Interrupt Control Register	TA1IC	XXXX X000b
008Dh	UART4 Transmit/NACK Interrupt Control Register	S4TIC	XXXX X000b
008Eh	Timer A3 Interrupt Control Register	TA3IC	XXXX X000b
008Fh	UART2 Bus Conflict Detection Interrupt Control Register	BCN2IC	XXXX X000b

X: Undefined
Blank spaces are all reserved. No access is allowed.

Table 4.4 SFR Address Map (4/20)

Address	Register	Symbol	After Reset
0090h	UART0 Transmit/NACK Interrupt Control Register	S0TIC	XXXX X000b
0091h	UART1/UART4 Bus Conflict Detection Interrupt Control Register	BCN1IC/BCN4IC	XXXX X000b
0092h	UART1 Transmit/NACK Interrupt Control Register	S1TIC	XXXX X000b
0093h	Key Input Interrupt Control Register	KUPIC	XXXX X000b
0094h	Timer B0 Interrupt Control Register	TB0IC	XXXX X000b
0095h	II/O Interrupt Control Register 1 / CAN1 Interrupt Control Register 1	IIO1IC/CAN4IC	XXXX X000b
0096h	Timer B2 Interrupt Control Register	TB2IC	XXXX X000b
0097h	II/O Interrupt Control Register 3	IIO3IC	XXXX X000b
0098h	Timer B4 Interrupt Control Register	TB4IC	XXXX X000b
0099h	II/O Interrupt Control Register 5 /CAN1 Interrupt Control Register 2	IIO5IC/CAN5IC	XXXX X000b
009Ah	$\overline{\text{INT4}}$ Interrupt Control Register	INT4IC	XX00 X000b
009Bh	II/O Interrupt Control Register 7	IIO7IC	XXXX X000b
009Ch	$\overline{\text{INT2}}$ Interrupt Control Register	INT2IC	XX00 X000b
009Dh	II/O Interrupt Control Register 9 / CAN0 Interrupt Control Register 0	IIO9IC/CAN0IC	XXXX X000b
009Eh	$\overline{\text{INT0}}$ Interrupt Control Register	INT0IC	XX00 X000b
009Fh	Exit Priority Register	RLVL	XXXX 0000b
00A0h	Interrupt Request Register 0	IIO0IR	0000 000Xb
00A1h	Interrupt Request Register 1	IIO1IR	0000 000Xb
00A2h	Interrupt Request Register 2	IIO2IR	0000 000Xb
00A3h	Interrupt Request Register 3	IIO3IR	0000 000Xb
00A4h	Interrupt Request Register 4	IIO4IR	0000 000Xb
00A5h	Interrupt Request Register 5	IIO5IR	0000 000Xb
00A6h	Interrupt Request Register 6	IIO6IR	0000 000Xb
00A7h	Interrupt Request Register 7	IIO7IR	0000 000Xb
00A8h	Interrupt Request Register 8	IIO8IR	0000 000Xb
00A9h	Interrupt Request Register 9	IIO9IR	0000 000Xb
00AAh	Interrupt Request Register 10	IIO10IR	0000 000Xb
00ABh	Interrupt Request Register 11	IIO11IR	0000 000Xb
00ACh			
00ADh			
00AEh			
00AFh			
00B0h	Interrupt Enable Register 0	IIO0IE	00h
00B1h	Interrupt Enable Register 1	IIO1IE	00h
00B2h	Interrupt Enable Register 2	IIO2IE	00h
00B3h	Interrupt Enable Register 3	IIO3IE	00h
00B4h	Interrupt Enable Register 4	IIO4IE	00h
00B5h	Interrupt Enable Register 5	IIO5IE	00h
00B6h	Interrupt Enable Register 6	IIO6IE	00h
00B7h	Interrupt Enable Register 7	IIO7IE	00h
00B8h	Interrupt Enable Register 8	IIO8IE	00h
00B9h	Interrupt Enable Register 9	IIO9IE	00h
00BAh	Interrupt Enable Register 10	IIO10IE	00h
00BBh	Interrupt Enable Register 11	IIO11IE	00h
00BCh			
00BDh			
00BEh			
00BFh to 00DFh			

X: Undefined
Blank spaces are all reserved. No access is allowed.

Table 4.5 SFR Address Map (5/20)

Address	Register	Symbol	After Reset
00E0h			
00E1h			
00E2h			
00E3h			
00E4h			
00E5h			
00E6h			
00E7h			
00E8h	Group 0 SI/O Receive Buffer Register	G0RB	XXXX XXXXb
00E9h			XXX0 XXXXb
00EAh	Group 0 Transmit Buffer/Receive Data Register	G0TB/G0DR	XXh
00EBh			
00ECh	Group 0 Receive Input Register	G0RI	XXh
00EDh	Group 0 SI/O Communication Mode Register	G0MR	00h
00EEh	Group 0 Transmit Output Register	G0TO	XXh
00EFh	Group 0 SI/O Communication Control Register	G0CR	0000 X011b
00F0h	Group 0 Data Compare Register 0	G0CMP0	XXh
00F1h	Group 0 Data Compare Register 1	G0CMP1	XXh
00F2h	Group 0 Data Compare Register 2	G0CMP2	XXh
00F3h	Group 0 Data Compare Register 3	G0CMP3	XXh
00F4h	Group 0 Data Mask Register 0	G0MSK0	XXh
00F5h	Group 0 Data Mask Register 1	G0MSK1	XXh
00F6h	Communication Clock Select Register	CCS	XXXX 0000b
00F7h			
00F8h	Group 0 Receive CRC Code Register	G0RCRC	XXXXh
00F9h			
00FAh	Group 0 Transmit CRC Code Register	G0TCRC	0000h
00FBh			
00FCh	Group 0 SI/O Expansion Mode Register	G0EMR	00h
00FDh	Group 0 SI/O Extended Receive Control Register	G0ERC	00h
00FEh	Group 0 SI/O Special Communication Interrupt Detection Register	G0IRF	0000 XXXXb
00FFh	Group 0 SI/O Extended Transmit Control Register	G0ETC	0000 0XXXb
0100h	Group 1 Time Measurement/Waveform Generation Register 0	G1TM0/G1PO0	XXXXh
0101h			
0102h	Group 1 Time Measurement/Waveform Generation Register 1	G1TM1/G1PO1	XXXXh
0103h			
0104h	Group 1 Time Measurement/Waveform Generation Register 2	G1TM2/G1PO2	XXXXh
0105h			
0106h	Group 1 Time Measurement/Waveform Generation Register 3	G1TM3/G1PO3	XXXXh
0107h			
0108h	Group 1 Time Measurement/Waveform Generation Register 4	G1TM4/G1PO4	XXXXh
0109h			
010Ah	Group 1 Time Measurement/Waveform Generation Register 5	G1TM5/G1PO5	XXXXh
010Bh			
010Ch	Group 1 Time Measurement/Waveform Generation Register 6	G1TM6/G1PO6	XXXXh
010Dh			
010Eh	Group 1 Time Measurement/Waveform Generation Register 7	G1TM7/G1PO7	XXXXh
010Fh			
0110h	Group 1 Waveform Generation Control Register 0	G1POCR0	0000 X000b
0111h	Group 1 Waveform Generation Control Register 1	G1POCR1	0X00 X000b
0112h	Group 1 Waveform Generation Control Register 2	G1POCR2	0X00 X000b
0113h	Group 1 Waveform Generation Control Register 3	G1POCR3	0X00 X000b
0114h	Group 1 Waveform Generation Control Register 4	G1POCR4	0X00 X000b
0115h	Group 1 Waveform Generation Control Register 5	G1POCR5	0X00 X000b
0116h	Group 1 Waveform Generation Control Register 6	G1POCR6	0X00 X000b
0117h	Group 1 Waveform Generation Control Register 7	G1POCR7	0X00 X000b
0118h	Group 1 Time Measurement Control Register 0	G1TMCR0	00h
0119h	Group 1 Time Measurement Control Register 1	G1TMCR1	00h

X: Undefined
Blank spaces are all reserved. No access is allowed.

Table 4.7 SFR Address Map (7/20)

Address	Register	Symbol	After Reset
0150h	Group 2 Waveform Generation Control Register 0	G2POCR0	00h
0151h	Group 2 Waveform Generation Control Register 1	G2POCR1	00h
0152h	Group 2 Waveform Generation Control Register 2	G2POCR2	00h
0153h	Group 2 Waveform Generation Control Register 3	G2POCR3	00h
0154h	Group 2 Waveform Generation Control Register 4	G2POCR4	00h
0155h	Group 2 Waveform Generation Control Register 5	G2POCR5	00h
0156h	Group 2 Waveform Generation Control Register 6	G2POCR6	00h
0157h	Group 2 Waveform Generation Control Register 7	G2POCR7	00h
0158h			
0159h			
015Ah			
015Bh			
015Ch			
015Dh			
015Eh			
015Fh			
0160h 0161h	Group 2 Base Timer Register	G2BT	XXXXh
0162h	Group 2 Base Timer Control Register 0	G2BCR0	00h
0163h	Group 2 Base Timer Control Register 1	G2BCR1	00h
0164h	Base Timer Start Register	BTSR	XXXX 0000b
0165h			
0166h	Group 2 Function Enable Register	G2FE	00h
0167h	Group 2 RTP Output Buffer Register	G2RTP	00h
0168h			
0169h			
016Ah	Group 2 SI/O Communication Mode Register	G2MR	00XX X000b
016Bh	Group 2 SI/O Communication Control Register	G2CR	0000 X000b
016Ch 016Dh	Group 2 SI/O Transmit Buffer Register	G2TB	XXXXh
016Eh 016Fh	Group 2 SI/O Receive Buffer Register	G2RB	XXXXh
0170h 0171h	Group 2 IEBus Address Register	IEAR	XXXXh
0172h	Group 2 IEBus Control Register	IECR	00XX X000b
0173h	Group 2 IEBus Transmit Interrupt Source Detection Register	IETIF	XXX0 0000b
0174h	Group 2 IEBus Receive Interrupt Source Detection Register	IERIF	XXX0 0000b
0175h			
0176h			
0177h	Input Function Select Register B	IPSB	00h
0178h	Input Function Select Register	IPS	00h
0179h	Input Function Select Register A	IPSA	00h
017Ah			
017Bh			
017Ch			
017Dh to 01BFh			

X: Undefined
Blank spaces are all reserved. No access is allowed.

Table 4.20 SFR Address Map (20/20)

Address	Register	Symbol	After Reset
03D0h	Port P14 Register(1)	P14	XXh
03D1h	Port P15 Register(1)	P15	XXh
03D2h	Port P14 Direction Register(1)(2)	PD14	X000 0000b
03D3h	Port P15 Direction Register(1)(2)	PD15	00h
03D4h			
03D5h			
03D6h			
03D7h			
03D8h			
03D9h			
03DAh	Pull-Up Control Register 2	PUR2	00h
03DBh	Pull-Up Control Register 3	PUR3	00h
03DCh	Pull-Up Control Register 4(1)(3)	PUR4	XXXX 0000b
03DDh			
03DEh			
03DFh			
03E0h	Port P0 Register	P0	XXh
03E1h	Port P1 Register	P1	XXh
03E2h	Port P0 Direction Register	PD0	00h
03E3h	Port P1 Direction Register	PD1	00h
03E4h	Port P2 Register	P2	XXh
03E5h	Port P3 Register	P3	XXh
03E6h	Port P2 Direction Register	PD2	00h
03E7h	Port P3 Direction Register	PD3	00h
03E8h	Port P4 Register	P4	XXh
03E9h	Port P5 Register	P5	XXh
03EAh	Port P4 Direction Register	PD4	00h
03EBh	Port P5 Direction Register	PD5	00h
03ECh			
03EDh			
03EEh			
03EFh			
03F0h	Pull-Up Control Register 0	PUR0	00h
03F1h	Pull-Up Control Register 1	PUR1	XXXX 0000b
03F2h			
03F3h			
03F4h			
03F5h			
03F6h			
03F7h			
03F8h			
03F9h			
03FAh			
03FBh			
03FCh			
03FDh			
03FEh			
03FFh	Port Control Register	PCR	XXXX X000b

X: Undefined
Blank spaces are all reserved. No access is allowed.
NOTES:
1. These registers cannot be used in the 100-pin package.
2. Set to FFh in the 100-pin package.
3. Set to 00h in the 100-pin package.

Table 5.3 Recommended Operating Conditions (2/3)
(VCC1 = VCC2 = 3.0 to 5.5 V, Topr = -20 to 85°C unless otherwise specified

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
IOH(peak)	Peak output high “H” current(2)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7(3)			-10.0	mA
IOH(avg)	Average output high “H” current(1)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7(3)			-5.0	mA
IOL(peak)	Peak output low “L” current(2)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7(3)			10.0	mA
IOL(avg)	Average output low “L” current(1)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7(3)			5.0	mA

NOTES:
1. Average output current is the average value within 100 ms.
2. A total IOL(peak) of P0, P1, P2, P8_6, P8_7, P9, P10, P11, P14, and P15 must be 80 mA or less.
   A total IOL(peak) of P3, P4, P5, P6, P7,P8_0 to P8_4, P12, and P13 must be 80 mA or less.
   A total IOH(peak) of P0, P1, P2, and P11 must be -40 mA or less.
   A total IOH(peak) of P8_6 to P8_7, P9, P10, P14, and P15 must be -40 mA or less.
   A total IOH(peak) of P3, P4, P5, P12, and P13 must be -40 mA or less.
   A total IOH(peak) of P6, P7, and P8_0 to P8_4 must be -40 mA or less.
3. P11 to P15 are provided in the 144-pin package only.

VCC1 = VCC2 = 5V

Table 5.11 Voltage Detection Circuit Electrical Characteristics (VCC1 = VCC2 = 3.0 to 5.5 V, VSS = 0 V, Topr = 25°C unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet4	Vdet4 detection voltage	VCC1 = 3.0 V to 5.5 V	3.3	3.8	4.4	V
Vdet3	Vdet3 detection voltage			3.0		V
Vdet3s	Hardware reset 2 hold voltage				2.0	V
Vdet3r	Hardware reset 2 release voltage			3.1		V

NOTES:
1. Vdet4 > Vdet3
2. Vdet3r > Vdet3 is not guaranteed.

Table 5.12 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
td(P-R)	Wait time to stabilize internal supply voltage when power-on	VCC1 = 3.0 to 5.5 V			2	ms
td(S-R)	Wait time to release hardware reset 2	VCC1 = Vdet3r to 5.5 V		6(1)	20	ms
td(E-A)	Start-up time for Vdet3 and Vdet4 detection circuit	VCC1 = 3.0 to 5.5 V			20	µs

NOTE:
1. When VCC1 = 5 V

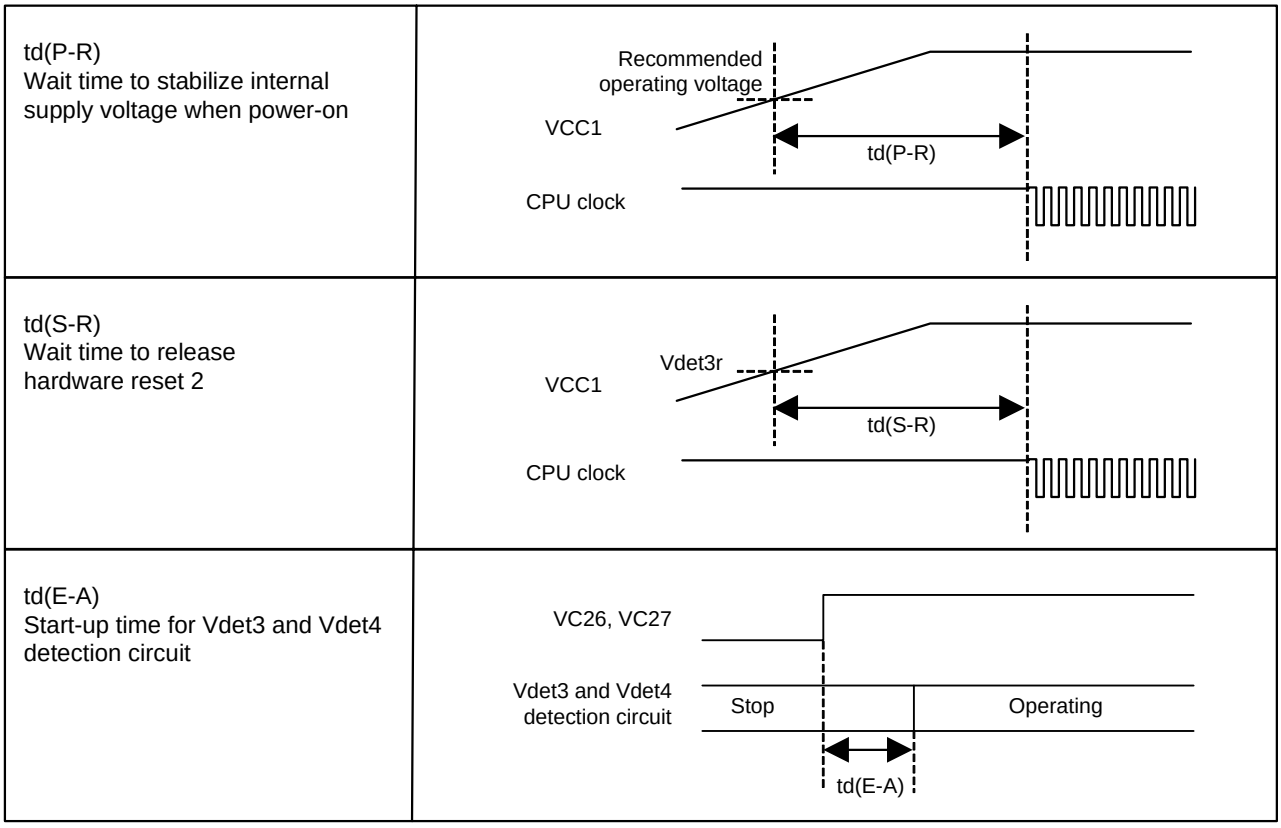


Figure 5.1 Power Supply Timing Diagram

VCC1 = VCC2 = 3.3 V

Timing Requirements
(VCC1 = VCC2 = 3.0 to 3.6 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.41 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(UP)	TAiOUT input cycle time	2000		ns
tw(UPH)	TAiOUT input high (“H”) pulse width	1000		ns
tw(UPL)	TAiOUT input low (“L”) pulse width	1000		ns
tsu(UP-TIN)	TAiOUT input setup time	400		ns
th(TIN-UP)	TAiOUT input hold time	400		ns

i = 0 to 4

Table 5.42 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	2		µs
tsu(TAIN-TAOUT)	TAiOUT input setup time	500		ns
tsu(TAOUT-TAIN)	TAiIN input setup time	500		ns

i = 0 to 4

Table 5.43 Timer B Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TB)	TBiIN input cycle time (counted on one edge)	100		ns
tw(TBH)	TBiIN input high (“H”) pulse width (counted on one edge)	40		ns
tw(TBL)	TBiIN input low (“L”) pulse width (counted on one edge)	40		ns
tc(TB)	TBiIN input cycle time (counted on both edges)	200		ns
tw(TBH)	TBiIN input high (“H”) pulse width (counted on both edges)	80		ns
tw(TBL)	TBiIN input low (“L”) pulse width (counted on both edges)	80		ns

i = 0 to 5

Table 5.44 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TB)	TBiIN input cycle time	400		ns
tw(TBH)	TBiIN input high (“H”) pulse width	200		ns
tw(TBL)	TBiIN input low (“L”) pulse width	200		ns

i = 0 to 5

Table 5.45 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TB)	TBiIN input cycle time	400		ns
tw(TBH)	TBiIN input high (“H”) pulse width	200		ns
tw(TBL)	TBiIN input low (“L”) pulse width	200		ns

i = 0 to 5

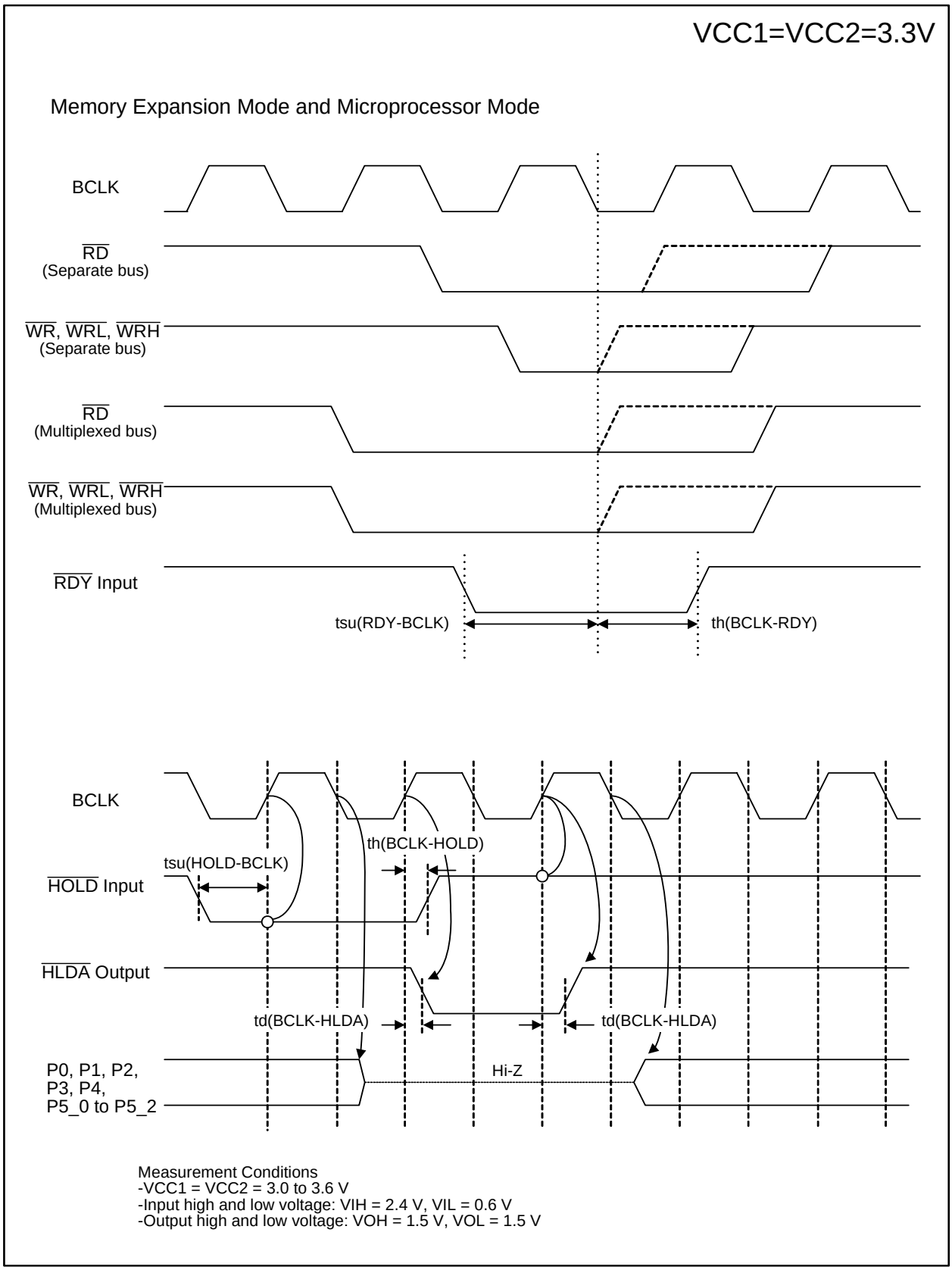


Figure 5.8 VCC1 = VCC2 = 3.3 V Timing Diagram (2/4)

REVISION HISTORY	M32C/87 Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.50	Dec.16, 04	–	New Document
1.00	Jul.14, 05	–	**M32C/87A and M32C/87B** added
		–	Package code changed: 144P6Q-A to PLQP0144KA-A, 100P6Q-A to PLQP0100KB-A, 100P6S-A to PRQP0100JB-A
		–	"Low Voltage Detection Reset" changed to "Brown-out Detection Reset"
			Overview
		2	• **Table 1.2 M32C/87 Group Performance (144-Pin Package)** M32C/87A and M32C/87B performance added to the CAN module performance; Power Consumption performance released
		3	• **Table 1.2 M32C/87 Group Performance (100-Pin Package)** M32C/87A and M32C/87B performance added to the CAN module performance; Power Consumption performance released
		4	• **Figure 1.1 M32C/87 Group Block Diagram** Note 4 deleted; note 5 added
		7	• **Figure 1.3 Pin Assignment for 144-Pin Package** Note 15 added
		8	• **Table 1.4 Pin Characteristics for 144-Pin Package** Note 1 added
		11	• **Figure 1.4 Pin Assignment for 100-Pin Package** Note 19 added
		12	• **Figure 1.5 Pin Assignment for 100-Pin Package** Note 15 added
		13	• **Table 1.5 Pin Characteristics for 100-Pin Package** Note 1 added
		17	• **Table 1.6 Pin Description** Note 2 added
			Memory
		22	• **Figure 3.1 Memory Map** Note 3 changed
			Special Function Register (SFR)
		26	• The RLVL register Value after reset modified
		26	• The IIO0IR to IIO11IR registers Value after reset modified
		27 to 30	• Name of the registers assosiated to Intelligent I/O changed
		27	• The G0RB register Value after reset modified
		27	• The G1BCR0 and G1BCR1 registers Value after reset modified
		29	• The G0CR register Value after reset modified
		32 to 37	• Note added to the CAN-associated registers
		40	• The TCSPR register Value after reset modified; note 1 added
		41	• The AD00 register Value after reset modified
		42	• The PSC register Value after reset modified
		42	• The PS2 register Value after reset modified
		43	• The PCR register Value after reset modified
		44	• The PSD1 register Value after reset modified
		45	• The PCR register Value after reset modified
			Electrical Characteristics
		48	• **Table 5.2 Electrical Characteristics** Parameter f(BCLK) and its values added; min. and max. values for f(RING) added
		49	• **Table 5.3 Electrical Characteristics** V_{OH} values modified**;** R_{PULLUP} value modified
		50	• **Table 5.3 Electrical Characteristics (Continued)** Measurement Condition and standard values for ICC added and some released
		52	• **Table 5.6 Flash Memory Version Electrical Characteristics** Word Program Time and Lock bit Program Time values modified; parameter All-Unlocked-Block-Erase Time deleted; note 1 deleted
		54	• **Table 5.10 Memory Expansion Mode and Microprocessor Mode** *tac1(RD-DB)* expression on note 1 modified; *tac2(RD-DB)* expression on note 1 added

REVISION HISTORY	M32C/87 Group Datasheet

Rev.	Date	Description	
		Page	Summary
			SFR
		42	• [Register names changed] 0342h One-Shot Start Flag → One-Shot Start Register 0344h Up-Down Flag → Up/Down Select Register
			• [Value After Reset changed]
		27	000Fh WDC 000X XXX$_2$ → 00XX XXXXb
		27	002Fh D4INT 00$_{16}$ → XX00 0000b
		29	007Bh IIO6IC XX00 X000$_2$ → XXXX X000b
		31	00EFh G0CR XX00 X011$_2$ → 0000 X011b
		31	00FEh G0IRF 00$_{16}$ → 0000 XXXXb
		32	013Eh G1IRF 00$_{16}$ → 0000 XXXXb
		34	01C7h to 01C6h U5RB XXXX XXXX XXXX 0XXX$_2$ → XXXXh
		34	01CFh to 01CEh U6RB XXXX XXXX XXXX 0XXX$_2$ → XXXXh
		44	038Fh to 0382h AD07 to AD01 XXXX$_{16}$ → 00XXh
			Electrical Characteristics
			• [Term changed] Low Voltage Reset → Hardware Reset 2 Low Voltage Detection → Vdet3 and Vdet4 detection circuit
		47	• **Table 5.1** Description in Condition field of Pd (Power consumption) partially modified
		50-53	• **Tables 5.2** to **5.9** f(BCLK) is changed to f(CPU)
		50	• **Table 5.4** Description added in Parameter field of f(CPU); f(VCO) added
		51,69	• **Tables 5.5** to **5.7** and **Tables 5.31** to **5.33** Description in XCOUT and Hysteresis in Parameter fields partially modified
		53,71	• **Table 5.7** and **5.33** Structure and standard values revised; items in Measurement Condition and NOTE added
		54	• **Table 5.8** Description in Parameter field and NOTE partially modified
		54,55	• **Table 5.9** and **5.10** Description in Parameter field and NOTE partially modified
		56,73	• **Tables 5.11** and **5.36** Description in Parameter field and standard value partially modified
		58,74	• **Tables 5.19** and **5.42** added
		59	• **Table 5.24** Values revised; **Table 5.25** and **5.26 added**
		60	• **Table 5.27** Titles modified; NOTE added
		61	• **Table 5.28** moved to the last table in Timing Requirements
		62-63	• **Table 5.29** NOTE 3 added; **Table 26.30** NOTE 5 added
		65-68	• **Figures 5.3** to **5.6** Order rearranged; measurement condition modified
		69-72	• **Table 5.31** to **5.35** f(BCLK) revised to f(CPU)
		75	• **Table 5.47** Values revised; **Table5.48** and **5.49** added
		76	• **Table 5.50** Titles modified; NOTE added
		77	• **Table 5.51** Table moved to the last table in Timing Requirements
		78-79	• **Table 5.52** NOTE 3 added**; Table 5.53** NOTE 5 added
		80-83	• **Figures 5.7** to **5.10** Order rearranged
1.51	Jul 31, 2008	–	**All in this manual** [description modified] • Title of group tables “(current table number / total tables)” added
			Overview
		19	• **1.5 Pin Descriptions** Chapter and table title changed to **Pin Functions**
		21	• **Table 1.17** Supply voltage for AN0_0 to AN0_7, AN2_0 to AN2_7 modified