Renesas Electronics America Inc - M30878FJGP#U5 Datasheet

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Applications of "Embedded - Microcontrollers"

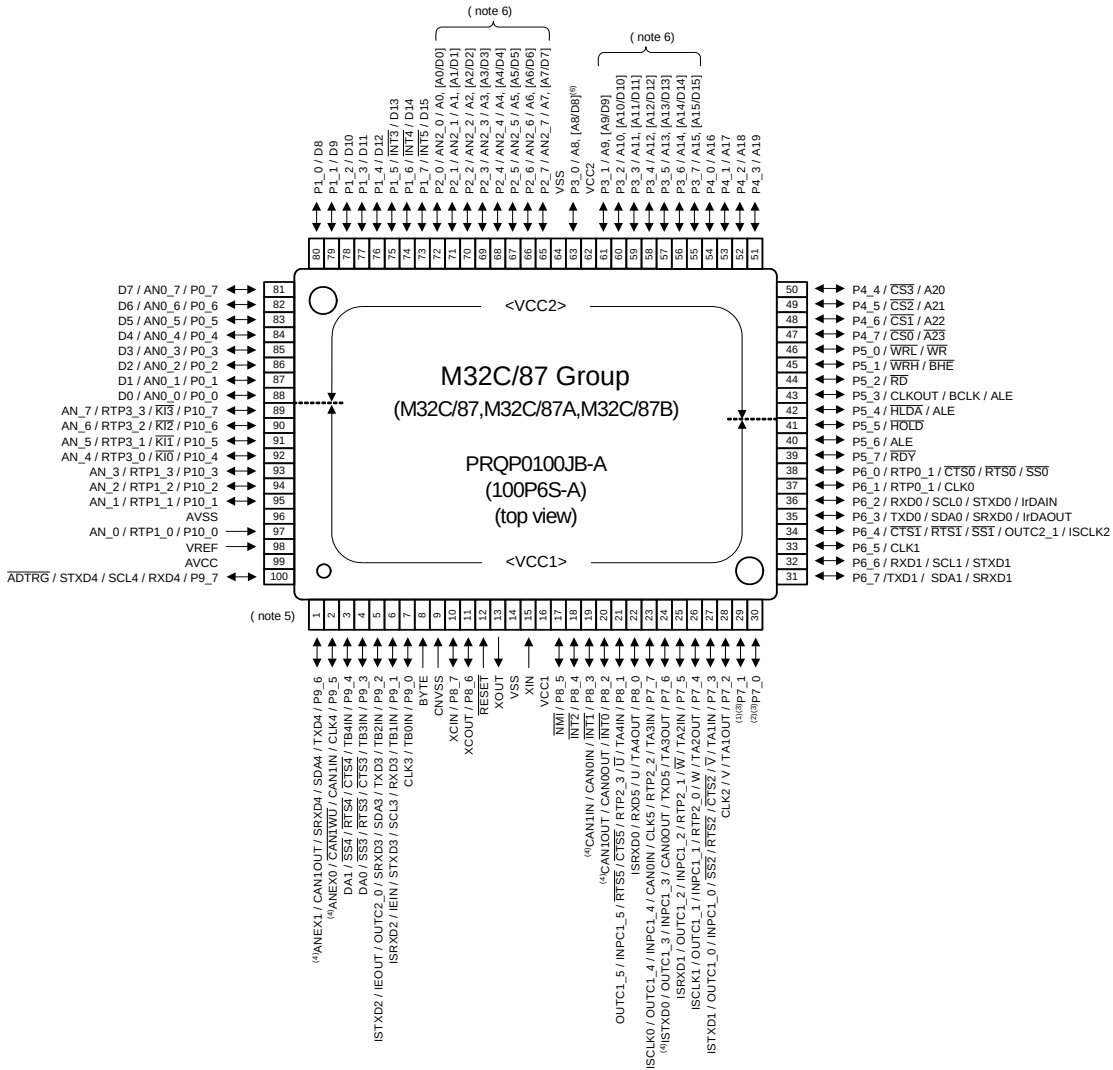
Details	
Product Status	Obsolete
Core Processor	M32C/80
Core Size	16/32-Bit
Speed	32MHz
Connectivity	CANbus, EBI/EMI, I²C, IEBus, IrDA, SIO, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	121
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	31K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 34x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30878fjgp-u5

1.1.2 Specifications

Tables 1.1 to 1.4 list the specifications of the M32C/87 Group (M32C/87, M32C/87A, M32C/87B).

Table 1.1 Specifications (144-Pin Package) (1/2)

Item	Function	Specification
CPU	Central processing unit	M32C/80 core (multiplier: 16 bits × 16 bits → 32 bits multiply-addition operation instructions: 16 × 16 + 48 → 48 bits) • Basic instructions: 108 • Minimum instruction execution time: 31.3 ns (f(CPU) = 32 MHz, VCC1 = 4.2 to 5.5 V) 41.7 ns (f(CPU) = 24 MHz, VCC1 = 3.0 to 5.5 V) • Operating modes: Single-chip mode, memory expansion mode, and microprocessor mode
Memory	ROM, RAM, data flash	See **Tables 1.5 to 1.7 Product List**.
Power Supply Voltage Detection		Vdet3 detection function, Vdet4 detection function, cold start/warm start determination function
External Bus Expansion	Bus/memory expansion function	• Address space: 16 Mbytes • External bus interface: 1 to 7 wait states can be inserted, 4 chip select outputs, 3 V and 5 V interfaces • Bus format: Switchable between separate bus and multiplexed bus formats, switchable data bus width (8-bit or 16-bit)
Clock	Clock generation circuits	• 4 circuits: Main clock, sub clock, on-chip oscillator, PLL frequency synthesizer • Oscillation stop detection: Main clock oscillation stop detection function • Frequency divider circuit: Dividing ratio selectable among 1, 2, 3, 4, 6, 8, 10, 12, 14, 16 • Low power consumption features: Wait mode, stop mode
Interrupts		• Interrupt vectors: 70 • External interrupt inputs: 14 ($\overline{\text{NMI}}$, $\overline{\text{INT}}$ × 9, key input × 4) • Interrupt priority levels: 7
Watchdog Timer		15-bit × 1 channel (with prescaler)
DMA	DMAC	• 4 channels, cycle steal method • Trigger sources: 43 • Transfer modes: 2 (single transfer and repeat transfer)
	DMACII	• Can be activated by all peripheral function interrupt sources • Transfer modes: 2 (single transfer and burst transfer) • Immediate transfer, calculation transfer, and chain transfer functions
Timer	Timer A	16-bit timer × 5 Timer mode, event counter mode, one-shot timer mode, pulse width modulation (PWM) mode, Event counter 2-phase pulse signal processing (2-phase encoder input) × 3
	Timer B	16-bit timer × 6 Timer mode, event counter mode, pulse period measurement mode, pulse width measurement mode
	Timer function for 3-phase motor control	3-phase inverter control × 1 (using timer A1, timer A2, timer A4, and timer B2) On-chip dead time timer



NOTES:
1. P7_1 / TA0IN / TB5IN / RTP0_3 / RXD2 / SCL2 / STXD2 / INPC1_7 / OUTC1_7 / OUTC2_2 / ISRXD2 / IEIN
2. P7_0 / TA0OUT / RTP0_2 / TXD2 / SDA2 / SRXD2 / INPC1_6 / OUTC1_6 / OUTC2_0 / ISTXD2 / IEOUT
3. P7_0 and P7_1 are N-channel open drain output ports.
4. The CAN pins cannot be used in M32C/87B. Only CAN0 pins can be used in M32C/87A.
5. Refer to **Package Dimensions** for the pin1 position on the package.
6. Pin names in brackets [ ] represent a single functional signal. They should not be considered as two separate functional signals.

Figure 1.4 Pin Assignment for 100-Pin Package

1.5 Pin Functions

Table 1.15 Pin Functions (100-Pin and 144-Pin Packages) (1/4)

Type	Symbol	I/O Type	Supply Voltage	Description
Power supply	VCC1,VCC2 VSS	–	–	Apply 3.0 to 5.5 V to pins VCC1 and VCC2, and 0 V to the VSS pin. The input condition of VCC1 ≥ VCC2 must be met.
Analog power supply input	AVCC AVSS	–	VCC1	Power supply input pins to the A/D converter and D/A converter. Connect the AVCC pin to VCC1, and the AVSS pin to VSS.
Reset input	$\overline{\text{RESET}}$	I	VCC1	The MCU is placed in the reset state while applying an “L” signal to the $\overline{\text{RESET}}$ pin.
CNVSS	CNVSS	I	VCC1	This pin switches processor mode. Apply an “L” to the CNVSS pin to start up in single-chip mode, or an “H” to start up in microprocessor mode (mask ROM, flash memory version) and boot mode (flash memory version).
External data bus width select input	BYTE	I	VCC1	This pin switches a data bus width in external memory space 3. A data bus is 16 bits wide when the BYTE pin is held “L” and 8 bits wide when it is held “H”. Fix to either “L” or “H”. Apply an “L” to the BYTE pin in single-chip mode.
Bus control Pins	D0 to D7	I/O	VCC2	Data (D0 to D7) input/output pins while accessing an external memory space with separate bus.
	D8 to D15	I/O	VCC2	Data (D8 to D15) input/output pins while accessing an external memory space with 16-bit separate bus.
	A0 to A22	O	VCC2	Address bits (A0 to A22) output pins.
	$\overline{\text{A23}}$	O	VCC2	Inverted address bit (A23) output pin.
	A0/D0 to A7/D7	I/O	VCC2	Data (D0 to D7) input/output and 8 low-order address bits (A0 to A7) output are performed by time-sharing these pins while accessing an external memory space with multiplexed bus.
	A8/D8 to A15/D15	I/O	VCC2	Data (D8 to D15) input/output and 8 middle-order address bits (A8 to A15) output are performed by time-sharing these pins while accessing an external memory space with 16-bit multiplexed bus.
	$\overline{\text{CS0}}$ to $\overline{\text{CS3}}$	O	VCC2	Chip-select signal output pins used to specify external devices.
	$\overline{\text{WRL}}$/$\overline{\text{WR}}$ $\overline{\text{WRH}}$/$\overline{\text{BHE}}$ $\overline{\text{RD}}$	O	VCC2	$\overline{\text{WRL}}$, $\overline{\text{WRH}}$, ($\overline{\text{WR}}$, $\overline{\text{BHE}}$) and $\overline{\text{RD}}$ signal output pins. $\overline{\text{WRL}}$ and $\overline{\text{WRH}}$ can be switched with $\overline{\text{WR}}$ and $\overline{\text{BHE}}$ by a program. • $\overline{\text{WRL}}$, $\overline{\text{WRH}}$ and $\overline{\text{RD}}$ are selected: If external data bus is 16 bits wide, data is written to an even address in external memory space while an “L” is output from the $\overline{\text{WRL}}$ pin. Data is written to an odd address while an “L” is output from the $\overline{\text{WRH}}$ pin. Data is read while an “L” is output from the $\overline{\text{RD}}$ pin. • $\overline{\text{WR}}$, $\overline{\text{BHE}}$ and $\overline{\text{RD}}$ are selected: Data is written while an “L” is output from the $\overline{\text{WR}}$ pin. Data is read while an “L” is output from the $\overline{\text{RD}}$ pin. Data in odd address is accessed while an “L” is output from the $\overline{\text{BHE}}$ pin. Select $\overline{\text{WR}}$, $\overline{\text{BHE}}$ and $\overline{\text{RD}}$ when an external data bus is 8 bits wide.
	ALE	O	VCC2	ALE signal is used for the external devices to latch address signals when the multiplexed bus is selected.
	$\overline{\text{HOLD}}$	I	VCC2	The MCU is placed in a hold state while an “L” signal is applied to the $\overline{\text{HOLD}}$ pin.
	$\overline{\text{HLDA}}$	O	VCC2	The $\overline{\text{HLDA}}$ pin outputs an “L” while the MCU is placed in a hold state.
	$\overline{\text{RDY}}$	I	VCC2	Bus is placed in a wait state while an “L” signal is applied to the $\overline{\text{RDY}}$ pin.

I: Input O: Output I/O: Input and output

Table 1.17 Pin Functions (100-Pin and 144-Pin Package) (3/4)

Type	Symbol	I/O Type	Supply Voltage	Description
Intelligent I/O	INPC1_0 to INPC1_3	I	VCC1/ VCC2(1)	Input pins for the time measurement function.
	INPC1_4 to INPC1_7	I	VCC1	
	OUTC1_0 to OUTC1_3	O	VCC1/ VCC2(1)	Output pins for the waveform generation function. (OUTC1_6/OUTC2_0 and OUTC1_7/OUTC2_2 assigned to ports 7_0 and 7_1 are N-channel open drain output.)
	OUTC1_4 to OUTC1_7	O	VCC1	
	OUTC2_0 to OUTC2_2	O	VCC1/ VCC2(1)	
	ISCLK0	I/O	VCC1	Clock input/output pins for the intelligent I/O communication function.
	ISCLK1, ISCLK2	I/O	VCC1/ VCC2(1)	
	ISRXD0	I	VCC1	Data input pins for the intelligent I/O communication function.
	ISRXD1, ISRXD2	I	VCC1/ VCC2(1)	
	ISTXD0	O	VCC1	Data output pins for the intelligent I/O communication function. (ISTXD2 assigned to port 7_0 is N-channel open drain output.)
	ISTXD1, ISTXD2	O	VCC1/ VCC2(1)	
	IEIN	I	VCC1/ VCC2(1)	Data input pin for the intelligent I/O communication function.
	IEOUT	O	VCC1/ VCC2(1)	Data output pin for the intelligent I/O communication function. (IEOUT assigned to port 7_0 is N-channel open drain output.)
Reference voltage input	VREF	I	–	The VREF pin supplies the reference voltage to the A/D converter and D/A converter.
A/D converter	AN_0 to AN_7	I	VCC1	Analog input pins for the A/D converter.
	AN0_0 to AN0_7, AN2_0 to AN2_7	I	VCC2	
	$\overline{\text{ADTRG}}$	I	VCC1	External trigger input pin for the A/D converter.
	ANEX0	I/O	VCC1	Extended analog input pin for the A/D converter or output pin in external op-amp connection mode.
	ANEX1	I	VCC1	Extended analog input pin for the A/D converter.
D/A converter	DA0, DA1	O	VCC1	Output pins for the D/A converter.
Real-time port	RTP0_0 to RTP0_3 RTP1_0 to RTP1_3 RTP2_0 to RTP2_3 RTP3_0 to RTP3_3	O	VCC1	These pins function as real-time ports. (RTP0_2 and RTP0_3 are N-channel open drain output.)

I: Input O: Output I/O: Input and output

NOTE:

1. Only VCC1 can be used in the 100-pin package.

Table 4.5 SFR Address Map (5/20)

Address	Register	Symbol	After Reset
00E0h			
00E1h			
00E2h			
00E3h			
00E4h			
00E5h			
00E6h			
00E7h			
00E8h	Group 0 SI/O Receive Buffer Register	G0RB	XXXX XXXXb
00E9h			XXX0 XXXXb
00EAh	Group 0 Transmit Buffer/Receive Data Register	G0TB/G0DR	XXh
00EBh			
00ECh	Group 0 Receive Input Register	G0RI	XXh
00EDh	Group 0 SI/O Communication Mode Register	G0MR	00h
00EEh	Group 0 Transmit Output Register	G0TO	XXh
00EFh	Group 0 SI/O Communication Control Register	G0CR	0000 X011b
00F0h	Group 0 Data Compare Register 0	G0CMP0	XXh
00F1h	Group 0 Data Compare Register 1	G0CMP1	XXh
00F2h	Group 0 Data Compare Register 2	G0CMP2	XXh
00F3h	Group 0 Data Compare Register 3	G0CMP3	XXh
00F4h	Group 0 Data Mask Register 0	G0MSK0	XXh
00F5h	Group 0 Data Mask Register 1	G0MSK1	XXh
00F6h	Communication Clock Select Register	CCS	XXXX 0000b
00F7h			
00F8h	Group 0 Receive CRC Code Register	G0RCRC	XXXXh
00F9h			
00FAh	Group 0 Transmit CRC Code Register	G0TCRC	0000h
00FBh			
00FCh	Group 0 SI/O Expansion Mode Register	G0EMR	00h
00FDh	Group 0 SI/O Extended Receive Control Register	G0ERC	00h
00FEh	Group 0 SI/O Special Communication Interrupt Detection Register	G0IRF	0000 XXXXb
00FFh	Group 0 SI/O Extended Transmit Control Register	G0ETC	0000 0XXXb
0100h	Group 1 Time Measurement/Waveform Generation Register 0	G1TM0/G1PO0	XXXXh
0101h			
0102h	Group 1 Time Measurement/Waveform Generation Register 1	G1TM1/G1PO1	XXXXh
0103h			
0104h	Group 1 Time Measurement/Waveform Generation Register 2	G1TM2/G1PO2	XXXXh
0105h			
0106h	Group 1 Time Measurement/Waveform Generation Register 3	G1TM3/G1PO3	XXXXh
0107h			
0108h	Group 1 Time Measurement/Waveform Generation Register 4	G1TM4/G1PO4	XXXXh
0109h			
010Ah	Group 1 Time Measurement/Waveform Generation Register 5	G1TM5/G1PO5	XXXXh
010Bh			
010Ch	Group 1 Time Measurement/Waveform Generation Register 6	G1TM6/G1PO6	XXXXh
010Dh			
010Eh	Group 1 Time Measurement/Waveform Generation Register 7	G1TM7/G1PO7	XXXXh
010Fh			
0110h	Group 1 Waveform Generation Control Register 0	G1POCR0	0000 X000b
0111h	Group 1 Waveform Generation Control Register 1	G1POCR1	0X00 X000b
0112h	Group 1 Waveform Generation Control Register 2	G1POCR2	0X00 X000b
0113h	Group 1 Waveform Generation Control Register 3	G1POCR3	0X00 X000b
0114h	Group 1 Waveform Generation Control Register 4	G1POCR4	0X00 X000b
0115h	Group 1 Waveform Generation Control Register 5	G1POCR5	0X00 X000b
0116h	Group 1 Waveform Generation Control Register 6	G1POCR6	0X00 X000b
0117h	Group 1 Waveform Generation Control Register 7	G1POCR7	0X00 X000b
0118h	Group 1 Time Measurement Control Register 0	G1TMCR0	00h
0119h	Group 1 Time Measurement Control Register 1	G1TMCR1	00h

X: Undefined
Blank spaces are all reserved. No access is allowed.

Table 4.6 SFR Address Map (6/20)

Address	Register	Symbol	After Reset
011Ah	Group 1 Time Measurement Control Register 2	G1TMCR2	00h
011Bh	Group 1 Time Measurement Control Register 3	G1TMCR3	00h
011Ch	Group 1 Time Measurement Control Register 4	G1TMCR4	00h
011Dh	Group 1 Time Measurement Control Register 5	G1TMCR5	00h
011Eh	Group 1 Time Measurement Control Register 6	G1TMCR6	00h
011Fh	Group 1 Time Measurement Control Register 7	G1TMCR7	00h
0120h 0121h	Group 1 Base Timer Register	G1BT	XXXXh
0122h	Group 1 Base Timer Control Register 0	G1BCR0	00h
0123h	Group 1 Base Timer Control Register 1	G1BCR1	X000 000Xb
0124h	Group 1 Time Measurement Prescaler Register 6	G1TPR6	00h
0125h	Group 1 Time Measurement Prescaler Register 7	G1TPR7	00h
0126h	Group 1 Function Enable Register	G1FE	00h
0127h	Group 1 Function Select Register	G1FS	00h
0128h 0129h	Group 1 SI/O Receive Buffer Register	G1RB	XXXX XXXXb X000 XXXXb
012Ah	Group 1 Transmit Buffer/Receive Data Register	G1TB/G1DR	XXh
012Bh			
012Ch	Group 1 Receive Input Register	G1RI	XXh
012Dh	Group 1 SI/O Communication Mode Register	G1MR	00h
012Eh	Group 1 Transmit Output Register	G1TO	XXh
012Fh	Group 1 SI/O Communication Control Register	G1CR	0000 X011b
0130h	Group 1 Data Compare Register 0	G1CMP0	XXh
0131h	Group 1 Data Compare Register 1	G1CMP1	XXh
0132h	Group 1 Data Compare Register 2	G1CMP2	XXh
0133h	Group 1 Data Compare Register 3	G1CMP3	XXh
0134h	Group 1 Data Mask Register 0	G1MSK0	XXh
0135h	Group 1 Data Mask Register 1	G1MSK1	XXh
0136h			
0137h			
0138h 0139h	Group 1 Receive CRC Code Register	G1RCRC	XXXXh
013Ah 013Bh	Group 1 Transmit CRC Code Register	G1TCRC	0000h
013Ch	Group 1 SI/O Expansion Mode Register	G1EMR	00h
013Dh	Group 1 SI/O Extended Receive Control Register	G1ERC	00h
013Eh	Group 1 SI/O Special Communication Interrupt Detection Register	G1IRF	0000 XXXXb
013Fh	Group 1 SI/O Extended Transmit Control Register	G1ETC	0000 0XXXb
0140h 0141h	Group 2 Waveform Generation Register 0	G2PO0	XXXXh
0142h 0143h	Group 2 Waveform Generation Register 1	G2PO1	XXXXh
0144h 0145h	Group 2 Waveform Generation Register 2	G2PO2	XXXXh
0146h 0147h	Group 2 Waveform Generation Register 3	G2PO3	XXXXh
0148h 0149h	Group 2 Waveform Generation Register 4	G2PO4	XXXXh
014Ah 014Bh	Group 2 Waveform Generation Register 5	G2PO5	XXXXh
014Ch 014Dh	Group 2 Waveform Generation Register 6	G2PO6	XXXXh
014Eh 014Fh	Group 2 Waveform Generation Register 7	G2PO7	XXXXh

X: Undefined
Blank spaces are all reserved. No access is allowed.

Table 4.8 SFR Address Map (8/20)

Address	Register	Symbol	After Reset
01C0h	UART5 Transmit/Receive Mode Register	U5MR	00h
01C1h	UART5 Baud Rate Register	U5BRG	XXh
01C2h	UART5 Transmit Buffer Register	U5TB	XXXXh
01C3h			
01C4h	UART5 Transmit/Receive Control Register 0	U5C0	0000 1000b
01C5h	UART5 Transmit/Receive Control Register 1	U5C1	XXXX 0010b
01C6h	UART5 Receive Buffer Register	U5RB	XXXXh
01C7h			
01C8h	UART6 Transmit/Receive Mode Register	U6MR	00h
01C9h	UART6 Baud Rate Register	U6BRG	XXh
01CAh	UART6 Transmit Buffer Register	U6TB	XXXXh
01CBh			
01CCh	UART6 Transmit/Receive Control Register 0	U6C0	0000 1000b
01CDh	UART6 Transmit/Receive Control Register 1	U6C1	XXXX 0010b
01CEh	UART6 Receive Buffer Register	U6RB	XXXXh
01CFh			
01D0h	UART5, UART6 Transmit/Receive Control Register	U56CON	X000 0000b
01D1h	UART5, UART6 Input Pin Function Select Register	U56IS	X000 X000b
01D2h			
01D3h			
01D4h			
01D5h			
01D6h			
01D7h			
01D8h	RTP Output Buffer Register 0	RTP0R	XXh
01D9h	RTP Output Buffer Register 1	RTP1R	XXh
01DAh	RTP Output Buffer Register 2	RTP2R	XXh
01DBh	RTP Output Buffer Register 3	RTP3R	XXh
01DCh			
01DDh			
01DEh			
01DFh			
01E0h	CAN0 Message Slot Buffer 0 Standard ID0(1)(2)	C0SLOT0_0	XXh
01E1h	CAN0 Message Slot Buffer 0 Standard ID1(1)(2)	C0SLOT0_1	XXh
01E2h	CAN0 Message Slot Buffer 0 Extended ID0(1)(2)	C0SLOT0_2	XXh
01E3h	CAN0 Message Slot Buffer 0 Extended ID1(1)(2)	C0SLOT0_3	XXh
01E4h	CAN0 Message Slot Buffer 0 Extended ID2(1)(2)	C0SLOT0_4	XXh
01E5h	CAN0 Message Slot Buffer 0 Data Length Code(1)(2)	C0SLOT0_5	XXh
01E6h	CAN0 Message Slot Buffer 0 Data 0(1)(2)	C0SLOT0_6	XXh
01E7h	CAN0 Message Slot Buffer 0 Data 1(1)(2)	C0SLOT0_7	XXh
01E8h	CAN0 Message Slot Buffer 0 Data 2(1)(2)	C0SLOT0_8	XXh
01E9h	CAN0 Message Slot Buffer 0 Data 3(1)(2)	C0SLOT0_9	XXh
01EAh	CAN0 Message Slot Buffer 0 Data 4(1)(2)	C0SLOT0_10	XXh
01EBh	CAN0 Message Slot Buffer 0 Data 5(1)(2)	C0SLOT0_11	XXh
01ECh	CAN0 Message Slot Buffer 0 Data 6(1)(2)	C0SLOT0_12	XXh
01EDh	CAN0 Message Slot Buffer 0 Data 7(1)(2)	C0SLOT0_13	XXh
01EEh	CAN0 Message Slot Buffer 0 Time Stamp High-Order(1)(2)	C0SLOT0_14	XXh
01EFh	CAN0 Message Slot Buffer 0 Time Stamp Low-Order(1)(2)	C0SLOT0_15	XXh

X: Undefined
Blank spaces are all reserved. No access is allowed.

NOTES:

1. The CAN-associated registers (allocated in addresses 01E0h to 02BFh) cannot be used in M32C/87B. In M32C/87A, only CAN0-associated registers can be used.
2. Set the PM13 bit in the PM1 register to 1 (2 wait states for SFR area) before accessing the CAN-associated registers.

Table 4.9 SFR Address Map (9/20)

Address	Register[2][3]	Symbol	After Reset
01F0h	CAN0 Message Slot Buffer 1 Standard ID0	C0SLOT1_0	XXh
01F1h	CAN0 Message Slot Buffer 1 Standard ID1	C0SLOT1_1	XXh
01F2h	CAN0 Message Slot Buffer 1 Extended ID0	C0SLOT1_2	XXh
01F3h	CAN0 Message Slot Buffer 1 Extended ID1	C0SLOT1_3	XXh
01F4h	CAN0 Message Slot Buffer 1 Extended ID2	C0SLOT1_4	XXh
01F5h	CAN0 Message Slot Buffer 1 Data Length Code	C0SLOT1_5	XXh
01F6h	CAN0 Message Slot Buffer 1 Data 0	C0SLOT1_6	XXh
01F7h	CAN0 Message Slot Buffer 1 Data 1	C0SLOT1_7	XXh
01F8h	CAN0 Message Slot Buffer 1 Data 2	C0SLOT1_8	XXh
01F9h	CAN0 Message Slot Buffer 1 Data 3	C0SLOT1_9	XXh
01FAh	CAN0 Message Slot Buffer 1 Data 4	C0SLOT1_10	XXh
01FBh	CAN0 Message Slot Buffer 1 Data 5	C0SLOT1_11	XXh
01FCh	CAN0 Message Slot Buffer 1 Data 6	C0SLOT1_12	XXh
01FDh	CAN0 Message Slot Buffer 1 Data 7	C0SLOT1_13	XXh
01FEh	CAN0 Message Slot Buffer 1 Time Stamp High-Order	C0SLOT1_14	XXh
01FFh	CAN0 Message Slot Buffer 1 Time Stamp Low-Order	C0SLOT1_15	XXh
0200h	CAN0 Control Register 0	C0CTLR0	XX01 0X01b[1]
0201h			XXXX 0000b[1]
0202h	CAN0 Status Register	C0STR	0000 0000b[1]
0203h			X000 0X01b[1]
0204h	CAN0 Extended ID Register	C0IDR	0000h[1]
0205h			
0206h	CAN0 Configuration Register	C0CONR	0000 XXXXb[1]
0207h			0000 0000b[1]
0208h	CAN0 Time Stamp Register	C0TSR	0000h[1]
0209h			
020Ah	CAN0 Transmit Error Count Register	C0TEC	00h[1]
020Bh	CAN0 Receive Error Count Register	C0REC	00h[1]
020Ch	CAN0 Slot Interrupt Status Register	C0SISTR	0000h[1]
020Dh			
020Eh			
020Fh			
0210h	CAN0 Slot Interrupt Mask Register	C0SIMKR	0000h[1]
0211h			
0212h			
0213h			
0214h	CAN0 Error Interrupt Mask Register	C0EIMKR	XXXX X000b[1]
0215h	CAN0 Error Interrupt Status Register	C0EISTR	XXXX X000b[1]
0216h	CAN0 Error Source Register	C0EFR	00h[1]
0217h	CAN0 Baud Rate Prescaler	C0BRP	0000 0001b[1]
0218h			
0219h	CAN0 Mode Register	C0MDR	XXXX XX00b[1]
021Ah			
021Bh			
021Ch			
021Dh			
021Eh			
021Fh			

X: Undefined
Blank spaces are all reserved. No access is allowed.
NOTES:
1. Values are obtained by setting the SLEEP bit in the C0SLPR register to “1” (sleep mode exited) after reset and supplying a clock to the CAN module.
2. The CAN-associated registers (allocated in addresses 01E0h to 02BFh) cannot be used in M32C/87B. In M32C/87A, only CAN0-associated registers can be used.
3. Set the PM13 bit in the PM1 register to 1 (2 wait states for SFR area) before accessing the CAN-associated registers.

Table 4.10 SFR Address Map (10/20)

Address	Register[3][4]	Symbol	After Reset
0220h	CAN0 Single Shot Control Register	C0SSCTLR	0000h[1][2]
0221h			
0222h			
0223h			
0224h	CAN0 Single Shot Status Register	C0SSSTR	0000h[1][2]
0225h			
0226h			
0227h			
0228h	CAN0 Global Mask Register Standard ID0	C0GMR0	XXX0 0000b[1][2]
0229h	CAN0 Global Mask Register Standard ID1	C0GMR1	XX00 0000b[1][2]
022Ah	CAN0 Global Mask Register Extended ID0	C0GMR2	XXXX 0000b[1][2]
022Bh	CAN0 Global Mask Register Extended ID1	C0GMR3	00h[1][2]
022Ch	CAN0 Global Mask Register Extended ID2	C0GMR4	XX00 0000b[1][2]
022Dh			
022Eh			
022Fh			
0230h	CAN0 Message Slot 0 Control Register / CAN0 Local Mask Register A Standard ID0	C0MCTL0 / C0LMAR0	0000 0000b[1][2]/ XXX0 0000b[1][2]
0231h	CAN0 Message Slot 1 Control Register / CAN0 Local Mask Register A Standard ID1	C0MCTL1 / C0LMAR1	0000 0000b[1][2]/ XX00 0000b[1][2]
0232h	CAN0 Message Slot 2 Control Register / CAN0 Local Mask Register A Extended ID0	C0MCTL2 / C0LMAR2	0000 0000b[1][2]/ XXXX 0000b[1][2]
0233h	CAN0 Message Slot 3 Control Register / CAN0 Local Mask Register A Extended ID1	C0MCTL3 / C0LMAR3	00h[1][2]/ 00h[1][2]
0234h	CAN0 Message Slot 4 Control Register / CAN0 Local Mask Register A Extended ID2	C0MCTL4 / C0LMAR4	0000 0000b[1][2]/ XX00 0000b[1][2]
0235h	CAN0 Message Slot 5 Control Register	C0MCTL5	00h[1][2]
0236h	CAN0 Message Slot 6 Control Register	C0MCTL6	00h[1][2]
0237h	CAN0 Message Slot 7 Control Register	C0MCTL7	00h[1][2]
0238h	CAN0 Message Slot 8 Control Register / CAN0 Local Mask Register B Standard ID0	C0MCTL8 / C0LMBR0	0000 0000b[1][2]/ XXX0 0000b[1][2]
0239h	CAN0 Message Slot 9 Control Register / CAN0 Local Mask Register B Standard ID1	C0MCTL9 / C0LMBR1	0000 0000b[1][2]/ XX00 0000b[1][2]
023Ah	CAN0 Message Slot 10 Control Register / CAN0 Local Mask Register B Extended ID0	C0MCTL10 / C0LMBR2	0000 0000b[1][2]/ XXXX 0000b[1][2]
023Bh	CAN0 Message Slot 11 Control Register / CAN0 Local Mask Register B Extended ID1	C0MCTL11 / C0LMBR3	00h[1][2]/ 00h[1][2]
023Ch	CAN0 Message Slot 12 Control Register / CAN0 Local Mask Register B Extended ID2	C0MCTL12 / C0LMBR4	0000 0000b[1][2]/ XX00 0000b[1][2]
023Dh	CAN0 Message Slot 13 Control Register	C0MCTL13	00h[1][2]
023Eh	CAN0 Message Slot 14 Control Register	C0MCTL14	00h[1][2]
023Fh	CAN0 Message Slot 15 Control Register	C0MCTL15	00h[1][2]
0240h	CAN0 Slot Buffer Select Register	C0SBS	00h[2]
0241h	CAN0 Control Register 1	C0CTLR1	X000 00XXb[2]
0242h	CAN0 Sleep Control Register	C0SLPR	XXXX XXX0b
0243h			
0244h	CAN0 Acceptance Filter Support Register	C0AFS	0000 0000b[2]
0245h			0000 0001b[2]
0246h			
0247h			
0248h			
0249h			
024Ah to 024Fh			

X: Undefined
Blank spaces are all reserved. No access is allowed.
NOTES:

1. The BANKSEL bit in the C0CTLR1 register can switch functions for addresses 0220h to 023Fh.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to “1” (sleep mode exited) after reset and supplying a clock to the CAN module.
3. The CAN-associated registers (allocated in addresses 01E0h to 02BFh) cannot be used in M32C/87B. In M32C/87A, only CAN0-associated registers can be used.
4. Set the PM13 bit in the PM1 register to 1 (2 wait states for SFR area) before accessing the CAN-associated registers.

Table 4.13 SFR Address Map (13/20)

Address	Register[3][4]	Symbol	After Reset
02B0h	CAN1 Message Slot 0 Control Register / CAN1 Local Mask Register A Standard ID0	C1MCTL0 / C1LMAR0	0000 0000b[1][2]/ XXX0 0000b[1][2]
02B1h	CAN1 Message Slot 1 Control Register / CAN1 Local Mask Register A Standard ID1	C1MCTL1 / C1LMAR1	0000 0000b[1][2]/ XX00 0000b[1][2]
02B2h	CAN1 Message Slot 2 Control Register / CAN1 Local Mask Register A Extended ID0	C1MCTL2 / C1LMAR2	0000 0000b[1][2]/ XXXX 0000b[1][2]
02B3h	CAN1 Message Slot 3 Control Register / CAN1 Local Mask Register A Extended ID1	C1MCTL3 / C1LMAR3	00h[1][2]/ 00h[1][2]
02B4h	CAN1 Message Slot 4 Control Register / CAN1 Local Mask Register A Extended ID2	C1MCTL4 / C1LMAR4	0000 0000b[1][2]/ XX00 0000b[1][2]
02B5h	CAN1 Message Slot 5 Control Register	C1MCTL5	00h[1][2]
02B6h	CAN1 Message Slot 6 Control Register	C1MCTL6	00h[1][2]
02B7h	CAN1 Message Slot 7 Control Register	C1MCTL7	00h[1][2]
02B8h	CAN1 Message Slot 8 Control Register / CAN1 Local Mask Register B Standard ID0	C1MCTL8 / C1LMBR0	0000 0000b[1][2]/ XXX0 0000b[1][2]
02B9h	CAN1 Message Slot 9 Control Register / CAN1 Local Mask Register B Standard ID1	C1MCTL9 / C1LMBR1	0000 0000b[1][2]/ XX00 0000b[1][2]
02BAh	CAN1 Message Slot 10 Control Register / CAN1 Local Mask Register B Extended ID0	C1MCTL10 / C1LMBR2	0000 0000b[1][2]/ XXXX 0000b[1][2]
02BBh	CAN1 Message Slot 11 Control Register / CAN1 Local Mask Register B Extended ID1	C1MCTL11 / C1LMBR3	00h[1][2]/ 00h[1][2]
02BCh	CAN1 Message Slot 12 Control Register / CAN1 Local Mask Register B Extended ID2	C1MCTL12 / C1LMBR4	0000 0000b[1][2]/ XX00 0000b[1][2]
02BDh	CAN1 Message Slot 13 Control Register	C1MCTL13	00h[1][2]
02BEh	CAN1 Message Slot 14 Control Register	C1MCTL14	00h[1][2]
02BFh	CAN1 Message Slot 15 Control Register	C1MCTL15	00h[1][2]

X: Undefined
Blank spaces are all reserved. No access is allowed.
NOTES:
1. The BANKSEL bit in the C1CTLR1 register can switch functions for addresses 02A0h to 02BFh.
2. Values are obtained by setting the SLEEP bit in the C1SLPR register to “1” (sleep mode exited) after reset and supplying a clock to the CAN module.
3. The CAN-associated registers (allocated in addresses 01E0h to 02BFh) cannot be used in M32C/87B. In M32C/87A, only CAN0-associated registers can be used.
4. Set the PM13 bit in the PM1 register to 1 (2 wait states for SFR area) before accessing the CAN-associated registers.

Table 4.15 SFR Address Map (15/20)

Address	Register	Symbol	After Reset
02F0h			
02F1h			
02F2h			
02F3h			
02F4h	UART4 Special Mode Register 4	U4SMR4	00h
02F5h	UART4 Special Mode Register 3	U4SMR3	00h
02F6h	UART4 Special Mode Register 2	U4SMR2	00h
02F7h	UART4 Special Mode Register	U4SMR	00h
02F8h	UART4 Transmit/Receive Mode Register	U4MR	00h
02F9h	UART4 Baud Rate Register	U4BRG	XXh
02FAh	UART4 Transmit Buffer Register	U4TB	XXXXh
02FBh			
02FCh	UART4 Transmit/Receive Control Register 0	U4C0	0000 1000b
02FDh	UART4 Transmit/Receive Control Register 1	U4C1	0000 0010b
02FEh	UART4 Receive Buffer Register	U4RB	XXXXh
02FFh			
0300h	Timer B3, B4, B5 Count Start Register	TBSR	000X XXXXb
0301h			
0302h	Timer A11 Register	TA11	XXXXh
0303h			
0304h	Timer A21 Register	TA21	XXXXh
0305h			
0306h	Timer A41 Register	TA41	XXXXh
0307h			
0308h	Three-Phase PWM Control Register 0	INVC0	00h
0309h	Three-Phase PWM Control Register 1	INVC1	00h
030Ah	Three-Phase Output Buffer Register 0	IDB0	XX11 1111b
030Bh	Three-Phase Output Buffer Register 1	IDB1	XX11 1111b
030Ch	Dead Time Timer	DTT	XXh
030Dh	Timer B2 Interrupt Generation Frequency Set Counter	ICTB2	XXh
030Eh			
030Fh			
0310h	Timer B3 Register	TB3	XXXXh
0311h			
0312h	Timer B4 Register	TB4	XXXXh
0313h			
0314h	Timer B5 Register	TB5	XXXXh
0315h			
0316h			
0317h			
0318h			
0319h			
031Ah			
031Bh	Timer B3 Mode Register	TB3MR	00XX 0000b
031Ch	Timer B4 Mode Register	TB4MR	00XX 0000b
031Dh	Timer B5 Mode Register	TB5MR	00XX 0000b
031Eh	External Interrupt Source Select Register 1(1)	IFSRA	00h
031Fh	External Interrupt Source Select Register	IFSR	00h

X: Undefined
Blank spaces are all reserved. No access is allowed.
NOTE:
1. The IFSRA register is included in the 144-pin package only.

VCC1 = VCC2 = 5V

Table 5.8 A/D Conversion Characteristics
(VCC1 = VCC2 = AVCC = VREF = 4.2 to 5.5 V, VSS = AVSS = 0 V, Topr = -20 to 85°C, f(CPU) = 32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition		Standard			Unit
				Min.	Typ.	Max.	
–	Resolution	VREF = VCC1				10	Bits
INL	Integral nonlinearity error	VREF = VCC1 = VCC2 = 5 V	AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, AN15_0 to AN15_7, ANEX0, ANEX1			±3	LSB
			External op-amp connection mode			±7	LSB
DNL	Differential nonlinearity error					±1	LSB
–	Offset error					±3	LSB
–	Gain error					±3	LSB
RLADDER	Resistor ladder	VREF = VCC1		8		40	kΩ
tCONV	10-bit conversion time(1)(2)			2.06			µs
tCONV	8-bit conversion time(1)(2)			1.75			µs
tSAMP	Sampling time(1)			0.188			µs
VREF	Reference voltage			2		VCC1	V
VIA	Analog input voltage			0		VREF	V

NOTES:
1. The value is obtained when ϕAD frequency is at 16 MHz. Keep ϕAD frequency at 16 MHz or lower.
2. With using the sample and hold function

Table 5.9 D/A Conversion Characteristics
(VCC1 = VCC2 = VREF = 4.2 to 5.5 V, VSS = AVSS = 0 V, Topr = -20 to 85°C, f(CPU) = 32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
–	Resolution				8	Bits
–	Absolute accuracy				1.0	%
tsu	Setup time				3	µs
RO	Output resistance		4	10	20	kΩ
IVREF	Reference power supply input current	(note 1)			1.5	mA

NOTE:
1. Measured when one D/A converter is used, and the DAi register (i = 0, 1) of the unused D/A converter is set to 00h. The current flown into the resistor ladder in the A/D converter is excluded. IVREF flows even if the VCUT bit in the AD0CON1 register is set to 0 (VREF not connected)

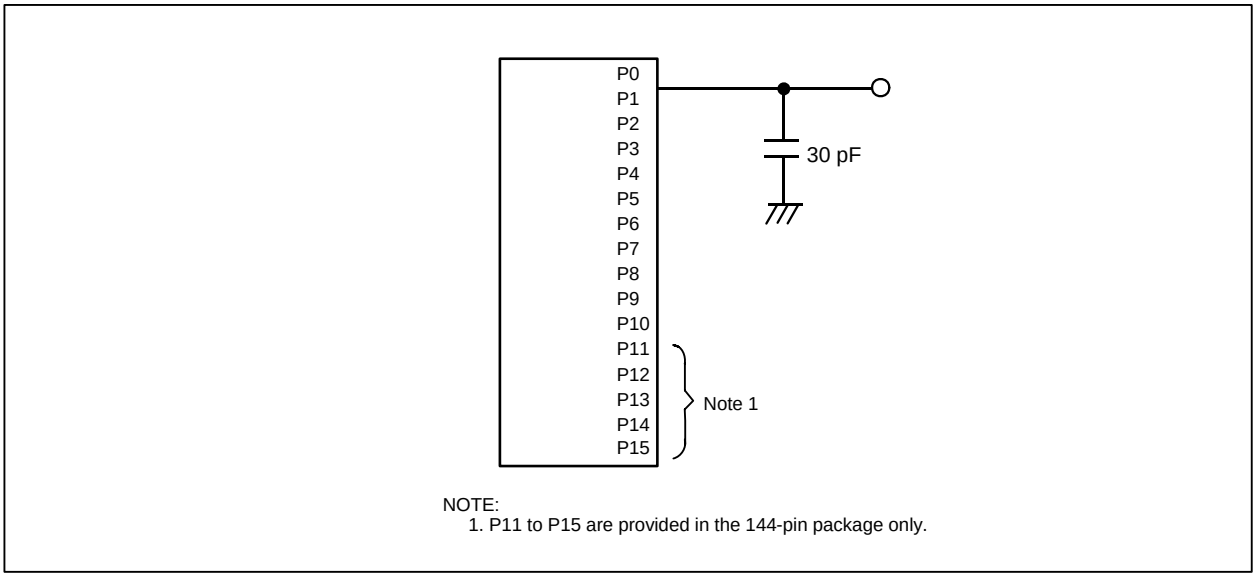


Figure 5.2 P0 to P15 Measurement Circuit

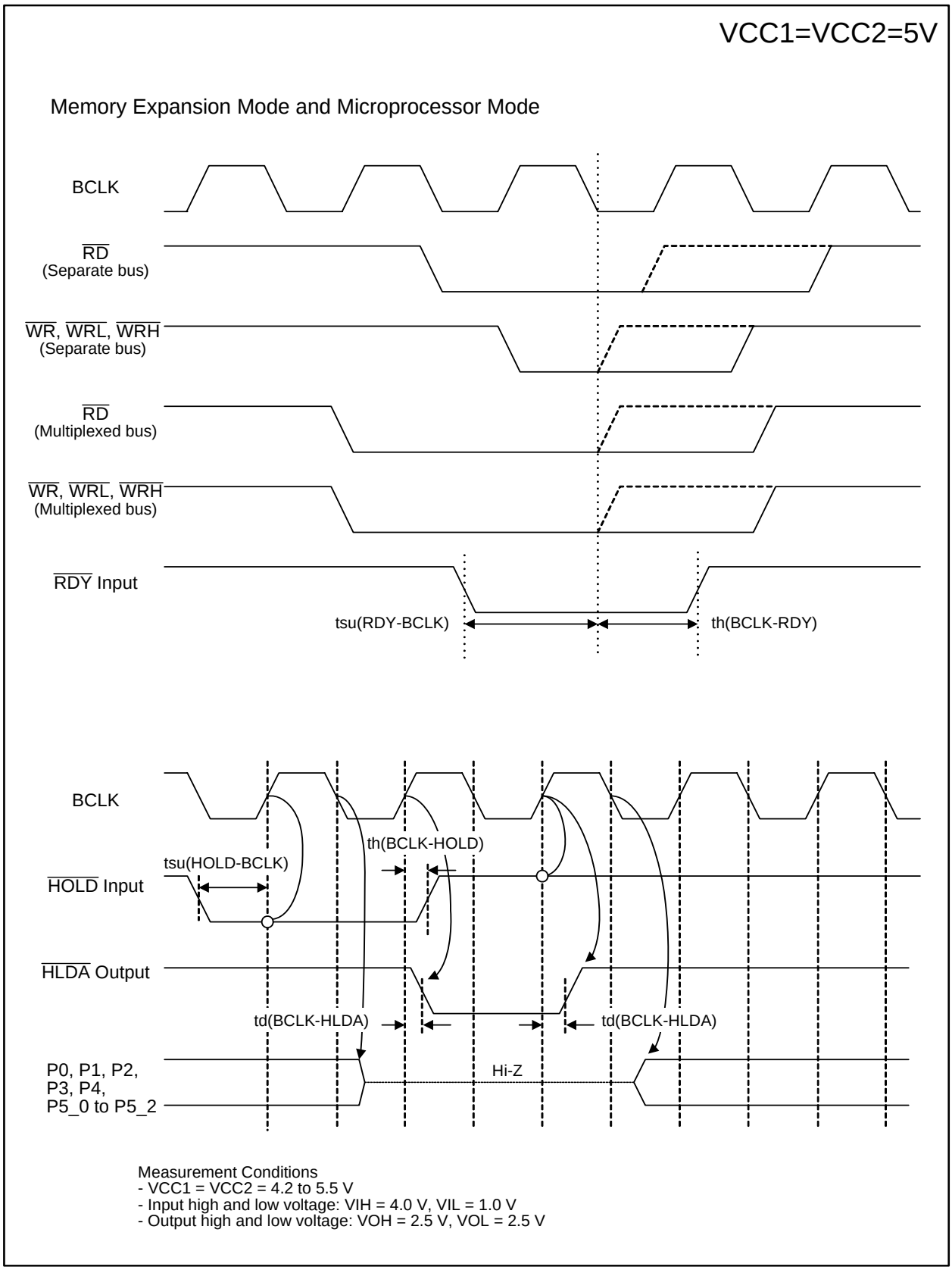


Figure 5.4 VCC1 = VCC2 = 5 V Timing Diagram (2/4)

VCC1 = VCC2 = 3.3 V

Timing Requirements
(VCC1 = VCC2 = 3.0 to 3.6 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.51 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tac1(RD-DB)	Data input access time (RD standard)		(note 1)	ns
tac1(AD-DB)	Data input access time (AD standard, CS standard)		(note 1)	ns
tac2(RD-DB)	Data input access time (RD standard, when accessing a space with the multiplexed bus)		(note 1)	ns
tac2(AD-DB)	Data input access time (AD standard, when accessing a space with the multiplexed bus)		(note 1)	ns
tsu(DB-BCLK)	Data input setup time	30		ns
tsu(RDY-BCLK)	$\overline{\text{RDY}}$ input setup time	40		ns
tsu(HOLD-BCLK)	$\overline{\text{HOLD}}$ input setup time	60		ns
th(RD-DB)	Data input hold time	0		ns
th(BCLK-RDY)	$\overline{\text{RDY}}$ input hold time	0		ns
th(BCLK-HOLD)	$\overline{\text{HOLD}}$ input hold time	0		ns
td(BCLK-HLDA)	$\overline{\text{HLDA}}$ output delay time		25	ns

NOTE:
1. Values, which depend on BCLK frequency and external bus cycles, can be obtained from the following equations. Insert wait states or lower the operation frequency, f(BCLK), if the calculated value is negative.

$$\text{tac1(RD-DB)} = \frac{10^9 \times m}{f(BCLK) \times 2} - 35\ [ns]$$ (if external bus cycle is $a\phi + b\phi$, $m = (b \times 2) + 1$)

$$\text{tac1(AD-DB)} = \frac{10^9 \times n}{f(BCLK)} - 35\ [ns]$$ (if external bus cycle is $a\phi + b\phi$, $n = a + b$)

$$\text{tac2(RD-DB)} = \frac{10^9 \times m}{f(BCLK) \times 2} - 35\ [ns]$$ (if external bus cycle is $a\phi + b\phi$, $m = (b \times 2) - 1$)

$$\text{tac2(AD-DB)} = \frac{10^9 \times p}{f(BCLK) \times 2} - 35\ [ns]$$ (if external bus cycle is $a\phi + b\phi$, $p = \{(a + b - 1) \times 2\} + 1$)

VCC1 = VCC2 = 3.3 V

Switching Characteristics
(VCC1 = VCC2 = 3.0 to 3.6 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.53 Memory Expansion Mode and Microprocessor Mode (when accessing external memory space with multiplexed bus)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min.	Max.	
td(BCLK-AD)	Address output delay time	See Figure 5.2		18	ns
th(BCLK-AD)	Address output hold time (BCLK standard)		-3		ns
th(RD-AD)	Address output hold time (RD standard)(5)		(note 1)		ns
th(WR-AD)	Address output hold time (WR standard)(5)		(note 1)		ns
td(BCLK-CS)	Chip-select signal output delay time			18	ns
th(BCLK-CS)	Chip-select signal output hold time (BCLK standard)		-3		ns
th(RD-CS)	Chip-select signal output hold time (RD standard)(5)		(note 1)		ns
th(WR-CS)	Chip-select signal output hold time (WR standard)(5)		(note 1)		ns
td(BCLK-RD)	RD signal output delay time			18	ns
th(BCLK-RD)	RD signal output hold time		-5		ns
td(BCLK-WR)	WR signal output delay time			18	ns
th(BCLK-WR)	WR signal output hold time		0		ns
td(DB-WR)	Data output delay time (WR standard)		(note 2)		ns
th(WR-DB)	Data output hold time (WR standard)(5)		(note 1)		ns
td(BCLK-ALE)	ALE signal output delay time (BCLK standard)			18	ns
th(BCLK-ALE)	ALE signal output hold time (BCLK standard)		-2		ns
td(AD-ALE)	ALE signal output delay time (address standard)		(note 3)		ns
th(ALE-AD)	ALE signal output hold time (address standard)		(note 4)		ns
tdz(RD-AD)	Address output float start time			8	ns

NOTES:

1. Values, which depend on BCLK frequency, can be obtained from the following equations.

$$th(RD\text{-}AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \text{ [ns]}$$

$$th(WR\text{-}AD) = \frac{10^9}{f(BCLK) \times 2} - 15 \text{ [ns]}$$

$$th(RD\text{-}CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \text{ [ns]}$$

$$th(WR\text{-}CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \text{ [ns]}$$

$$th(WR\text{-}DB) = \frac{10^9}{f(BCLK) \times 2} - 20 \text{ [ns]}$$

2. Values, which depend on BCLK frequency and external bus cycles, can be obtained from the following equation.

$$td(DB\text{-}WR) = \frac{10^9 \times m}{f(BCLK) \times 2} - 25 \text{ [ns]}$$ (if external bus cycle is $a\phi + b\phi$, $m = (b \times 2) - 1$)

3. Values, which depend on BCLK frequency and external bus cycles, can be obtained from the following equation.

$$td(AD\text{-}ALE) = \frac{10^9 \times n}{f(BCLK) \times 2} - 20 \text{ [ns]}$$ (if external bus cycle is $a\phi + b\phi$, $n = a$)

4. Values, which depend on BCLK frequency and external bus cycles, can be obtained from the following equation.

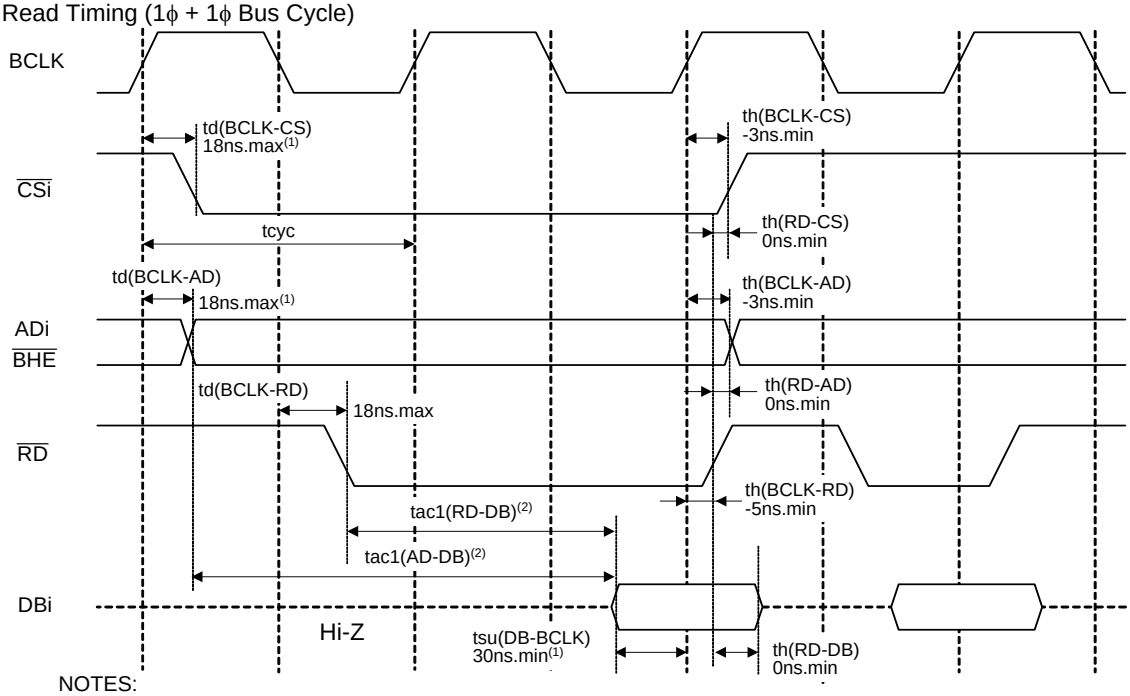
$$th(ALE\text{-}AD) = \frac{10^9 \times n}{f(BCLK) \times 2} - 20 \text{ [ns]}$$ (if external bus cycle is $a\phi + b\phi$, $n = a$)

5. tc [ns] is added when recovery cycle is inserted.

Memory Expansion Mode and Microprocessor Mode
(when accessing an external memory space)

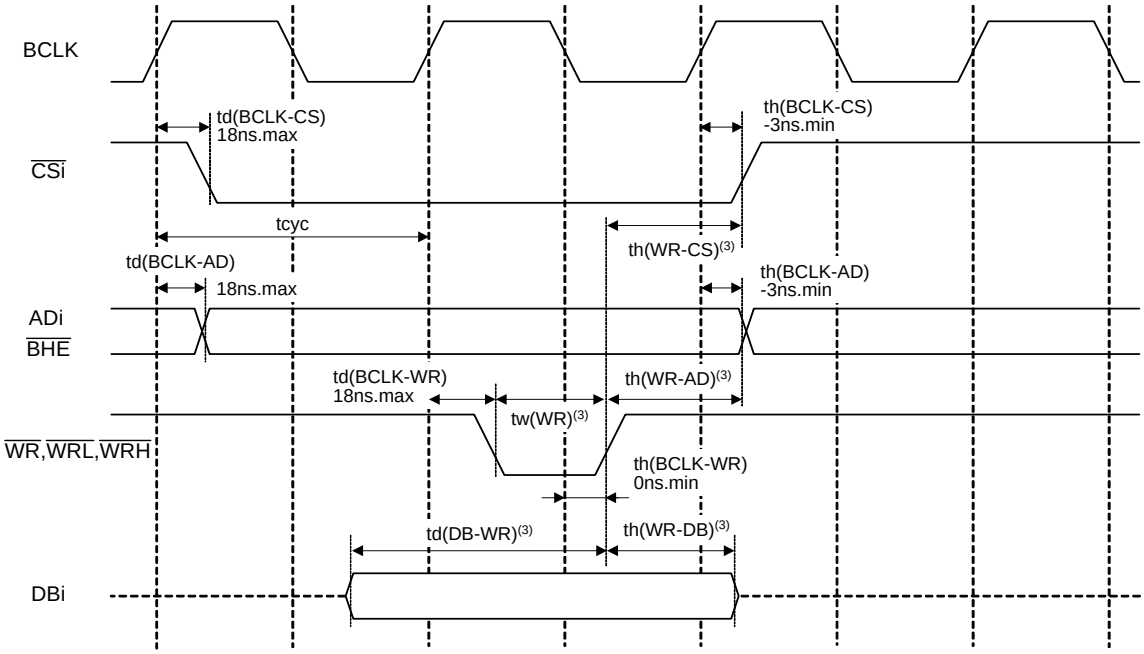
VCC1=VCC2=3.3V

Read Timing (1ϕ + 1ϕ Bus Cycle)



NOTES:
1. Values guaranteed only when the MCU is used stand-alone.
   A maximum of 35 ns is guaranteed for td(BCLK-AD) + tsu(DB-BCLK).
2. Varies with operation frequency:
   tac1(RD-DB) = (tcyc / 2 x m - 35) ns.max (if external bus cycle aϕ + bϕ, m = (b x 2) + 1)
   tac1(AD-DB) = (tcyc x n - 35) ns.max (if external bus cycle aϕ + bϕ, n = a + b)

Write Timing (1ϕ + 1ϕ Bus Cycle)



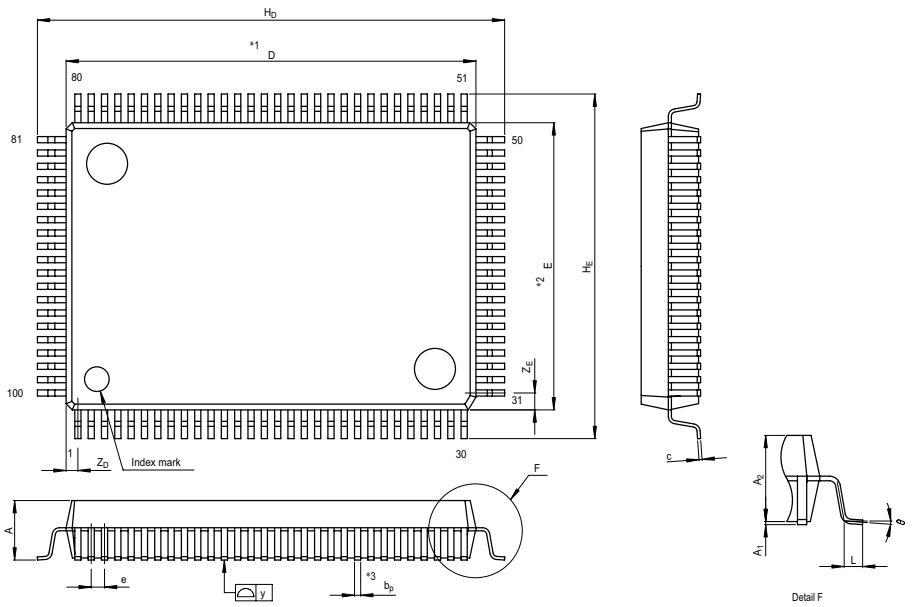
NOTES:
3. Varies with operation frequency:
   td(DB-WR) = (tcyc x m - 20) ns.min
   (if external bus cycle aϕ + bϕ, m = b)
   th(WR-DB) = (tcyc / 2 - 20) ns.min
   th(WR-AD) = (tcyc / 2 - 15) ns.min
   th(WR-CS) = (tcyc / 2 - 10) ns.min
   tw(WR) = (tcyc / 2 x n - 15) ns.min
   (if external bus cycle aϕ + bϕ, n = (b x 2) - 1)

Measurement Conditions:
- VCC1 = VCC2 = 3.0 to 3.6 V
- Input high and low voltage: VIH = 1.5 V, VIL = 0.5 V
- Output high and low voltage: VOH = 1.5 V, VOL = 1.5 V

$$tcyc = \frac{10^9}{f(BCLK)}$$

Figure 5.9 VCC1 = VCC2 = 3.3 V Timing Diagram (3/4)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-QFP100-14x20-0.65	PRQP0100JB-A	100P6S-A	1.6g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.8	20.0	20.2
E	13.8	14.0	14.2
A_2	—	2.8	—
H_D	22.5	22.8	23.1
H_E	16.5	16.8	17.1
A	—	—	3.05
A_1	0	0.1	0.2
b_p	0.25	0.3	0.4
c	0.13	0.15	0.2
θ	0°	—	10°
e	0.5	0.65	0.8
y	—	—	0.10
Z_D	—	0.575	—
Z_E	—	0.825	—
L	0.4	0.6	0.8

REVISION HISTORY	M32C/87 Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.50	Dec.16, 04	–	New Document
1.00	Jul.14, 05	–	**M32C/87A and M32C/87B** added
		–	Package code changed: 144P6Q-A to PLQP0144KA-A, 100P6Q-A to PLQP0100KB-A, 100P6S-A to PRQP0100JB-A
		–	"Low Voltage Detection Reset" changed to "Brown-out Detection Reset"
			Overview
		2	• **Table 1.2 M32C/87 Group Performance (144-Pin Package)** M32C/87A and M32C/87B performance added to the CAN module performance; Power Consumption performance released
		3	• **Table 1.2 M32C/87 Group Performance (100-Pin Package)** M32C/87A and M32C/87B performance added to the CAN module performance; Power Consumption performance released
		4	• **Figure 1.1 M32C/87 Group Block Diagram** Note 4 deleted; note 5 added
		7	• **Figure 1.3 Pin Assignment for 144-Pin Package** Note 15 added
		8	• **Table 1.4 Pin Characteristics for 144-Pin Package** Note 1 added
		11	• **Figure 1.4 Pin Assignment for 100-Pin Package** Note 19 added
		12	• **Figure 1.5 Pin Assignment for 100-Pin Package** Note 15 added
		13	• **Table 1.5 Pin Characteristics for 100-Pin Package** Note 1 added
		17	• **Table 1.6 Pin Description** Note 2 added
			Memory
		22	• **Figure 3.1 Memory Map** Note 3 changed
			Special Function Register (SFR)
		26	• The RLVL register Value after reset modified
		26	• The IIO0IR to IIO11IR registers Value after reset modified
		27 to 30	• Name of the registers assosiated to Intelligent I/O changed
		27	• The G0RB register Value after reset modified
		27	• The G1BCR0 and G1BCR1 registers Value after reset modified
		29	• The G0CR register Value after reset modified
		32 to 37	• Note added to the CAN-associated registers
		40	• The TCSPR register Value after reset modified; note 1 added
		41	• The AD00 register Value after reset modified
		42	• The PSC register Value after reset modified
		42	• The PS2 register Value after reset modified
		43	• The PCR register Value after reset modified
		44	• The PSD1 register Value after reset modified
		45	• The PCR register Value after reset modified
			Electrical Characteristics
		48	• **Table 5.2 Electrical Characteristics** Parameter f(BCLK) and its values added; min. and max. values for f(RING) added
		49	• **Table 5.3 Electrical Characteristics** V_{OH} values modified**;** R_{PULLUP} value modified
		50	• **Table 5.3 Electrical Characteristics (Continued)** Measurement Condition and standard values for ICC added and some released
		52	• **Table 5.6 Flash Memory Version Electrical Characteristics** Word Program Time and Lock bit Program Time values modified; parameter All-Unlocked-Block-Erase Time deleted; note 1 deleted
		54	• **Table 5.10 Memory Expansion Mode and Microprocessor Mode** *tac1(RD-DB)* expression on note 1 modified; *tac2(RD-DB)* expression on note 1 added

REVISION HISTORY	M32C/87 Group Datasheet

Rev.	Date	Description	
		Page	Summary
		46	**Special Function Registers (SFRs)** • **Table 4.20** A value of After Reset column in 03FFh modified