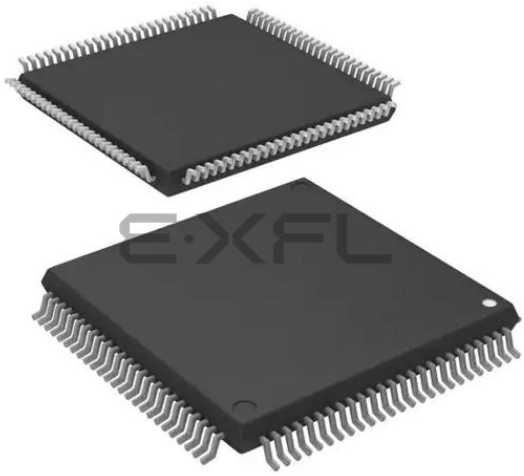

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M32C/80
Core Size	16/32-Bit
Speed	32MHz
Connectivity	CANbus, EBI/EMI, I²C, IEBus, IrDA, SIO, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	85
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30879fkagp-u3

Table 1.2 Specifications (144-Pin Package) (2/2)

Item	Function	Specification
Serial Interface	UART0 to UART4	Clock synchronous/asynchronous × 5 I^2C bus, special mode 2, GCI mode, SIM mode, IrDA mode(2), IEBus (optional)(1)(3)
	UART5, UART6	Clock synchronous/asynchronous × 2
A/D Converter		10-bit resolution × 34 channels (in single-chip mode) 10-bit resolution × 18 channels (in memory expansion mode and microprocessor mode) Including sample and hold function
D/A Converter		8-bit resolution × 2 channels
CRC Calculation Circuit		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) compliant
X/Y Converter		16 bits x 16 bits
Intelligent I/O		16-bit timer × 2 • Time measurement function (input capture): 8 channels • Waveform generation function (output compare): 16 channels • Communication function: Clock synchronous mode, clock asynchronous mode, HDLC data processing mode, IEBus (optional)(1)(3) • 2-phase pulse signal processing (2-phase encoder input) × 1
ROM Correction Function		Address match interrupt × 8
CAN modules		Supporting CAN 2.0B specification M32C/87: 16 slots × 2 channels, M32C/87A: 16 slots × 1 channel M32C/87B: none
I/O Ports	Programmable I/O ports	• Input only: 1 • CMOS I/O: 121 with selectable pull-up resistor • N channel open drain ports: 2
Flash Memory		• Erase and program voltage: 3.3 V ± 0.3 V or 5.0 V ± 0.5 V • Erase and program endurance: 100 times (all areas) • Program security: ROM code protect and ID code check • Debug functions: On-chip debug and on-board flash reprogram
Operating Frequency/Supply Voltage		32 MHz: VCC1 = 4.2 to 5.5 V, VCC2 = 3.0 V to VCC1 24 MHz: VCC1 = 3.0 to 5.5 V, VCC2 = 3.0 V to VCC1
Current Consumption		32 mA (32 MHz, VCC1 = VCC2 = 5 V) 23 mA (24 MHz, VCC1 = VCC2 = 3.3 V) 45 µA (approx. 1 MHz, VCC1 = VCC2 = 3.3 V, on-chip oscillator low-power consumption mode → wait mode) 0.8 µA (VCC1 = VCC2 = 3.3 V, stop mode)
Operating Ambient Temperature (°C)		-20 to 85°C, -40 to 85°C (optional)(3)
Package		144-pin LQFP (PLQP0144KA-A)

NOTES:
1. IEBus is a registered trademark of NEC Electronics Corporation.
2. Available in UART0.
3. Please contact a Renesas sales office for optional features.

Table 1.12 100-Pin Package List of Pin Names (1/3)

Pin No.		Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin(1)	Intelligent I/O Pin	Analog Pin	Bus Control Pin
FP	GP								
1	99		P9_6			TXD4/SDA4/SRXD4/CAN1OUT		ANEX1	
2	100		P9_5			CLK4/CAN1IN/CAN1WU		ANEX0	
3	1		P9_4		TB4IN	CTS4/RTS4/SS4		DA1	
4	2		P9_3		TB3IN	CTS3/RTS3/SS3		DA0	
5	3		P9_2		TB2IN	TXD3/SDA3/SRXD3	OUTC2_0/IEOUT/ISTXD2		
6	4		P9_1		TB1IN	RXD3/SCL3/STXD3	IEIN/ISRXD2		
7	5		P9_0		TB0IN	CLK3			
8	6	BYTE							
9	7	CNVSS							
10	8	XCIN	P8_7						
11	9	XCOUT	P8_6						
12	10	RESET							
13	11	XOUT							
14	12	VSS							
15	13	XIN							
16	14	VCC1							
17	15		P8_5	NMI					
18	16		P8_4	INT2					
19	17		P8_3	INT1		CAN0IN/CAN1IN			
20	18		P8_2	INT0		CAN0OUT/CAN1OUT			
21	19		P8_1		TA4IN/U/RTP2_3	CTS5/RTS5	INPC1_5/OUTC1_5		
22	20		P8_0		TA4OUT/U	RXD5	ISRXD0		
23	21		P7_7		TA3IN/RTP2_2	CLK5/CAN0IN	INPC1_4/OUTC1_4/ISCLK0		
24	22		P7_6		TA3OUT	TXD5/CAN0OUT	INPC1_3/OUTC1_3/ISTXD0		
25	23		P7_5		TA2IN/W/RTP2_1		INPC1_2/OUTC1_2 ISRXD1		
26	24		P7_4		TA2OUT/W/RTP2_0		INPC1_1/OUTC1_1/ISCLK1		
27	25		P7_3		TA1IN/V	CTS2/RTS2/SS2	INPC1_0/OUTC1_0/ISTXD1		
28	26		P7_2		TA1OUT/V	CLK2			
29	27		P7_1		TA0IN/TB5IN/RTP0_3	RXD2/SCL2/STXD2	INPC1_7/OUTC1_7/OUTC2_2/ISRXD2/IEIN		
30	28		P7_0		TA0OUT/RTP0_2	TXD2/SDA2/SRXD2	INPC1_6/OUTC1_6/OUTC2_0/ISTXD2/IEOUT		
31	29		P6_7			TXD1/SDA1/SRXD1			
32	30		P6_6			RXD1/SCL1/STXD1			
33	31		P6_5			CLK1			
34	32		P6_4			CTS1/RTS1/SS1	OUTC2_1/ISCLK2		
35	33		P6_3			TXD0/SDA0/SRXD0/IrDAOUT			
36	34		P6_2			RXD0/SCL0/STXD0/IrDAIN			
37	35		P6_1		RTP0_1	CLK0			
38	36		P6_0		RTP0_0	CTS0/RTS0/SS0			
39	37		P5_7						RDY
40	38		P5_6						ALE

NOTE:
1. The CAN pins cannot be used in M32C/87B. Only CAN0 pins can be used in M32C/87A.

Table 4.4 SFR Address Map (4/20)

Address	Register	Symbol	After Reset
0090h	UART0 Transmit/NACK Interrupt Control Register	S0TIC	XXXX X000b
0091h	UART1/UART4 Bus Conflict Detection Interrupt Control Register	BCN1IC/BCN4IC	XXXX X000b
0092h	UART1 Transmit/NACK Interrupt Control Register	S1TIC	XXXX X000b
0093h	Key Input Interrupt Control Register	KUPIC	XXXX X000b
0094h	Timer B0 Interrupt Control Register	TB0IC	XXXX X000b
0095h	II/O Interrupt Control Register 1 / CAN1 Interrupt Control Register 1	IIO1IC/CAN4IC	XXXX X000b
0096h	Timer B2 Interrupt Control Register	TB2IC	XXXX X000b
0097h	II/O Interrupt Control Register 3	IIO3IC	XXXX X000b
0098h	Timer B4 Interrupt Control Register	TB4IC	XXXX X000b
0099h	II/O Interrupt Control Register 5 /CAN1 Interrupt Control Register 2	IIO5IC/CAN5IC	XXXX X000b
009Ah	$\overline{\text{INT4}}$ Interrupt Control Register	INT4IC	XX00 X000b
009Bh	II/O Interrupt Control Register 7	IIO7IC	XXXX X000b
009Ch	$\overline{\text{INT2}}$ Interrupt Control Register	INT2IC	XX00 X000b
009Dh	II/O Interrupt Control Register 9 / CAN0 Interrupt Control Register 0	IIO9IC/CAN0IC	XXXX X000b
009Eh	$\overline{\text{INT0}}$ Interrupt Control Register	INT0IC	XX00 X000b
009Fh	Exit Priority Register	RLVL	XXXX 0000b
00A0h	Interrupt Request Register 0	IIO0IR	0000 000Xb
00A1h	Interrupt Request Register 1	IIO1IR	0000 000Xb
00A2h	Interrupt Request Register 2	IIO2IR	0000 000Xb
00A3h	Interrupt Request Register 3	IIO3IR	0000 000Xb
00A4h	Interrupt Request Register 4	IIO4IR	0000 000Xb
00A5h	Interrupt Request Register 5	IIO5IR	0000 000Xb
00A6h	Interrupt Request Register 6	IIO6IR	0000 000Xb
00A7h	Interrupt Request Register 7	IIO7IR	0000 000Xb
00A8h	Interrupt Request Register 8	IIO8IR	0000 000Xb
00A9h	Interrupt Request Register 9	IIO9IR	0000 000Xb
00AAh	Interrupt Request Register 10	IIO10IR	0000 000Xb
00ABh	Interrupt Request Register 11	IIO11IR	0000 000Xb
00ACh			
00ADh			
00AEh			
00AFh			
00B0h	Interrupt Enable Register 0	IIO0IE	00h
00B1h	Interrupt Enable Register 1	IIO1IE	00h
00B2h	Interrupt Enable Register 2	IIO2IE	00h
00B3h	Interrupt Enable Register 3	IIO3IE	00h
00B4h	Interrupt Enable Register 4	IIO4IE	00h
00B5h	Interrupt Enable Register 5	IIO5IE	00h
00B6h	Interrupt Enable Register 6	IIO6IE	00h
00B7h	Interrupt Enable Register 7	IIO7IE	00h
00B8h	Interrupt Enable Register 8	IIO8IE	00h
00B9h	Interrupt Enable Register 9	IIO9IE	00h
00BAh	Interrupt Enable Register 10	IIO10IE	00h
00BBh	Interrupt Enable Register 11	IIO11IE	00h
00BCh			
00BDh			
00BEh			
00BFh to 00DFh			

X: Undefined
Blank spaces are all reserved. No access is allowed.

Table 4.8 SFR Address Map (8/20)

Address	Register	Symbol	After Reset
01C0h	UART5 Transmit/Receive Mode Register	U5MR	00h
01C1h	UART5 Baud Rate Register	U5BRG	XXh
01C2h	UART5 Transmit Buffer Register	U5TB	XXXXh
01C3h			
01C4h	UART5 Transmit/Receive Control Register 0	U5C0	0000 1000b
01C5h	UART5 Transmit/Receive Control Register 1	U5C1	XXXX 0010b
01C6h	UART5 Receive Buffer Register	U5RB	XXXXh
01C7h			
01C8h	UART6 Transmit/Receive Mode Register	U6MR	00h
01C9h	UART6 Baud Rate Register	U6BRG	XXh
01CAh	UART6 Transmit Buffer Register	U6TB	XXXXh
01CBh			
01CCh	UART6 Transmit/Receive Control Register 0	U6C0	0000 1000b
01CDh	UART6 Transmit/Receive Control Register 1	U6C1	XXXX 0010b
01CEh	UART6 Receive Buffer Register	U6RB	XXXXh
01CFh			
01D0h	UART5, UART6 Transmit/Receive Control Register	U56CON	X000 0000b
01D1h	UART5, UART6 Input Pin Function Select Register	U56IS	X000 X000b
01D2h			
01D3h			
01D4h			
01D5h			
01D6h			
01D7h			
01D8h	RTP Output Buffer Register 0	RTP0R	XXh
01D9h	RTP Output Buffer Register 1	RTP1R	XXh
01DAh	RTP Output Buffer Register 2	RTP2R	XXh
01DBh	RTP Output Buffer Register 3	RTP3R	XXh
01DCh			
01DDh			
01DEh			
01DFh			
01E0h	CAN0 Message Slot Buffer 0 Standard ID0(1)(2)	C0SLOT0_0	XXh
01E1h	CAN0 Message Slot Buffer 0 Standard ID1(1)(2)	C0SLOT0_1	XXh
01E2h	CAN0 Message Slot Buffer 0 Extended ID0(1)(2)	C0SLOT0_2	XXh
01E3h	CAN0 Message Slot Buffer 0 Extended ID1(1)(2)	C0SLOT0_3	XXh
01E4h	CAN0 Message Slot Buffer 0 Extended ID2(1)(2)	C0SLOT0_4	XXh
01E5h	CAN0 Message Slot Buffer 0 Data Length Code(1)(2)	C0SLOT0_5	XXh
01E6h	CAN0 Message Slot Buffer 0 Data 0(1)(2)	C0SLOT0_6	XXh
01E7h	CAN0 Message Slot Buffer 0 Data 1(1)(2)	C0SLOT0_7	XXh
01E8h	CAN0 Message Slot Buffer 0 Data 2(1)(2)	C0SLOT0_8	XXh
01E9h	CAN0 Message Slot Buffer 0 Data 3(1)(2)	C0SLOT0_9	XXh
01EAh	CAN0 Message Slot Buffer 0 Data 4(1)(2)	C0SLOT0_10	XXh
01EBh	CAN0 Message Slot Buffer 0 Data 5(1)(2)	C0SLOT0_11	XXh
01ECh	CAN0 Message Slot Buffer 0 Data 6(1)(2)	C0SLOT0_12	XXh
01EDh	CAN0 Message Slot Buffer 0 Data 7(1)(2)	C0SLOT0_13	XXh
01EEh	CAN0 Message Slot Buffer 0 Time Stamp High-Order(1)(2)	C0SLOT0_14	XXh
01EFh	CAN0 Message Slot Buffer 0 Time Stamp Low-Order(1)(2)	C0SLOT0_15	XXh

X: Undefined
Blank spaces are all reserved. No access is allowed.
NOTES:
1. The CAN-associated registers (allocated in addresses 01E0h to 02BFh) cannot be used in M32C/87B. In M32C/87A, only CAN0-associated registers can be used.
2. Set the PM13 bit in the PM1 register to 1 (2 wait states for SFR area) before accessing the CAN-associated registers.

Table 4.11 SFR Address Map (11/20)

Address	Register(2)(3)	Symbol	After Reset
0250h	CAN1 Slot Buffer Select Register	C1SBS	00h(1)
0251h	CAN1 Control Register 1	C1CTLR1	X000 00XXb(1)
0252h	CAN1 Sleep Control Register	C1SLPR	XXXX XXX0b(1)
0253h			
0254h	CAN1 Acceptance Filter Support Register	C1AFS	0000 0000b(1)
0255h			0000 0001b(1)
0256h			
0257h			
0258h			
0259h			
025Ah			
025Bh			
025Ch			
025Dh			
025Eh			
025Fh			
0260h	CAN1 Message Slot Buffer 0 Standard ID0	C1SLOT0_0	XXh
0261h	CAN1 Message Slot Buffer 0 Standard ID1	C1SLOT0_1	XXh
0262h	CAN1 Message Slot Buffer 0 Extended ID0	C1SLOT0_2	XXh
0263h	CAN1 Message Slot Buffer 0 Extended ID1	C1SLOT0_3	XXh
0264h	CAN1 Message Slot Buffer 0 Extended ID2	C1SLOT0_4	XXh
0265h	CAN1 Message Slot Buffer 0 Data Length Code	C1SLOT0_5	XXh
0266h	CAN1 Message Slot Buffer 0 Data 0	C1SLOT0_6	XXh
0267h	CAN1 Message Slot Buffer 0 Data 1	C1SLOT0_7	XXh
0268h	CAN1 Message Slot Buffer 0 Data 2	C1SLOT0_8	XXh
0269h	CAN1 Message Slot Buffer 0 Data 3	C1SLOT0_9	XXh
026Ah	CAN1 Message Slot Buffer 0 Data 4	C1SLOT0_10	XXh
026Bh	CAN1 Message Slot Buffer 0 Data 5	C1SLOT0_11	XXh
026Ch	CAN1 Message Slot Buffer 0 Data 6	C1SLOT0_12	XXh
026Dh	CAN1 Message Slot Buffer 0 Data 7	C1SLOT0_13	XXh
026Eh	CAN1 Message Slot Buffer 0 Time Stamp High-Order	C1SLOT0_14	XXh
026Fh	CAN1 Message Slot Buffer 0 Time Stamp Low-Order	C1SLOT0_15	XXh
0270h	CAN1 Message Slot Buffer 1 Standard ID0	C1SLOT1_0	XXh
0271h	CAN1 Message Slot Buffer 1 Standard ID1	C1SLOT1_1	XXh
0272h	CAN1 Message Slot Buffer 1 Extended ID0	C1SLOT1_2	XXh
0273h	CAN1 Message Slot Buffer 1 Extended ID1	C1SLOT1_3	XXh
0274h	CAN1 Message Slot Buffer 1 Extended ID2	C1SLOT1_4	XXh
0275h	CAN1 Message Slot Buffer 1 Data Length Code	C1SLOT1_5	XXh
0276h	CAN1 Message Slot Buffer 1 Data 0	C1SLOT1_6	XXh
0277h	CAN1 Message Slot Buffer 1 Data 1	C1SLOT1_7	XXh
0278h	CAN1 Message Slot Buffer 1 Data 2	C1SLOT1_8	XXh
0279h	CAN1 Message Slot Buffer 1 Data 3	C1SLOT1_9	XXh
027Ah	CAN1 Message Slot Buffer 1 Data 4	C1SLOT1_10	XXh
027Bh	CAN1 Message Slot Buffer 1 Data 5	C1SLOT1_11	XXh
027Ch	CAN1 Message Slot Buffer 1 Data 6	C1SLOT1_12	XXh
027Dh	CAN1 Message Slot Buffer 1 Data 7	C1SLOT1_13	XXh
027Eh	CAN1 Message Slot Buffer 1 Time Stamp High-Order	C1SLOT1_14	XXh
027Fh	CAN1 Message Slot Buffer 1 Time Stamp Low-Order	C1SLOT1_15	XXh

X: Undefined
Blank spaces are all reserved. No access is allowed.
NOTES:
1. Values are obtained by setting the SLEEP bit in the C1SLPR register to “1” (sleep mode exited) after reset and supplying a clock to the CAN module.
2. The CAN-associated registers (allocated in addresses 01E0h to 02BFh) cannot be used in M32C/87B. In M32C/87A, only CAN0-associated registers can be used.
3. Set the PM13 bit in the PM1 register to 1 (2 wait states for SFR area) before accessing the CAN-associated registers.

Table 4.12 SFR Address Map (12/20)

Address	Register(3)(4)	Symbol	After Reset
0280h	CAN1 Control Register 0	C1CTLR0	XX01 0X01b(2)
0281h			XXXX 0000b(2)
0282h	CAN1 Status Register	C1STR	0000 0000b(2)
0283h			X000 0X01b(2)
0284h	CAN1 Extended ID Register	C1IDR	0000h(2)
0285h			
0286h	CAN1 Configuration Register	C1CONR	0000 XXXXb(2)
0287h			0000 0000b(2)
0288h	CAN1 Time Stamp Register	C1TSR	0000h(2)
0289h			
028Ah	CAN1 Transmit Error Count Register	C1TEC	00h(2)
028Bh	CAN1 Receive Error Count Register	C1REC	00h(2)
028Ch	CAN1 Slot Interrupt Status Register	C1SISTR	0000h(2)
028Dh			
028Eh			
028Fh			
0290h	CAN1 Slot Interrupt Mask Register	C1SIMKR	0000h(2)
0291h			
0292h			
0293h			
0294h	CAN1 Error Interrupt Mask Register	C1EIMKR	XXXX X000b(2)
0295h	CAN1 Error Interrupt Status Register	C1EISTR	XXXX X000b(2)
0296h	CAN1 Error Source Register	C1EFR	00h(2)
0297h	CAN1 Baud Rate Prescaler	C1BRP	0000 0001b(2)
0298h			
0299h	CAN1 Mode Register	C1MDR	XXXX XX00b(2)
029Ah			
029Bh			
029Ch			
029Dh			
029Eh			
029Fh			
02A0h	CAN1 Single Shot Control Register	C1SSCTLR	0000h(1)(2)
02A1h			
02A2h			
02A3h			
02A4h	CAN1 Single Shot Status Register	C1SSSTR	0000h(1)(2)
02A5h			
02A6h			
02A7h			
02A8h	CAN1 Global Mask Register Standard ID0	C1GMR0	XXX0 0000b(1)(2)
02A9h	CAN1 Global Mask Register Standard ID1	C1GMR1	XX00 0000b(1)(2)
02AAh	CAN1 Global Mask Register Extended ID0	C1GMR2	XXXX 0000b(1)(2)
02ABh	CAN1 Global Mask Register Extended ID1	C1GMR3	00h(1)(2)
02ACh	CAN1 Global Mask Register Extended ID2	C1GMR4	XX00 0000b(1)(2)
02ADh			
02AEh			
02AFh			

X: Undefined
Blank spaces are all reserved. No access is allowed.
NOTES:
1. The BANKSEL bit in the C0CTLR1 register can switch functions for addresses 02A0h to 02BFh.
2. Values are obtained by setting the SLEEP bit in the C1SLPR register to “1” (sleep mode exited) after reset and supplying a clock to the CAN module.
3. The CAN-associated registers (allocated in addresses 01E0h to 02BFh) cannot be used in M32C/87B. In M32C/87A, only CAN0-associated registers can be used.
4. Set the PM13 bit in the PM1 register to 1 (2 wait states for SFR area) before accessing the CAN-associated registers.

Table 4.18 SFR Address Map (18/20)

Address	Register	Symbol	After Reset
0380h 0381h	A/D0 Register 0	AD00	00XXh
0382h 0383h	A/D0 Register 1	AD01	00XXh
0384h 0385h	A/D0 Register 2	AD02	00XXh
0386h 0387h	A/D0 Register 3	AD03	00XXh
0388h 0389h	A/D0 Register 4	AD04	00XXh
038Ah 038Bh	A/D0 Register 5	AD05	00XXh
038Ch 038Dh	A/D0 Register 6	AD06	00XXh
038Eh 038Fh	A/D0 Register 7	AD07	00XXh
0390h			
0391h			
0392h	A/D0 Control Register 4	AD0CON4	XXXX 00XXb
0393h			
0394h	A/D0 Control Register 2	AD0CON2	XX0X X000b
0395h	A/D0 Control Register 3	AD0CON3	XXXX X000b
0396h	A/D0 Control Register 0	AD0CON0	00h
0397h	A/D0 Control Register 1	AD0CON1	00h
0398h	D/A Register 0	DA0	XXh
0399h			
039Ah	D/A Register 1	DA1	XXh
039Bh			
039Ch	D/A Control Register	DACON	XXXX XX00b
039Dh	D/A Control Register 1	DACON1	XXXX 0000b
039Eh			
039Fh			

X: Undefined
Blank spaces are all reserved. No access is allowed.

Table 4.19 SFR Address Map (19/20)

Address	Register	Symbol	After Reset
03A0h	Function Select Register A8(1)	PS8	X000 0000b
03A1h	Function Select Register A9(1)	PS9	00h
03A2h			
03A3h	Function Select Register B9(1)	PSL9	XXX0 XX00b
03A4h	Function Select Register E2	PSE2	XXXX XX0Xb
03A5h			
03A6h			
03A7h	Function Select Register D1	PSD1	00X0 XX00b
03A8h	Function Select Register D2	PSD2	XXXX XX0Xb
03A9h			
03AAh	Function Select Register C6(1)	PSC6	XXXX 0X00b
03ABh	Function Select Register E1	PSE1	00XX XX00b
03ACh	Function Select Register C2	PSC2	XXXX X00Xb
03ADh	Function Select Register C3	PSC3	X0XX XXXXb
03AEh			
03AFh	Function Select Register C	PSC	00h
03B0h	Function Select Register A0	PS0	00h
03B1h	Function Select Register A1	PS1	00h
03B2h	Function Select Register B0	PSL0	00h
03B3h	Function Select Register B1	PSL1	00h
03B4h	Function Select Register A2	PS2	00X0 0000b
03B5h	Function Select Register A3	PS3	00h
03B6h	Function Select Register B2	PSL2	00X0 0000b
03B7h	Function Select Register B3	PSL3	00h
03B8h	Function Select Register A4	PS4	00h
03B9h	Function Select Register A5(1)	PS5	XXX0 0000b
03BAh			
03BBh	Function Select Register B5(1)	PSL5	XXX0 0000b
03BCh	Function Select Register A6(1)	PS6	00h
03BDh	Function Select Register A7(1)	PS7	00h
03BEh	Function Select Register B6(1)	PSL6	00h
03BFh	Function Select Register B7(1)	PSL7	00h
03C0h	Port P6 Register	P6	XXh
03C1h	Port P7 Register	P7	XXh
03C2h	Port P6 Direction Register	PD6	00h
03C3h	Port P7 Direction Register	PD7	00h
03C4h	Port P8 Register	P8	XXh
03C5h	Port P9 Register	P9	XXh
03C6h	Port P8 Direction Register	PD8	00X0 0000b
03C7h	Port P9 Direction Register	PD9	00h
03C8h	Port P10 Register	P10	XXh
03C9h	Port P11 Register(1)	P11	XXh
03CAh	Port P10 Direction Register	PD10	00h
03CBh	Port P11 Direction Register(1)(2)	PD11	XXX0 0000b
03CCh	Port P12 Register(1)	P12	XXh
03CDh	Port P13 Register(1)	P13	XXh
03CEh	Port P12 Direction Register(1)(2)	PD12	00h
03CFh	Port P13 Direction Register(1)(2)	PD13	00h

X: Undefined
Blank spaces are all reserved. No access is allowed.
NOTES:
1. These registers cannot be used in the 100-pin package.
2. Set to FFh in the 100-pin package.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter		Condition	Value	Unit
VCC1, VCC2	Supply voltage		VCC1 = AVCC	-0.3 to 6.0	V
VCC2	Supply voltage		–	-0.3 to VCC1 + 0.1	V
AVCC	Analog supply voltage		VCC1 = AVCC	-0.3 to 6.0	V
VI	Input voltage	$\overline{\text{RESET}}$, CNVSS, BYTE, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P14_0 to P14_6, P15_0 to P15_7(1), VREF, XIN		-0.3 to VCC1 + 0.3	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7(1)		-0.3 to VCC2 + 0.3	
		P7_0, P7_1		-0.3 to 6.0	
VO	Output voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P14_0 to 14_6, P15_0 to P15_7(1), XOUT		-0.3 to VCC1 + 0.3	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7(1)		-0.3 to VCC2 + 0.3	
		P7_0, P7_1		-0.3 to 6.0	
Pd	Power consumption		-40°C≤Topr≤85°C	500	mW
Topr	Operating ambient temperature	during CPU operation		-20 to 85/ -40 to 85(2)	°C
		during programming or erasing Flash memory		0 to 60	°C
Tstg	Storage temperature			-65 to 150	°C

NOTES:
1. P11 to P15 are provided in the 144-pin package only.
2. Contact a Renesas sales office if temperature range of -40 to 85°C is required.

Table 5.3 Recommended Operating Conditions (2/3)
(VCC1 = VCC2 = 3.0 to 5.5 V, Topr = -20 to 85°C unless otherwise specified

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
IOH(peak)	Peak output high "H" current(2)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7(3)			-10.0	mA
IOH(avg)	Average output high "H" current(1)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7(3)			-5.0	mA
IOL(peak)	Peak output low "L" current(2)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7(3)			10.0	mA
IOL(avg)	Average output low "L" current(1)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7(3)			5.0	mA

NOTES:
1. Average output current is the average value within 100 ms.
2. A total IOL(peak) of P0, P1, P2, P8_6, P8_7, P9, P10, P11, P14, and P15 must be 80 mA or less.
   A total IOL(peak) of P3, P4, P5, P6, P7,P8_0 to P8_4, P12, and P13 must be 80 mA or less.
   A total IOH(peak) of P0, P1, P2, and P11 must be -40 mA or less.
   A total IOH(peak) of P8_6 to P8_7, P9, P10, P14, and P15 must be -40 mA or less.
   A total IOH(peak) of P3, P4, P5, P12, and P13 must be -40 mA or less.
   A total IOH(peak) of P6, P7, and P8_0 to P8_4 must be -40 mA or less.
3. P11 to P15 are provided in the 144-pin package only.

VCC1 = VCC2 = 5V

Table 5.8 A/D Conversion Characteristics
(VCC1 = VCC2 = AVCC = VREF = 4.2 to 5.5 V, VSS = AVSS = 0 V, Topr = -20 to 85°C, f(CPU) = 32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition		Standard			Unit
				Min.	Typ.	Max.	
–	Resolution	VREF = VCC1				10	Bits
INL	Integral nonlinearity error	VREF = VCC1 = VCC2 = 5 V	AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, AN15_0 to AN15_7, ANEX0, ANEX1			±3	LSB
			External op-amp connection mode			±7	LSB
DNL	Differential nonlinearity error					±1	LSB
–	Offset error					±3	LSB
–	Gain error					±3	LSB
RLADDER	Resistor ladder	VREF = VCC1		8		40	kΩ
tCONV	10-bit conversion time(1)(2)			2.06			µs
tCONV	8-bit conversion time(1)(2)			1.75			µs
tSAMP	Sampling time(1)			0.188			µs
VREF	Reference voltage			2		VCC1	V
VIA	Analog input voltage			0		VREF	V

NOTES:
1. The value is obtained when ϕAD frequency is at 16 MHz. Keep ϕAD frequency at 16 MHz or lower.
2. With using the sample and hold function

Table 5.9 D/A Conversion Characteristics
(VCC1 = VCC2 = VREF = 4.2 to 5.5 V, VSS = AVSS = 0 V, Topr = -20 to 85°C, f(CPU) = 32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
–	Resolution				8	Bits
–	Absolute accuracy				1.0	%
tsu	Setup time				3	µs
RO	Output resistance		4	10	20	kΩ
IVREF	Reference power supply input current	(note 1)			1.5	mA

NOTE:
1. Measured when one D/A converter is used, and the DAi register (i = 0, 1) of the unused D/A converter is set to 00h. The current flown into the resistor ladder in the A/D converter is excluded. IVREF flows even if the VCUT bit in the AD0CON1 register is set to 0 (VREF not connected)

VCC1 = VCC2 = 5V

Table 5.11 Voltage Detection Circuit Electrical Characteristics
(VCC1 = VCC2 = 3.0 to 5.5 V, VSS = 0 V, Topr = 25°C unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet4	Vdet4 detection voltage	VCC1 = 3.0 V to 5.5 V	3.3	3.8	4.4	V
Vdet3	Vdet3 detection voltage			3.0		V
Vdet3s	Hardware reset 2 hold voltage				2.0	V
Vdet3r	Hardware reset 2 release voltage			3.1		V

NOTES:
1. Vdet4 > Vdet3
2. Vdet3r > Vdet3 is not guaranteed.

Table 5.12 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
td(P-R)	Wait time to stabilize internal supply voltage when power-on	VCC1 = 3.0 to 5.5 V			2	ms
td(S-R)	Wait time to release hardware reset 2	VCC1 = Vdet3r to 5.5 V		6(1)	20	ms
td(E-A)	Start-up time for Vdet3 and Vdet4 detection circuit	VCC1 = 3.0 to 5.5 V			20	µs

NOTE:
1. When VCC1 = 5 V

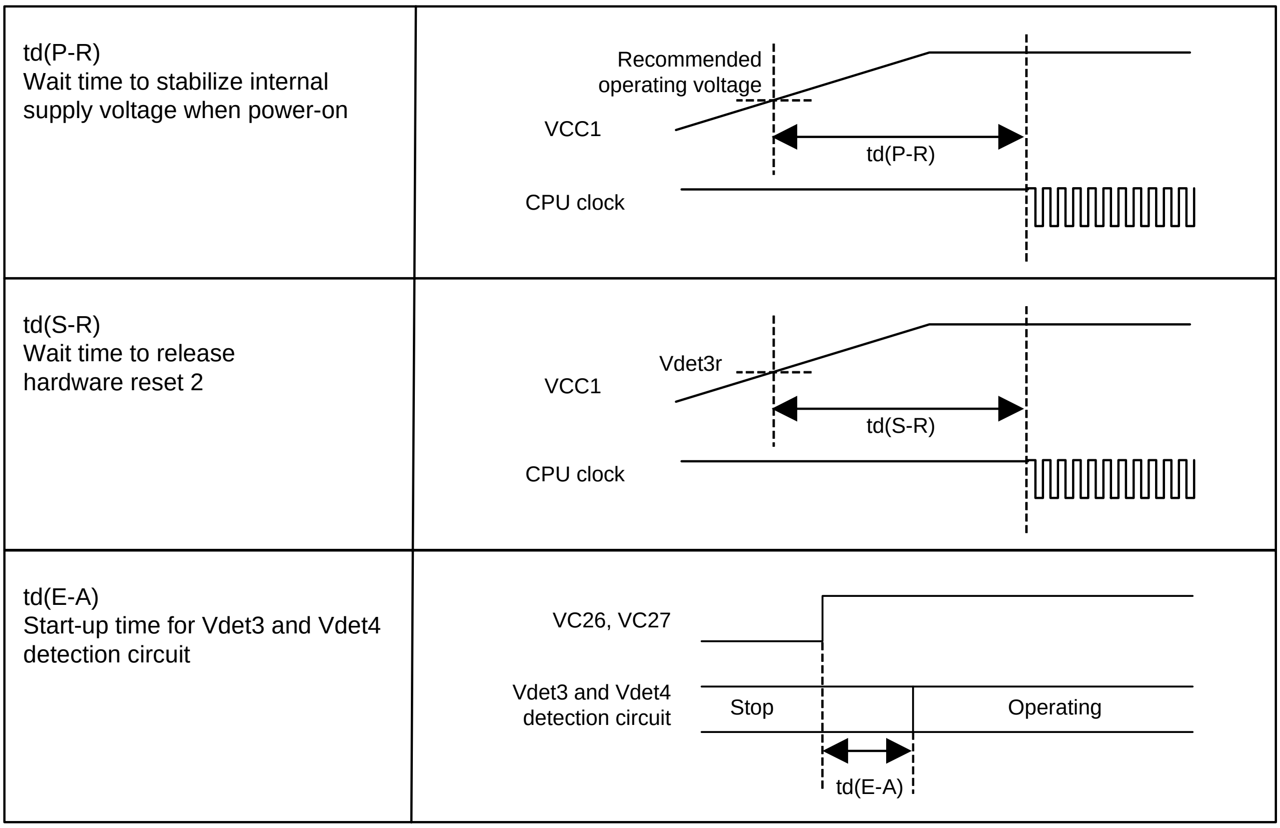

Figure 5.1 Power Supply Timing Diagram

VCC1 = VCC2 = 5V

Timing Requirements
(VCC1 = VCC2 = 4.2 to 5.5 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.28 Memory Expansion mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tac1(RD-DB)	Data input access time (RD standard)		(note 1)	ns
tac1(AD-DB)	Data input access time (AD standard, CS standard)		(note 1)	ns
tac2(RD-DB)	Data input access time (RD standard, when accessing a space with the multiplexed bus)		(note 1)	ns
tac2(AD-DB)	Data input access time (AD standard, when accessing a space with the multiplexed bus)		(note 1)	ns
tsu(DB-BCLK)	Data input setup time	26		ns
tsu(RDY-BCLK)	$\overline{\text{RDY}}$ input setup time	26		ns
tsu(HOLD-BCLK)	$\overline{\text{HOLD}}$ input setup time	30		ns
th(RD-DB)	Data input hold time	0		ns
th(BCLK-RDY)	$\overline{\text{RDY}}$ input hold time	0		ns
th(BCLK-HOLD)	$\overline{\text{HOLD}}$ input hold time	0		ns
td(BCLK-HLDA)	$\overline{\text{HLDA}}$ output delay time		25	ns

NOTE:
1. Values, which depend on BCLK frequency and external bus cycles, can be obtained from the following equations. Insert wait states or lower the operation frequency, f(BCLK), if the calculated value is negative.

$$tac1(RD\text{-}DB) = \frac{10^9 \times m}{f(BCLK) \times 2} - 35 \text{ [ns] (if external bus cycle is } a\phi + b\phi,\ m = (b \times 2) + 1)$$

$$tac1(AD\text{-}DB) = \frac{10^9 \times n}{f(BCLK)} - 35 \text{ [ns] (if external bus cycle is } a\phi + b\phi,\ n = a + b)$$

$$tac2(RD\text{-}DB) = \frac{10^9 \times m}{f(BCLK) \times 2} - 35 \text{ [ns] (if external bus cycle is } a\phi + b\phi,\ m = (b \times 2) - 1)$$

$$tac2(AD\text{-}DB) = \frac{10^9 \times p}{f(BCLK) \times 2} - 35 \text{ [ns] (if external bus cycle is } a\phi + b\phi,\ p = \{(a + b - 1) \times 2\} + 1)$$

VCC1 = VCC2 = 5V

Switching Characteristics
(VCC1 = VCC2 = 4.2 to 5.5 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.29 Memory Expansion Mode and Microprocessor Mode (when accessing external memory space)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min.	Max.	
td(BCLK-AD)	Address output delay time	See Figure 5.2		18	ns
th(BCLK-AD)	Address output hold time (BCLK standard)		-3		ns
th(RD-AD)	Address output hold time (RD standard)(3)		0		ns
th(WR-AD)	Address output hold time (WR standard)(3)		(note 1)		ns
td(BCLK-CS)	Chip-select signal output delay time			18	ns
th(BCLK-CS)	Chip-select signal output hold time (BCLK standard)		-3		ns
th(RD-CS)	Chip-select signal output hold time (RD standard)(3)		0		ns
th(WR-CS)	Chip-select signal output hold time (WR standard)(3)		(note 1)		ns
td(BCLK-RD)	RD signal output delay time			18	ns
th(BCLK-RD)	RD signal output hold time		-5		ns
td(BCLK-WR)	WR signal output delay time			18	ns
th(BCLK-WR)	WR signal output hold time		-5		ns
td(DB-WR)	Data output delay time (WR standard)		(note 2)		ns
th(WR-DB)	Data output hold time (WR standard)(3)		(note 1)		ns
tw(WR)	WR output width		(note 2)		ns

NOTES:

1. Values, which depend on BCLK frequency, can be obtained from the following equations.

$$th(WR\text{-}DB) = \frac{10^9}{f(BCLK) \times 2} - 15 \text{ [ns]}$$

$$th(WR\text{-}AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \text{ [ns]}$$

$$th(WR\text{-}CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \text{ [ns]}$$

2. Values, which depend on BCLK frequency and external bus cycles, can be obtained from the following equations.

$$td(DB\text{-}WR) = \frac{10^9 \times m}{f(BCLK)} - 20 \text{ [ns] (if external bus cycle is } a\phi + b\phi,\ m = b)$$

$$tw(WR) = \frac{10^9 \times n}{f(BCLK) \times 2} - 15 \text{ [ns] (if external bus cycle is } a\phi + b\phi,\ n = (b \times 2) - 1)$$

3. tc [ns] is added when recovery cycle is inserted.

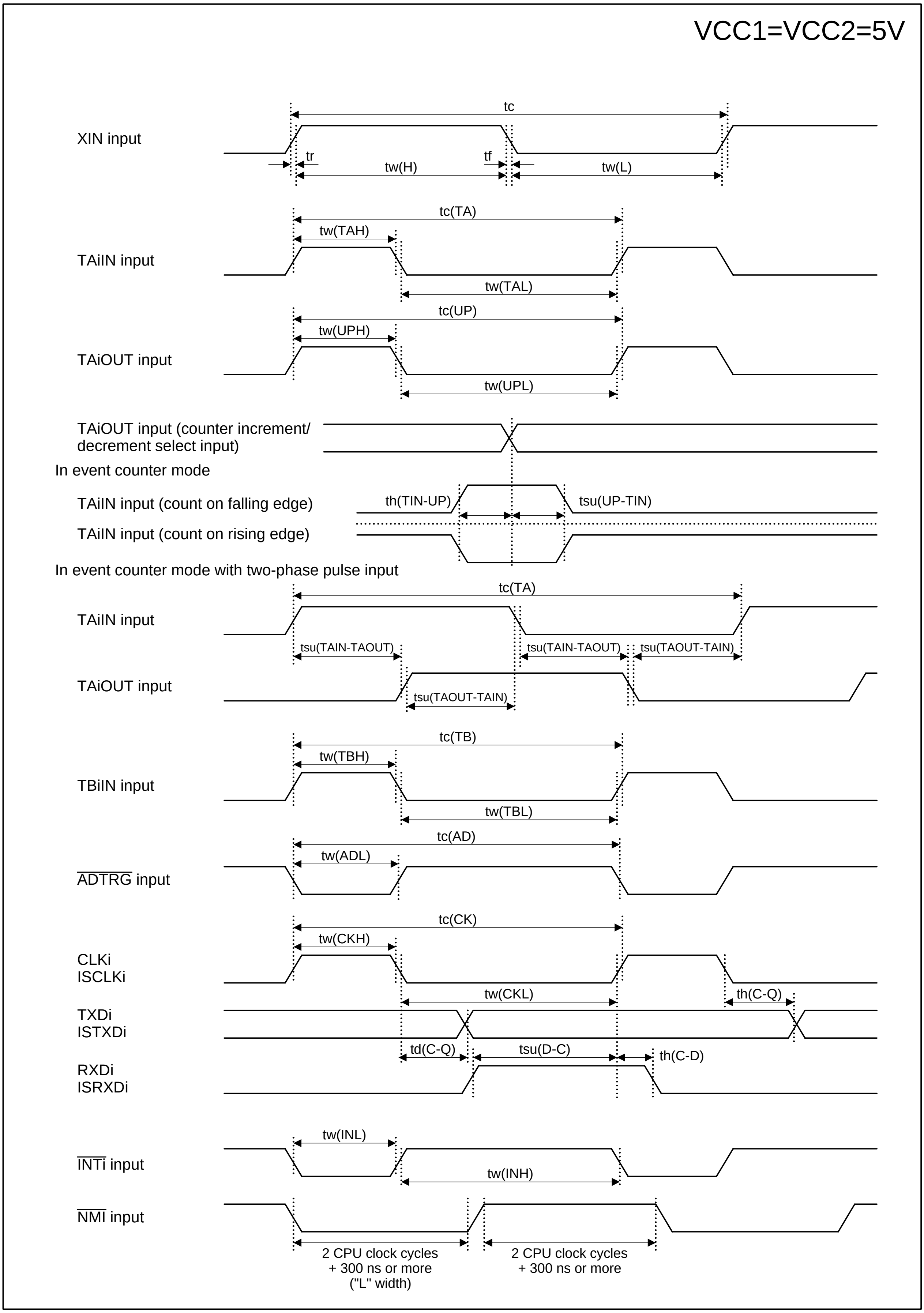

Figure 5.3 VCC1 = VCC2 = 5 V Timing Diagram (1/4)

VCC1 = VCC2 = 3.3 V

Table 5.33 Electrical Characteristics (3/3)
(VCC1 = VCC2 = 3.3 V, VSS = 0 V, Topr = 25°C)

Symbol	Parameter	Measurement Condition[1]		Standard			Unit
				Min.	Typ.	Max.	
ICC	Power supply current	Flash memory version	f(CPU) = 24 MHz		23	33	mA
			f(CPU) = 16 MHz		17		mA
			f(CPU) = 8 MHz		11		mA
			f(CPU) = f(Ring) In on-chip oscillator low-power consumption mode		2.6		mA
			f(CPU) = 32 kHz In low-power consumption mode While flash memory is operating		430		µA
			f(CPU) = 32 kHz In low-power consumption mode While flash memory is stopped[2]		30		µA
			Wait mode: f(CPU) = f(Ring) After entering wait mode from on-chip oscillator low-power consumption mode		45		µA
			Stop mode (while clock is stopped)		0.8	5	µA
			Stop mode (while clock is stopped) Topr = 85°C			50	µA
		Mask ROM version	f(CPU) = 24 MHz		23	33	mA
			f(CPU) = 16 MHz		17		mA
			f(CPU) = 8 MHz		11		mA
			f(CPU) = f(Ring) In on-chip oscillator low-power consumption mode		1		mA
			f(CPU) = 32 kHz In low-power consumption mode		30		µA
			Wait mode: f(CPU) = f(Ring) After entering wait mode from on-chip oscillator low-power consumption mode		45		µA
			Stop mode (while clock is stopped)		0.8	5	µA
			Stop mode (while clock is stopped) Topr = 85°C			50	µA

NOTES:
1. In single-chip mode, leave the output pins open and connect the input pins to VSS.
2. Value is obtained when setting the FMSTP bit in the FMR0 register to 1 (flash memory stopped) and running the program on RAM.

VCC1 = VCC2 = 3.3 V

Table 5.34 A/D Conversion Characteristics (VCC1 = VCC2 = AVCC = VREF = 3.0 to 3.6 V, VSS = AVSS = 0 V, Topr = -20 to 85°C, f(CPU) = 24MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
–	Resolution	VREF = VCC1			10	Bits
INL	Integral nonlinearity error (8-bit)	VREF = VCC1 = VCC2 = 3.3 V			±2	LSB
DNL	Differential nonlinearity error (8-bit)				±1	LSB
–	Offset error (8-bit)				±2	LSB
–	Gain error (8-bit)				±2	LSB
RLADDER	Resistor ladder	VREF = VCC1	8		40	kΩ
tCONV	8-bit conversion time(1)(2)		4.9			μs
VREF	Reference voltage		3		VCC1	V
VIA	Analog input voltage		0		VREF	V

NOTES:
1. The value when ϕAD frequency is at 10 MHz. Keep ϕAD frequency at 10 MHz or lower.
   If f(CPU) (=fAD) is 24 MHz, divide f(CPU) by 3 to make it 8 MHz. The conversion time in this case is 6.1 μs.
2. Sample and hold function is not available.

Table 5.35 D/A Conversion Characteristics (VCC1 = VCC2 = VREF = 3.0 to 3.6 V, VSS = AVSS = 0 V, Topr = -20 to 85°C, f(CPU) = 24MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
–	Resolution				8	Bits
–	Absolute accuracy				1.0	%
tsu	Setup time				3	μs
RO	Output resistance		4	10	20	kΩ
IVREF	Reference power supply input current	(note 1)			1.0	mA

NOTE:
1. Measurement when one D/A converter is used, and the DAi register (i = 0, 1) of the unused D/A converter is set to 00h. The current flown into the resistor ladder in the A/D converter is excluded. IVREF flows even if VCUT bit in the AD0CON1 register is set to 0 (VREF not connected)

VCC1 = VCC2 = 3.3 V

Timing Requirements
(VCC1 = VCC2 = 3.0 to 3.6 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.36 External Clock Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc	External clock input cycle time	41		ns
tw(H)	External clock input high (“H”) pulse width	18		ns
tw(L)	External clock input low (“L”) pulse width	18		ns
tr	External clock rise time		5	ns
tf	External clock fall time		5	ns

Table 5.37 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	100		ns
tw(TAH)	TAiIN input high (“H”) pulse width	40		ns
tw(TAL)	TAiIN input low (“L”) pulse width	40		ns

i = 0 to 4

Table 5.38 Timer A Input (Gate Signal Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	400		ns
tw(TAH)	TAiIN input high (“H”) pulse width	200		ns
tw(TAL)	TAiIN input low (“L”) pulse width	200		ns

i = 0 to 4

Table 5.39 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	200		ns
tw(TAH)	TAiIN input high (“H”) pulse width	100		ns
tw(TAL)	TAiIN input low (“L”) pulse width	100		ns

i = 0 to 4

Table 5.40 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tw(TAH)	TAiIN input high (“H”) pulse width	100		ns
tw(TAL)	TAiIN input low (“L”) pulse width	100		ns

i = 0 to 4

VCC1 = VCC2 = 3.3 V

Timing Requirements
(VCC1 = VCC2 = 3.0 to 3.6 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.41 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(UP)	TAiOUT input cycle time	2000		ns
tw(UPH)	TAiOUT input high (“H”) pulse width	1000		ns
tw(UPL)	TAiOUT input low (“L”) pulse width	1000		ns
tsu(UP-TIN)	TAiOUT input setup time	400		ns
th(TIN-UP)	TAiOUT input hold time	400		ns

i = 0 to 4

Table 5.42 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	2		μs
tsu(TAIN-TAOUT)	TAiOUT input setup time	500		ns
tsu(TAOUT-TAIN)	TAiIN input setup time	500		ns

i = 0 to 4

Table 5.43 Timer B Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TB)	TBiIN input cycle time (counted on one edge)	100		ns
tw(TBH)	TBiIN input high (“H”) pulse width (counted on one edge)	40		ns
tw(TBL)	TBiIN input low (“L”) pulse width (counted on one edge)	40		ns
tc(TB)	TBiIN input cycle time (counted on both edges)	200		ns
tw(TBH)	TBiIN input high (“H”) pulse width (counted on both edges)	80		ns
tw(TBL)	TBiIN input low (“L”) pulse width (counted on both edges)	80		ns

i = 0 to 5

Table 5.44 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TB)	TBiIN input cycle time	400		ns
tw(TBH)	TBiIN input high (“H”) pulse width	200		ns
tw(TBL)	TBiIN input low (“L”) pulse width	200		ns

i = 0 to 5

Table 5.45 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TB)	TBiIN input cycle time	400		ns
tw(TBH)	TBiIN input high (“H”) pulse width	200		ns
tw(TBL)	TBiIN input low (“L”) pulse width	200		ns

i = 0 to 5

VCC1 = VCC2 = 3.3 V

Timing Requirements
(VCC1 = VCC2 = 3.0 to 3.6 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.51 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tac1(RD-DB)	Data input access time (RD standard)		(note 1)	ns
tac1(AD-DB)	Data input access time (AD standard, CS standard)		(note 1)	ns
tac2(RD-DB)	Data input access time (RD standard, when accessing a space with the multiplexed bus)		(note 1)	ns
tac2(AD-DB)	Data input access time (AD standard, when accessing a space with the multiplexed bus)		(note 1)	ns
tsu(DB-BCLK)	Data input setup time	30		ns
tsu(RDY-BCLK)	$\overline{\text{RDY}}$ input setup time	40		ns
tsu(HOLD-BCLK)	$\overline{\text{HOLD}}$ input setup time	60		ns
th(RD-DB)	Data input hold time	0		ns
th(BCLK-RDY)	$\overline{\text{RDY}}$ input hold time	0		ns
th(BCLK-HOLD)	$\overline{\text{HOLD}}$ input hold time	0		ns
td(BCLK-HLDA)	$\overline{\text{HLDA}}$ output delay time		25	ns

NOTE:

1. Values, which depend on BCLK frequency and external bus cycles, can be obtained from the following equations. Insert wait states or lower the operation frequency, f(BCLK), if the calculated value is negative.

$$tac1(RD\text{-}DB) = \frac{10^9 \times m}{f(BCLK) \times 2} - 35 \text{ [ns] (if external bus cycle is } a\phi + b\phi,\ m = (b \times 2) + 1)$$

$$tac1(AD\text{-}DB) = \frac{10^9 \times n}{f(BCLK)} - 35 \text{ [ns] (if external bus cycle is } a\phi + b\phi,\ n = a + b)$$

$$tac2(RD\text{-}DB) = \frac{10^9 \times m}{f(BCLK) \times 2} - 35 \text{ [ns] (if external bus cycle is } a\phi + b\phi,\ m = (b \times 2) - 1)$$

$$tac2(AD\text{-}DB) = \frac{10^9 \times p}{f(BCLK) \times 2} - 35 \text{ [ns] (if external bus cycle is } a\phi + b\phi,\ p = \{(a + b - 1) \times 2\} + 1)$$