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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	M32C/80
Core Size	16/32-Bit
Speed	32MHz
Connectivity	CANbus, EBI/EMI, I ² C, IEBus, IrDA, SIO, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	85
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30879flafp-u3

Table 1.4 Specifications (100-Pin Package) (2/2)

Item	Function	Specification
Serial Interface	UART0 to UART4	Clock synchronous/asynchronous × 5 I ² C bus, special mode 2, GCI mode, SIM mode, IrDA mode ⁽²⁾ , IEBus (optional) ⁽¹⁾⁽³⁾
	UART5	Clock synchronous/asynchronous × 1
A/D Converter		10-bit resolution × 26 channels (in single-chip mode) 10-bit resolution × 10 channels (in memory expansion mode and microprocessor mode) Including sample and hold function
D/A Converter		8-bit resolution × 2 channels
CRC Calculation Circuit		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) compliant
X/Y Converter		16 bits × 16 bits
Intelligent I/O		16-bit timer × 2 • Time measurement function (input capture): 8 channels • Waveform generation function (output compare): 10 channels • Communication function: Clock synchronous mode, clock asynchronous mode, HDLC data processing mode, IEBus (optional) ⁽¹⁾⁽³⁾ • 2-phase pulse signal processing (2-phase encoder input) × 1
ROM Correction Function		Address match interrupt × 8
CAN modules		Supporting CAN 2.0B specification M32C/87: 16 slots × 2 channels, M32C/87A: 16 slots × 1 channel M32C/87B: none
I/O Ports	Programmable I/O ports	• Input only: 1 • CMOS I/O: 85, selectable pull-up resistor • N channel open drain ports: 2
Flash Memory		• Erase and program voltage: 3.3 V ± 0.3 V or 5.0 V ± 0.5 V • Erase and program endurance: 100 times (all areas) • Program security: ROM code protect and ID code check • Debug functions: On-chip debug and on-board flash reprogram
Operating Frequency/Supply Voltage		32 MHz: VCC1 = 4.2 to 5.5 V, VCC2 = 3.0 V to VCC1 24 MHz: VCC1 = 3.0 to 5.5 V, VCC2 = 3.0 V to VCC1
Current Consumption		32 mA (32 MHz, VCC1 = VCC2 = 5 V) 23 mA (24 MHz, VCC1 = VCC2 = 3.3 V) 45 μA (approx. 1 MHz, VCC1 = VCC2 = 3.3 V, on-chip oscillator low-power consumption mode → wait mode) 0.8 μA (VCC1 = VCC2 = 3.3 V, stop mode)
Operating Ambient Temperature (°C)		-20 to 85°C, -40 to 85°C (optional) ⁽³⁾
Package		100-pin LQFP (PLQP0100KB-A) 100-pin QFP (PRQP0100JB-A)

NOTES:

1. IEBus is a registered trademark of NEC Electronics Corporation.
2. Available in UART0.
3. Please contact a Renesas sales office for optional features.

1.3 Block Diagram

Figure 1.2 shows a block diagram of the M32C/87 Group (M32C/87, M32C/87A, M32C/87B).

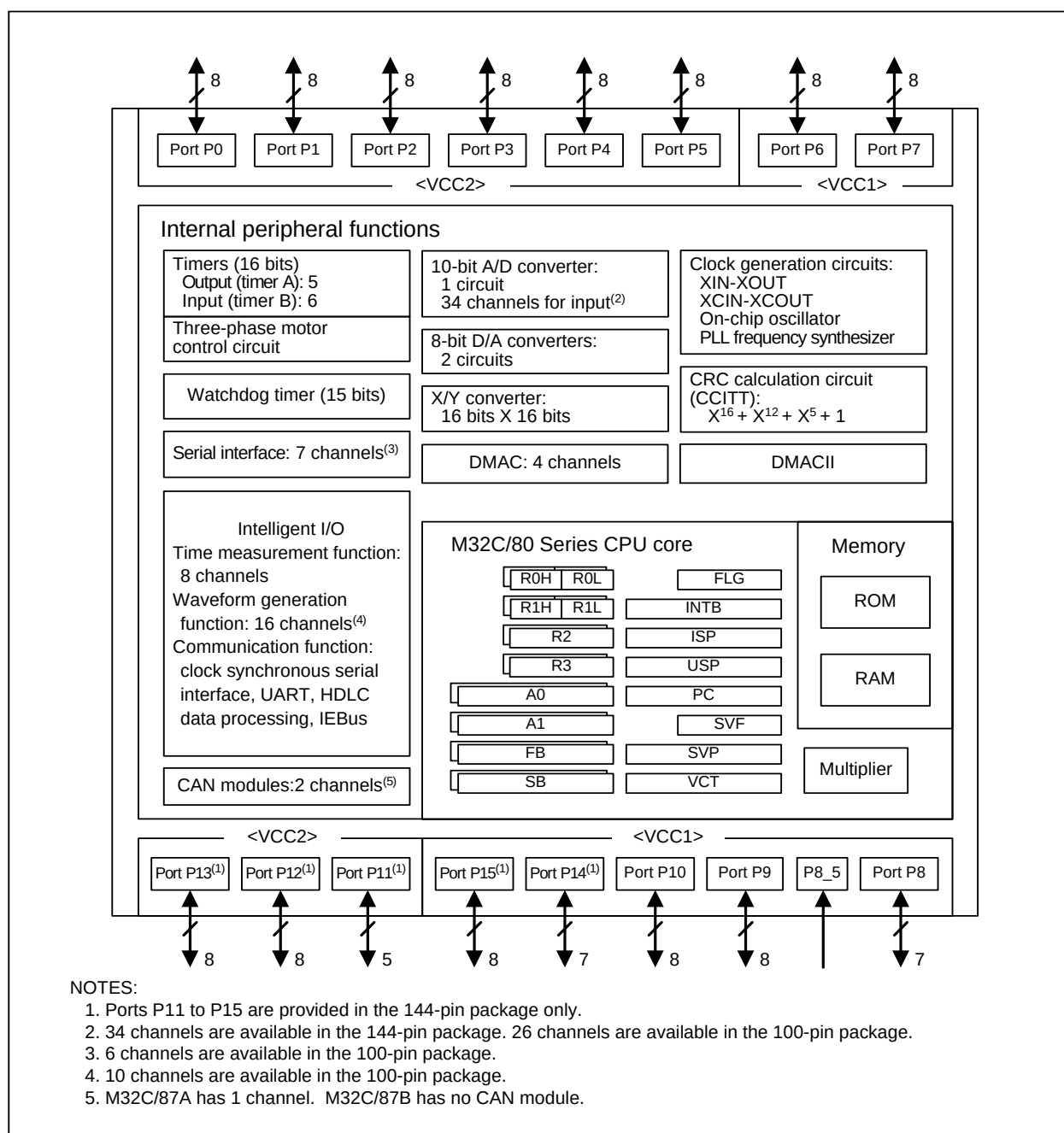


Figure 1.2 M32C/87 Group (M32C/87, M32C/87A, M32C/87B) Block Diagram

Table 1.10 144-Pin Package List of Pin Names (3/4)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
81		P3_5						A13,[A13/D13]
82		P3_4						A12,[A12/D12]
83		P3_3						A11,[A11/D11]
84		P3_2						A10,[A10/D10]
85		P3_1						A9,[A9/D9]
86		P12_4						
87		P12_3			CTS6/RTS6			
88		P12_2			RXD6			
89		P12_1			CLK6			
90		P12_0			TXD6			
91	VCC2							
92		P3_0						A8,[A8/D8]
93	VSS							
94		P2_7					AN2_7	A7,[A7/D7]
95		P2_6					AN2_6	A6,[A6/D6]
96		P2_5					AN2_5	A5,[A5/D5]
97		P2_4					AN2_4	A4,[A4/D4]
98		P2_3					AN2_3	A3,[A3/D3]
99		P2_2					AN2_2	A2,[A2/D2]
100		P2_1					AN2_1	A1,[A1/D1]
101		P2_0					AN2_0	A0,[A0/D0]
102		P1_7	INT5					D15
103		P1_6	INT4					D14
104		P1_5	INT3					D13
105		P1_4						D12
106		P1_3						D11
107		P1_2						D10
108		P1_1						D9
109		P1_0						D8
110		P0_7					AN0_7	D7
111		P0_6					AN0_6	D6
112		P0_5					AN0_5	D5
113		P0_4					AN0_4	D4
114		P11_4						
115		P11_3				INPC1_3/OUTC1_3		
116		P11_2				INPC1_2/OUTC1_2/ ISRXD1		
117		P11_1				INPC1_1/OUTC1_1/ ISCLK1		
118		P11_0				INPC1_0/OUTC1_0/ ISTXD1		
119		P0_3					AN0_3	D3
120		P0_2					AN0_2	D2

Table 1.18 Pin Functions (100-Pin and 144-Pin Package) (4/4)

Type	Symbol	I/O Type	Supply Voltage	Description
I/O port	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7	I/O	VCC2	8-bit CMOS I/O ports. The Port Pi Direction Register (i = 0 to 15) determines if each pin is used as an input port or an output port. The Pull-Up Control Registers determine if the input ports, divided into groups of four, are pulled up or not.
	P6_0 to P6_7, P7_0 to P7_7, P9_0 to P9_7, P10_0 to P10_7	I/O	VCC1	These 8-bit I/O ports are functionally equivalent to P0. (P7_0 and P7_1 are N-channel open drain output.)
	P8_0 to P8_4 P8_6, P8_7	I/O	VCC1	These I/O ports are functionally equivalent to P0.
Input port	P8_5	I	VCC1	Shares the pin with $\overline{\text{NMI}}$. Input port to read $\overline{\text{NMI}}$ pin level.
Key input interrupt input	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	VCC1	Key input interrupt input pins.

I: Input O: Output I/O: Input and output

Table 1.19 Pin Functions (144-Pin Package Only)

Type	Symbol	I/O Type	Supply Voltage	Description
$\overline{\text{INT}}$ Interrupt Input	$\overline{\text{INT6}}$ to $\overline{\text{INT8}}$	I	VCC1	$\overline{\text{INT}}$ interrupt input pins.
Serial interface	$\overline{\text{CTS6}}$	I	VCC1/ VCC2	Input pin to control data transmission.
	$\overline{\text{RTS6}}$	O	VCC1/ VCC2	Output pin to control data reception.
	CLK6	I/O	VCC1/ VCC2	Serial clock input/output pin.
	RXD6	I	VCC1/ VCC2	Serial data input pin.
	TXD6	O	VCC1/ VCC2	Serial data output pin.
Intelligent I/O	OUTC2_3 to OUTC2_7	O	VCC2	Output pins for the waveform generation function.
A/D converter	AN15_0 to AN15_7	I	VCC1	Analog input pins for the A/D converter.
I/O port	P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7	I/O	VCC2	These I/O ports are functionally equivalent to P0.
	P14_0 to P14_6, P15_0 to P15_7	I/O	VCC1	These I/O ports are functionally equivalent to P0.

I: Input O: Output I/O: Input and output

Table 4.11 SFR Address Map (11/20)

Address	Register ⁽²⁾⁽³⁾	Symbol	After Reset
0250h	CAN1 Slot Buffer Select Register	C1SBS	00h ⁽¹⁾
0251h	CAN1 Control Register 1	C1CTLR1	X000 00XXb ⁽¹⁾
0252h	CAN1 Sleep Control Register	C1SLPR	XXXX XXX0b ⁽¹⁾
0253h			
0254h	CAN1 Acceptance Filter Support Register	C1AFS	0000 0000b ⁽¹⁾
0255h			0000 0001b ⁽¹⁾
0256h			
0257h			
0258h			
0259h			
025Ah			
025Bh			
025Ch			
025Dh			
025Eh			
025Fh			
0260h	CAN1 Message Slot Buffer 0 Standard ID0	C1SLOT0_0	XXh
0261h	CAN1 Message Slot Buffer 0 Standard ID1	C1SLOT0_1	XXh
0262h	CAN1 Message Slot Buffer 0 Extended ID0	C1SLOT0_2	XXh
0263h	CAN1 Message Slot Buffer 0 Extended ID1	C1SLOT0_3	XXh
0264h	CAN1 Message Slot Buffer 0 Extended ID2	C1SLOT0_4	XXh
0265h	CAN1 Message Slot Buffer 0 Data Length Code	C1SLOT0_5	XXh
0266h	CAN1 Message Slot Buffer 0 Data 0	C1SLOT0_6	XXh
0267h	CAN1 Message Slot Buffer 0 Data 1	C1SLOT0_7	XXh
0268h	CAN1 Message Slot Buffer 0 Data 2	C1SLOT0_8	XXh
0269h	CAN1 Message Slot Buffer 0 Data 3	C1SLOT0_9	XXh
026Ah	CAN1 Message Slot Buffer 0 Data 4	C1SLOT0_10	XXh
026Bh	CAN1 Message Slot Buffer 0 Data 5	C1SLOT0_11	XXh
026Ch	CAN1 Message Slot Buffer 0 Data 6	C1SLOT0_12	XXh
026Dh	CAN1 Message Slot Buffer 0 Data 7	C1SLOT0_13	XXh
026Eh	CAN1 Message Slot Buffer 0 Time Stamp High-Order	C1SLOT0_14	XXh
026Fh	CAN1 Message Slot Buffer 0 Time Stamp Low-Order	C1SLOT0_15	XXh
0270h	CAN1 Message Slot Buffer 1 Standard ID0	C1SLOT1_0	XXh
0271h	CAN1 Message Slot Buffer 1 Standard ID1	C1SLOT1_1	XXh
0272h	CAN1 Message Slot Buffer 1 Extended ID0	C1SLOT1_2	XXh
0273h	CAN1 Message Slot Buffer 1 Extended ID1	C1SLOT1_3	XXh
0274h	CAN1 Message Slot Buffer 1 Extended ID2	C1SLOT1_4	XXh
0275h	CAN1 Message Slot Buffer 1 Data Length Code	C1SLOT1_5	XXh
0276h	CAN1 Message Slot Buffer 1 Data 0	C1SLOT1_6	XXh
0277h	CAN1 Message Slot Buffer 1 Data 1	C1SLOT1_7	XXh
0278h	CAN1 Message Slot Buffer 1 Data 2	C1SLOT1_8	XXh
0279h	CAN1 Message Slot Buffer 1 Data 3	C1SLOT1_9	XXh
027Ah	CAN1 Message Slot Buffer 1 Data 4	C1SLOT1_10	XXh
027Bh	CAN1 Message Slot Buffer 1 Data 5	C1SLOT1_11	XXh
027Ch	CAN1 Message Slot Buffer 1 Data 6	C1SLOT1_12	XXh
027Dh	CAN1 Message Slot Buffer 1 Data 7	C1SLOT1_13	XXh
027Eh	CAN1 Message Slot Buffer 1 Time Stamp High-Order	C1SLOT1_14	XXh
027Fh	CAN1 Message Slot Buffer 1 Time Stamp Low-Order	C1SLOT1_15	XXh

X: Undefined

Blank spaces are all reserved. No access is allowed.

NOTES:

1. Values are obtained by setting the SLEEP bit in the C1SLPR register to "1" (sleep mode exited) after reset and supplying a clock to the CAN module.
2. The CAN-associated registers (allocated in addresses 01E0h to 02BFh) cannot be used in M32C/87B. In M32C/87A, only CAN0-associated registers can be used.
3. Set the PM13 bit in the PM1 register to 1 (2 wait states for SFR area) before accessing the CAN-associated registers.

Table 4.18 SFR Address Map (18/20)

Address	Register	Symbol	After Reset
0380h	A/D0 Register 0	AD00	00XXh
0381h			
0382h	A/D0 Register 1	AD01	00XXh
0383h			
0384h	A/D0 Register 2	AD02	00XXh
0385h			
0386h	A/D0 Register 3	AD03	00XXh
0387h			
0388h	A/D0 Register 4	AD04	00XXh
0389h			
038Ah	A/D0 Register 5	AD05	00XXh
038Bh			
038Ch	A/D0 Register 6	AD06	00XXh
038Dh			
038Eh	A/D0 Register 7	AD07	00XXh
038Fh			
0390h			
0391h			
0392h	A/D0 Control Register 4	AD0CON4	XXXX 00XXb
0393h			
0394h	A/D0 Control Register 2	AD0CON2	XX0X X000b
0395h	A/D0 Control Register 3	AD0CON3	XXXX X000b
0396h	A/D0 Control Register 0	AD0CON0	00h
0397h	A/D0 Control Register 1	AD0CON1	00h
0398h	D/A Register 0	DA0	XXh
0399h			
039Ah	D/A Register 1	DA1	XXh
039Bh			
039Ch	D/A Control Register	DACON	XXXX XX00b
039Dh	D/A Control Register 1	DACON1	XXXX 0000b
039Eh			
039Fh			

X: Undefined

Blank spaces are all reserved. No access is allowed.

Table 4.19 SFR Address Map (19/20)

Address	Register	Symbol	After Reset
03A0h	Function Select Register A8 ⁽¹⁾	PS8	X000 0000b
03A1h	Function Select Register A9 ⁽¹⁾	PS9	00h
03A2h			
03A3h	Function Select Register B9 ⁽¹⁾	PSL9	XXX0 XX00b
03A4h	Function Select Register E2	PSE2	XXXX XX0Xb
03A5h			
03A6h			
03A7h	Function Select Register D1	PSD1	00X0 XX00b
03A8h	Function Select Register D2	PSD2	XXXX XX0Xb
03A9h			
03AAh	Function Select Register C6 ⁽¹⁾	PSC6	XXXX 0X00b
03ABh	Function Select Register E1	PSE1	00XX XX00b
03ACh	Function Select Register C2	PSC2	XXXX X00Xb
03ADh	Function Select Register C3	PSC3	X0XX XXXXb
03AEh			
03AFh	Function Select Register C	PSC	00h
03B0h	Function Select Register A0	PS0	00h
03B1h	Function Select Register A1	PS1	00h
03B2h	Function Select Register B0	PSL0	00h
03B3h	Function Select Register B1	PSL1	00h
03B4h	Function Select Register A2	PS2	00X0 0000b
03B5h	Function Select Register A3	PS3	00h
03B6h	Function Select Register B2	PSL2	00X0 0000b
03B7h	Function Select Register B3	PSL3	00h
03B8h	Function Select Register A4	PS4	00h
03B9h	Function Select Register A5 ⁽¹⁾	PS5	XXX0 0000b
03BAh			
03BBh	Function Select Register B5 ⁽¹⁾	PSL5	XXX0 0000b
03BCh	Function Select Register A6 ⁽¹⁾	PS6	00h
03BDh	Function Select Register A7 ⁽¹⁾	PS7	00h
03BEh	Function Select Register B6 ⁽¹⁾	PSL6	00h
03BFh	Function Select Register B7 ⁽¹⁾	PSL7	00h
03C0h	Port P6 Register	P6	XXh
03C1h	Port P7 Register	P7	XXh
03C2h	Port P6 Direction Register	PD6	00h
03C3h	Port P7 Direction Register	PD7	00h
03C4h	Port P8 Register	P8	XXh
03C5h	Port P9 Register	P9	XXh
03C6h	Port P8 Direction Register	PD8	00X0 0000b
03C7h	Port P9 Direction Register	PD9	00h
03C8h	Port P10 Register	P10	XXh
03C9h	Port P11 Register ⁽¹⁾	P11	XXh
03CAh	Port P10 Direction Register	PD10	00h
03CBh	Port P11 Direction Register ⁽¹⁾⁽²⁾	PD11	XXX0 0000b
03CCh	Port P12 Register ⁽¹⁾	P12	XXh
03CDh	Port P13 Register ⁽¹⁾	P13	XXh
03CEh	Port P12 Direction Register ⁽¹⁾⁽²⁾	PD12	00h
03CFh	Port P13 Direction Register ⁽¹⁾⁽²⁾	PD13	00h

X: Undefined

Blank spaces are all reserved. No access is allowed.

NOTES:

1. These registers cannot be used in the 100-pin package.
2. Set to FFh in the 100-pin package.

$$VCC1 = VCC2 = 5V$$

Table 5.6 Electrical Characteristics (2/3)

(VCC1 = VCC2 = 4.2 to 5.5 V, VSS = 0 V, Topr = -20 to 85°C, f(CPU) = 32 MHz unless otherwise specified)

Symbol	Parameter		Measurement Condition	Standard			Unit
				Min.	Typ.	Max.	
IIH	Input high "H" current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7 ⁽¹⁾ , XIN, RESET, CNVSS, BYTE	VI = 5 V			5.0	μA
IIL	Input low "L" current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7 ⁽¹⁾ , XIN, RESET, CNVSS, BYTE	VI = 0V			-5.0	μA
RPULLUP	Pull-up resistance	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7 ⁽¹⁾	VI = 0V	30	50	167	kΩ
RfXIN	Feedback resistance	XIN			1.5		MΩ
RfXCIN	Feedback resistance	XCIN			10		MΩ
VRAM	RAM data retention voltage	In stop mode		2.0			V

NOTE:

1. P11 to P15 are provided in the 144-pin package only.

$$VCC1 = VCC2 = 5V$$

Table 5.7 Electrical Characteristics (3/3)
(VCC1 = VCC2 = 5.5 V, VSS = 0 V, Topr = 25°C)

Symbol	Parameter	Measurement Condition ⁽¹⁾	Standard			Unit
			Min.	Typ.	Max.	
ICC	Power supply current	Flash memory version	f(CPU) = 32 MHz	32	45	mA
			f(CPU) = 16 MHz	19		mA
			f(CPU) = 8 MHz	12		mA
			f(CPU) = f(Ring) In on-chip oscillator low-power consumption mode	2.6		mA
			f(CPU) = 32 kHz In low-power consumption mode While flash memory is operating	430		μA
			f(CPU) = 32 kHz In low-power consumption mode While flash memory is stopped ⁽²⁾	30		μA
			Wait mode: f(CPU) = f(Ring) After entering wait mode from on-chip oscillator low-power consumption mode	50		μA
			Stop mode (while clock is stopped)	0.8	5	μA
			Stop mode (while clock is stopped) Topr = 85°C		50	μA
		Mask ROM version	f(CPU) = 32 MHz	32	45	mA
			f(CPU) = 16 MHz	19		mA
			f(CPU) = 8 MHz	12		mA
			f(CPU) = f(Ring) In on-chip oscillator low-power consumption mode	1		mA
			f(CPU) = 32 kHz In low-power consumption mode	30		μA
			Wait mode: f(CPU) = f(Ring) After entering wait mode from on-chip oscillator low-power consumption mode	50		μA
			Stop mode (while clock is stopped)	0.8	5	μA
			Stop mode (while clock is stopped) Topr = 85°C		50	μA

NOTES:

1. In single-chip mode, leave the output pins open and connect the input pins to VSS.
2. Value is obtained when setting the FMSTP bit in the FMR0 register to 1 (flash memory stopped) and running the program on RAM.

$$VCC1 = VCC2 = 5V$$

Timing Requirements

(VCC1 = VCC2 = 4.2 to 5.5 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.28 Memory Expansion mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tac1(RD-DB)	Data input access time (RD standard)		(note 1)	ns
tac1(AD-DB)	Data input access time (AD standard, CS standard)		(note 1)	ns
tac2(RD-DB)	Data input access time (RD standard, when accessing a space with the multiplexed bus)		(note 1)	ns
tac2(AD-DB)	Data input access time (AD standard, when accessing a space with the multiplexed bus)		(note 1)	ns
tsu(DB-BCLK)	Data input setup time	26		ns
tsu(RDY-BCLK)	$\overline{RDY}$ input setup time	26		ns
tsu(HOLD-BCLK)	$\overline{HOLD}$ input setup time	30		ns
th(RD-DB)	Data input hold time	0		ns
th(BCLK-RDY)	$\overline{RDY}$ input hold time	0		ns
th(BCLK-HOLD)	$\overline{HOLD}$ input hold time	0		ns
td(BCLK-HLDA)	HLDA output delay time		25	ns

NOTE:

1. Values, which depend on BCLK frequency and external bus cycles, can be obtained from the following equations. Insert wait states or lower the operation frequency, f(BCLK), if the calculated value is negative.

$$tac1(RD-DB) = \frac{10^9 \times m}{f(BCLK) \times 2} - 35 \text{ [ns]} \text{ (if external bus cycle is } a\phi + b\phi, m = (b \times 2) + 1)$$

$$tac1(AD-DB) = \frac{10^9 \times n}{f(BCLK)} - 35 \text{ [ns]} \text{ (if external bus cycle is } a\phi + b\phi, n = a + b)$$

$$tac2(RD-DB) = \frac{10^9 \times m}{f(BCLK) \times 2} - 35 \text{ [ns]} \text{ (if external bus cycle is } a\phi + b\phi, m = (b \times 2) - 1)$$

$$tac2(AD-DB) = \frac{10^9 \times p}{f(BCLK) \times 2} - 35 \text{ [ns]} \text{ (if external bus cycle is } a\phi + b\phi, p = \{(a + b - 1) \times 2\} + 1)$$

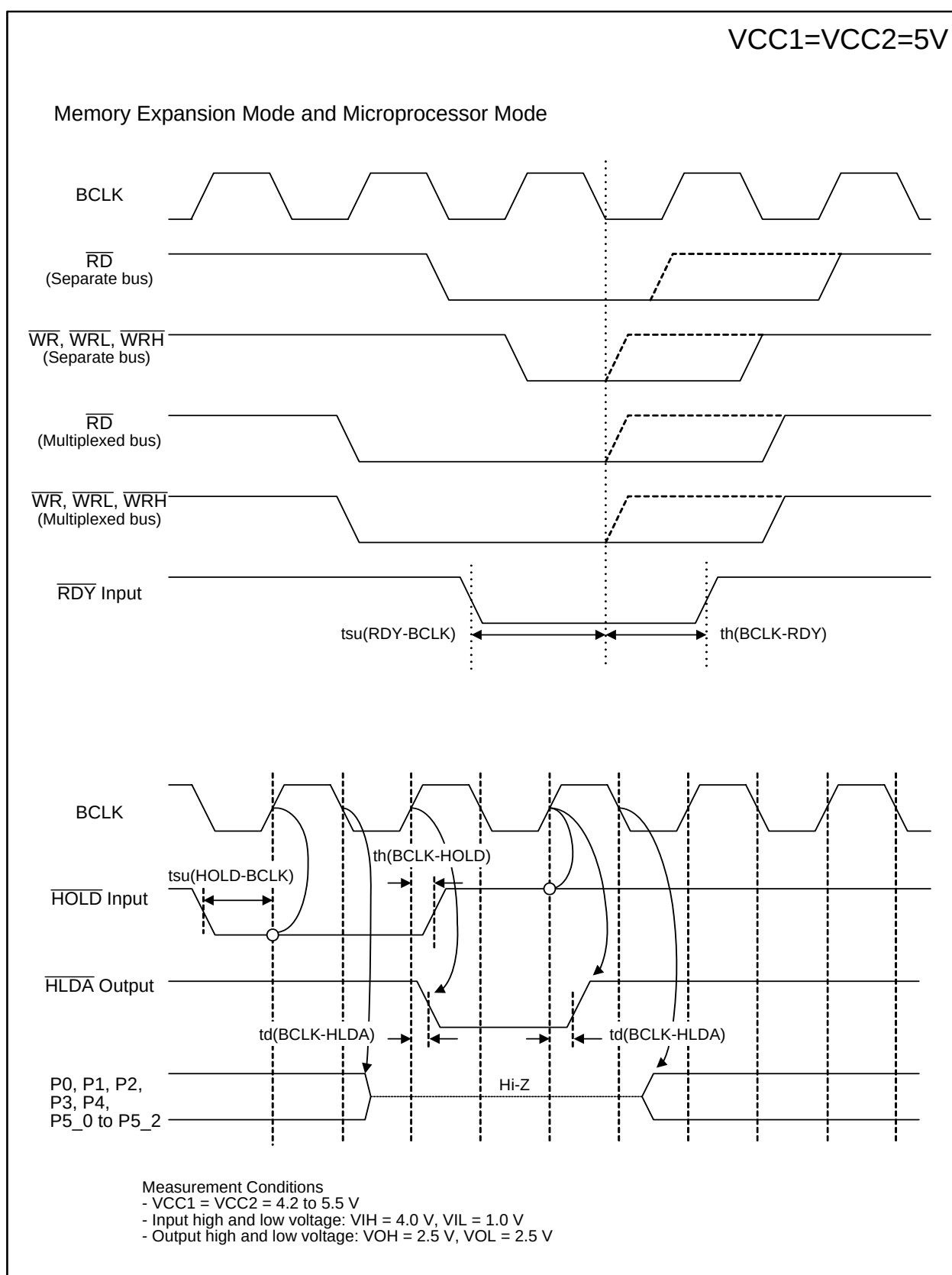
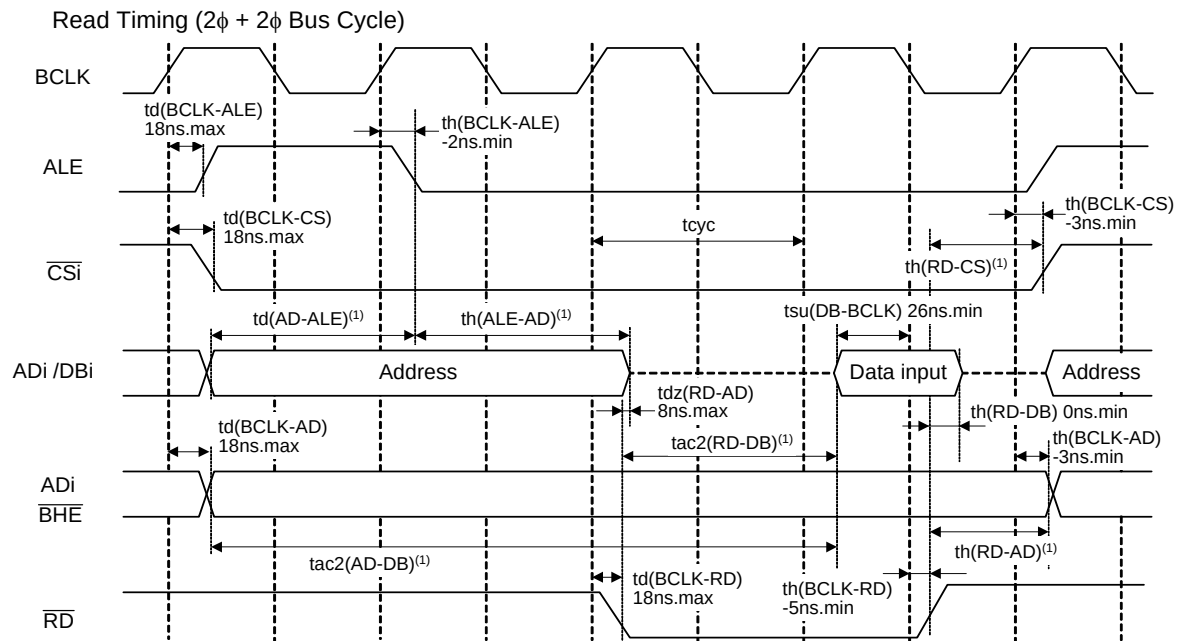


Figure 5.4 VCC1 = VCC2 = 5 V Timing Diagram (2/4)

Memory Expansion Mode and Microprocessor Mode (when accessing an external memory space with the multiplexed bus)

VCC1=VCC2=5V



NOTES:

1. Varies with operation frequency:

$$td(AD-ALE) = (tcyc / 2 \times n - 20) \text{ ns.min (if external bus cycle } a\phi + b\phi, n = a)$$

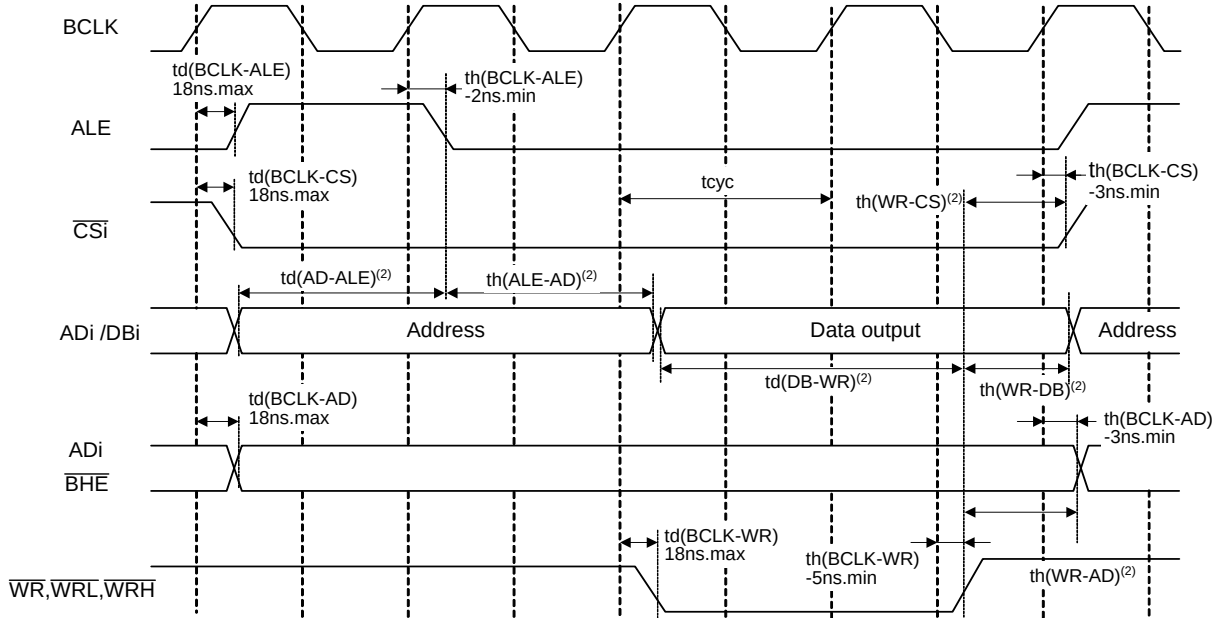
$$th(ALE-AD) = (tcyc / 2 \times n - 20) \text{ ns.min (if external bus cycle } a\phi + b\phi, n = a)$$

$$th(RD-AD) = (tcyc / 2 - 10) \text{ ns.min, } th(RD-CS) = (tcyc / 2 - 10) \text{ ns.min}$$

$$tac2(RD-DB) = (tcyc / 2 \times m - 35) \text{ ns.max (if external bus cycle } a\phi + b\phi, m = (b \times 2) - 1)$$

$$tac2(AD-DB) = (tcyc / 2 \times p - 35) \text{ ns.max (if external bus cycle } a\phi + b\phi, p = \{(a + b - 1) \times 2\} + 1)$$

Write Timing ($2\phi + 2\phi$ Bus Cycle)



NOTES:

1. Varies with operation frequency:

$$td(AD-ALE) = (tcyc / 2 \times n - 20) \text{ ns.min (if external bus cycle } a\phi + b\phi, n = a)$$

$$th(ALE-AD) = (tcyc / 2 \times n - 20) \text{ ns.min (if external bus cycle } a\phi + b\phi, n = a)$$

$$th(WR-AD) = (tcyc / 2 - 10) \text{ ns.min, } th(WR-CS) = (tcyc / 2 - 10) \text{ ns.min}$$

$$th(WR-DB) = (tcyc / 2 - 15) \text{ ns.min}$$

$$td(DB-WR) = (tcyc / 2 \times m - 25) \text{ ns.min (if external bus cycle } a\phi + b\phi, m = (b \times 2) - 1)$$

$$tcyc = \frac{10^9}{f(BCLK)}$$

Measurement Conditions:

- VCC1 = VCC2 = 4.2 to 5.5 V

- Input high and low voltage $V_{IH} = 2.5 \text{ V}$, $V_{IL} = 0.8 \text{ V}$ - Output high and low voltage $V_{OH} = 2.0 \text{ V}$, $V_{OL} = 0.8 \text{ V}$

Figure 5.6 VCC1 = VCC2 = 5 V Timing Diagram (4/4)

$$VCC1 = VCC2 = 3.3 \text{ V}$$

Table 5.31 Electrical Characteristics (1/3)

(VCC1 = VCC2 = 3.0 to 3.6 V, VSS = 0 V, Topr = -20 to 85°C, f(CPU) = 24 MHz unless otherwise specified)

Symbol	Parameter		Measurement Condition	Standard			Unit
				Min.	Typ.	Max.	
VOH	Output high "H" voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7 ⁽¹⁾	IOH = -1 mA	VCC2 - 0.6		VCC2	V
		P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P14_0 to P14_6, P15_0 to P15_7 ⁽¹⁾		VCC1 - 0.6		VCC1	
		XOUT	IOH = -0.1 mA	2.7		VCC1	V
		XCOUT	Drive capability = high		2.5		V
			Drive capability = low		1.6		V
VOL	Output low "L" voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7 ⁽¹⁾	IOL = 1 mA			0.5	V
		XOUT	IOL = 0.1 mA			0.5	V
		XCOUT	Drive capability = high		0		V
			Drive capability = low		0		V
VT+ - VT-	Hysteresis	HOLD, RDY, TA0IN to TA4IN, TB0IN to TB5IN, INT0 to INT8, ADTRG, CTS0 to CTS6, CLK0 to CLK6, TA0OUT to TA4OUT, NMI, KI0 to KI3, RXD0 to RXD6, SCL0 to SCL4, SDA0 to SDA4, INPC1_0 to INPC1_7, ISCLK0 to ISCLK2, ISRXD0 to ISRXD2, IEIN, CAN0IN, CAN1IN, CAN1WU		0.2		1.0	V
		RESET		0.2		1.8	V

NOTE:

1. P11 to P15 are provided in the 144-pin package only.

$$VCC1 = VCC2 = 3.3\text{ V}$$

Timing Requirements

(VCC1 = VCC2 = 3.0 to 3.6 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.46 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(AD)	ADTRG input cycle time (required for trigger)	1000		ns
tw(ADL)	ADTRG input low ("L") pulse width	125		ns

Table 5.47 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CK)	CLKi input cycle time	200		ns
tw(CKH)	CLKi input high ("H") pulse width	100		ns
tw(CKL)	CLKi input low ("L") pulse width	100		ns
td(C-Q)	TXDi output delay time		80	ns
th(C-Q)	TXDi output hold time	0		ns
tsu(D-C)	RXDi input setup time	70		ns
th(C-D)	RXDi input hold time	90		ns

i = 0 to 6

Table 5.48 Intelligent I/O Communication Function (Groups 0 and 1)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CK)	ISCLKi input cycle time	600		ns
tw(CKH)	ISCLKi input high ("H") pulse width	300		ns
tw(CKL)	ISCLKi input low ("L") pulse width	300		ns
td(C-Q)	ISTXDi output delay time		100	ns
th(C-Q)	ISTXDi output hold time	0		ns
tsu(D-C)	ISRXDi input setup time	100		ns
th(C-D)	ISRXDi input hold time	100		ns

i = 0, 1

Table 5.49 Intelligent I/O Communication Function (Group 2)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CK)	ISCLK2 input cycle time	600		ns
tw(CKH)	ISCLK2 input high ("H") pulse width	300		ns
tw(CKL)	ISCLK2 input low ("L") pulse width	300		ns
td(C-Q)	ISTXD2 output delay time		180	ns
th(C-Q)	ISTXD2 output hold time	0		ns
tsu(D-C)	ISRXD2 input setup time	150		ns
th(C-D)	ISRXD2 input hold time	100		ns

$$VCC1 = VCC2 = 3.3 \text{ V}$$

Switching Characteristics

(VCC1 = VCC2 = 3.0 to 3.6 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.52 Memory Expansion Mode and Microprocessor Mode (when accessing external memory space)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min.	Max.	
td(BCLK-AD)	Address output delay time	See Figure 5.2		18	ns
th(BCLK-AD)	Address output hold time (BCLK standard)		-3		ns
th(RD-AD)	Address output hold time (RD standard) ⁽³⁾		0		ns
th(WR-AD)	Address output hold time (WR standard) ⁽³⁾		(note 1)		ns
td(BCLK-CS)	Chip-select signal output delay time			18	ns
th(BCLK-CS)	Chip-select signal output hold time (BCLK standard)		-3		ns
th(RD-CS)	Chip-select signal output hold time (RD standard) ⁽³⁾		0		ns
th(WR-CS)	Chip-select signal output hold time (WR standard) ⁽³⁾		(note 1)		ns
td(BCLK-RD)	RD signal output delay time			18	ns
th(BCLK-RD)	RD signal output hold time		-5		ns
td(BCLK-WR)	WR signal output delay time			18	ns
th(BCLK-WR)	WR signal output hold time		0		ns
td(DB-WR)	Data output delay time (WR standard)		(note 2)		ns
th(WR-DB)	Data output hold time (WR standard) ⁽³⁾		(note 1)		ns
tw(WR)	WR output width		(note 2)		ns

NOTES:

- Values, which depend on BCLK frequency, can be obtained from the following equations.

$$th(WR-DB) = \frac{10^9}{f(BCLK) \times 2} - 20 \text{ [ns]}$$

$$th(WR-AD) = \frac{10^9}{f(BCLK) \times 2} - 15 \text{ [ns]}$$

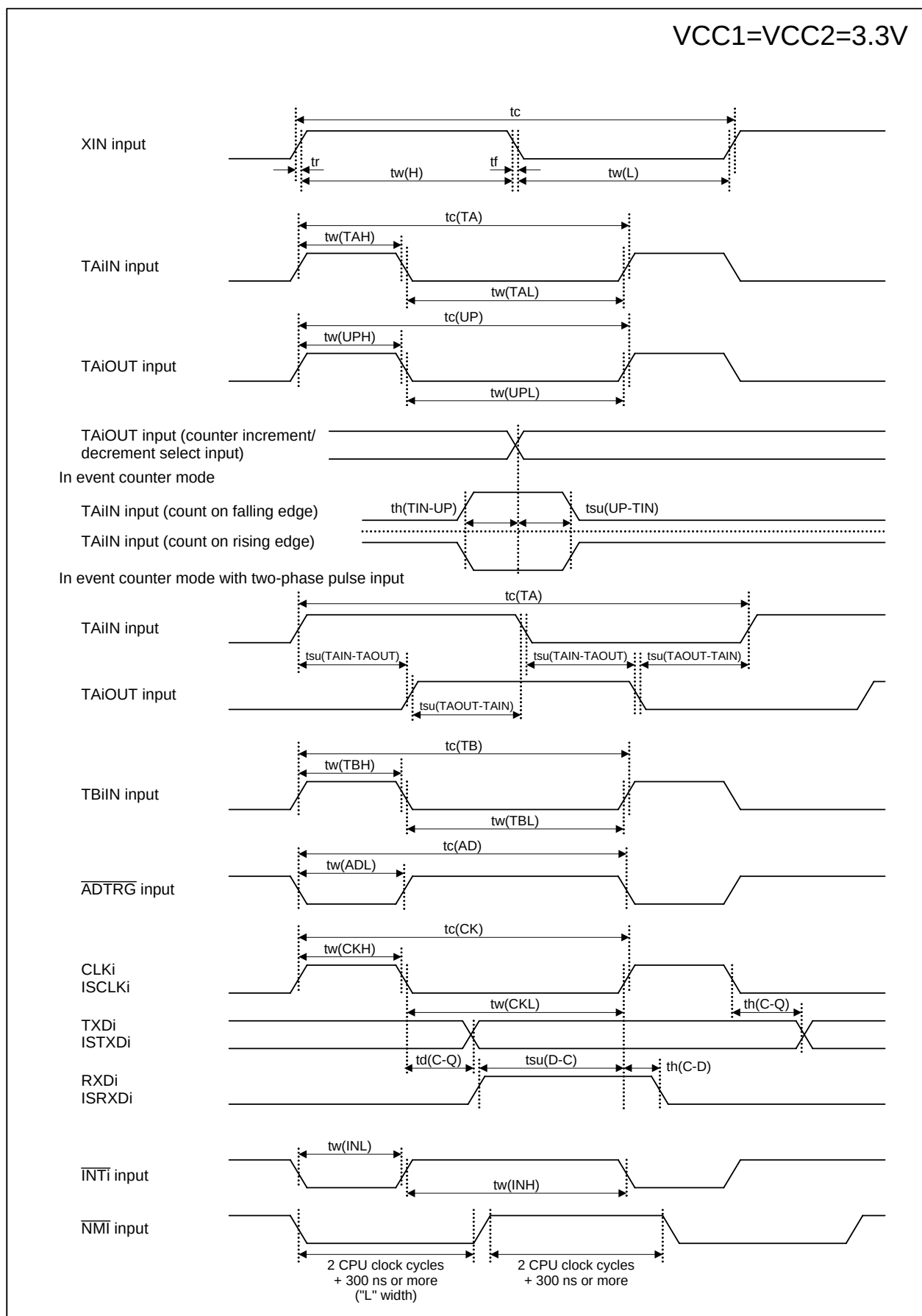
$$th(WR-CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \text{ [ns]}$$

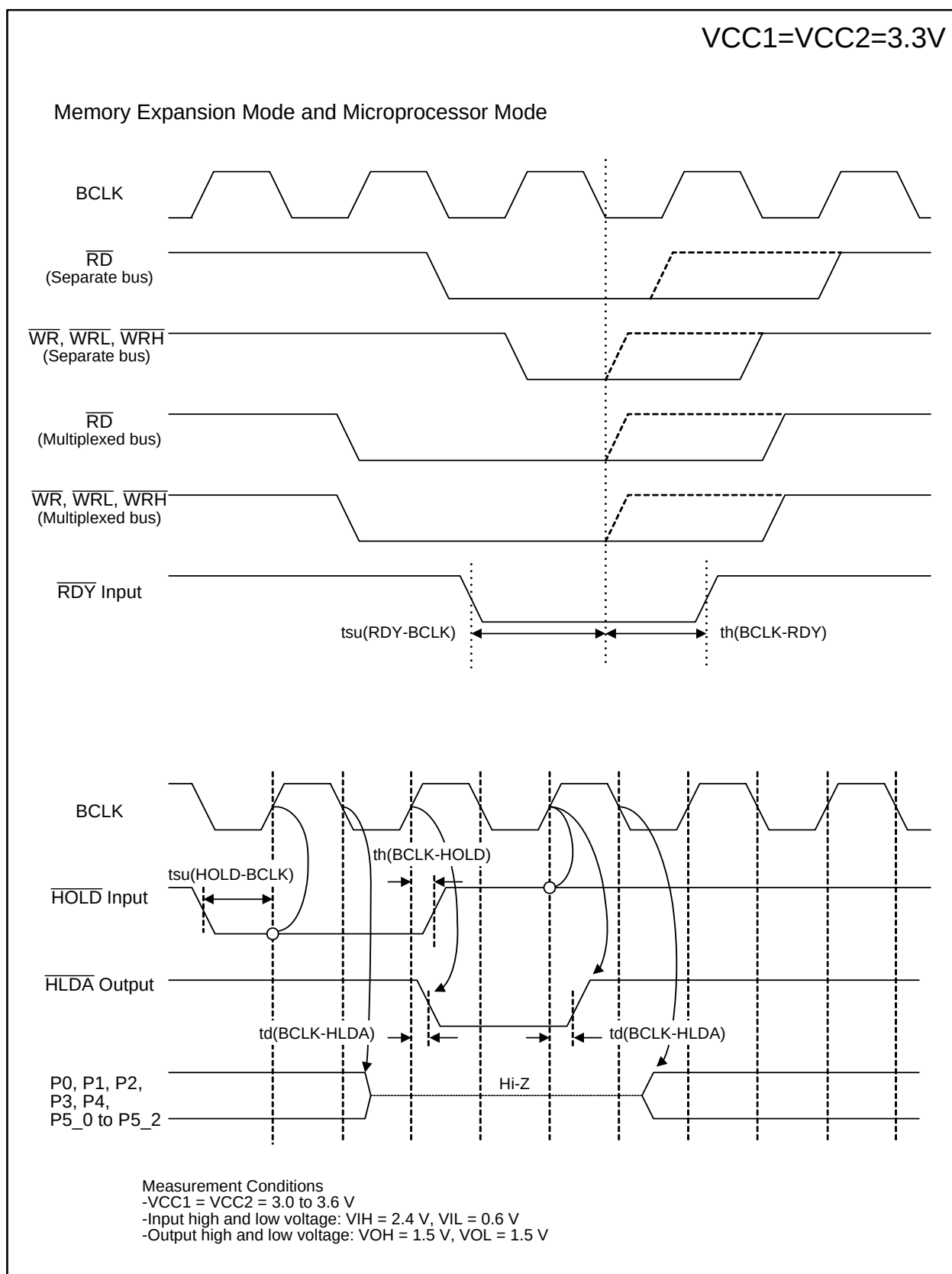
- Values, which depend on BCLK frequency and external bus cycles, can be obtained from the following equations.

$$td(DB-WR) = \frac{10^9 \times m}{f(BCLK)} - 20 \text{ [ns]} \text{ (if external bus cycle is } a\phi + b\phi, m = b)$$

$$tw(WR) = \frac{10^9 \times n}{f(BCLK) \times 2} - 15 \text{ [ns]} \text{ (if external bus cycle is } a\phi + b\phi, n = (b \times 2) - 1)$$

- tc [ns] is added when recovery cycle is inserted.

**Figure 5.7** VCC1 = VCC2 = 3.3 V Timing Diagram (1/4)

**Figure 5.8** VCC1 = VCC2 = 3.3 V Timing Diagram (2/4)

REVISION HISTORY		M32C/87 Group Datasheet	
Rev.	Date	Description	
		Page	Summary
			Electrical Characteristics • Table 5.22 Memory Expansion Mode and Microprocessor Mode $t_h(WR-DB)$ expression on note 1 modified • Table 5.23 Memory Expansion Mode and Microprocessor Mode $t_h(WR-DB)$ expression on note 1 modified; $t_h(ALE-AD)$ expression on note 4 modified • Figure 5.3 Vcc1=Vcc2=5V Timing Diagram (1) $t_{ac1}(RD-DB)$ expression on note 2 modified; $t_h(WR-DB)$ and $t_w(ER)$ expressions on note 3 modified; t_{cyc} expression added • Figure 5.4 Vcc1=Vcc2=5V Timing Diagram (2) $t_{ac2}(RD-DB)$ and $t_{ac2}(AD-DB)$ expressions on note 1 modified; $t_h(ALE-AD)$ expressions on notes 1 and 2 modified; $t_d(DB-WR)$ expression on note 2 modified; t_{cyc} expression added • Figure 5.5 Vcc1=Vcc2=5V Timing Diagram (3) $\overline{NMI}$ input diagram added • Table 5.24 Electrical Characteristics V_{OH} values changed; R_{PULLUP} and I_{CC} values modified • Table 5.25 A/D Conversion Characteristics t_{CONV} value modified • Table 5.28 Memory Expansion Mode and Microprocessor Mode $t_{ac1}(RD-DB)$ expression on note 1 modified; $t_{ac2}(RD-DB)$ expression on note 1 added • Table 5.40 Memory Expansion Mode and Microprocessor Mode $t_h(BCLK-AD)$, $t_h(BCLK-CS)$ and $t_h(BCLK-RD)$ values modified; $t_h(WR-AD)$ expression on note 1 modified • Table 5.41 Memory Expansion Mode and Microprocessor Mode $t_h(BCLK-AD)$, $t_h(BCLK-CS)$ and $t_h(BCLK-RD)$ values modified; $t_h(WR-AD)$ expression on note 1 modified; $t_h(ALE-AD)$ expression on note 4 modified • Figure 5.7 Vcc1=Vcc2=3.3V Timing Diagram (1) $t_h(BCLK-AD)$, $t_h(BCLK-CS)$ and $t_h(BCLK-RD)$ values modified; $t_{ac1}(AD-DB)$ expression on note 2 modified; $t_h(WR-DB)$, $t_h(WR-AD)$ and $t_w(WR)$ expression on note 3 modified; t_{cyc} expression added • Figure 5.8 Vcc1=Vcc2=3.3V Timing Diagram (2) $t_{ac2}(RD-DB)$ and $t_{ac1}(AD-DB)$ expressions on note 1 modified; $t_h(ALE-AD)$ expressions on notes 1 and 2 modified; $t_d(WR-AD)$, $t_d(DB-WR)$ and $t_h(WR-DB)$ expressions on note 2 modified; t_{cyc} expression added • Figure 5.9 Vcc1=Vcc2=3.3V Timing Diagram (3) $\overline{NMI}$ input diagram added
1.01	Aug. 29, 05		Overview
		17	• Tables 1.6 Pin Description Intelligent I/O functions modified
		29	Special Function Register (SFR)
		29	• The G1BCR0 register Value after reset modified • The G1BCR1 register Value after reset modified
		49	Electrical Characteristics • Table 5.3 Electrical Characteristics I_{CC} standard value modified

REVISION HISTORY		M32C/87 Group Datasheet	
Rev.	Date	Description	
		Page	Summary
1.50	Oct 20, 2007	All	All in this manual • Descriptions and formats unified • Notation of numbers changed (e.g. 00₂ → 00_b, FF₁₆ → FF_h) • Notation of pin name changed (e.g. RTP00 → RTP_0, A15(/D15) → [A15/D15]) • [Term changed] - Serial I/O → Serial interface - Clock synchronous serial I/O mode → Clock synchronous mode - Clock asynchronous serial I/O mode → Clock asynchronous mode - Clock synchronous variable length → Variable data length clock synchronous - Voltage detection circuit → Power supply voltage detection function - Low voltage detection interrupt → Vdet4 detection interrupt - Brown-out detection reset → Vdet3 detection function
		1	Overview • Header SINGLE-CHIP 16/32-BIT CMOS MICROCOMPUTER → RENESAS MCU • 1.1 Features title added; 1.1 Applications changed to 1.1.1 Applications
		2	• 1.2 Performance Overview changed to 1.1.2 Specifications
		2-5	• Tables 1.1 to 1.4 Structure, descriptions in Specification field, NOTE, and value partially revised or deleted • Real-Time Port Item deleted; ROM Correction Function Item added
		8	• 1.3 Block Diagram moved following the 1.2 Product List
		6-7	• 1.2 Product List Tables revised; NOTE 1 added
1.50	Oct 20, 2007	9, 14, 15	• Figures 1.3 to 1.5 Arrows for VSS and VCC deleted; NOTES partially modified
		11,17	• Tables 1.9 and 1.13 CLKOUT pin moved from Bus Control Pin column to Control Pin column
		19-22	• Tables 1.15 to 1.19 Descriptions revised; NOTE 1 added
			Memory • Text partially modified
		26	
		34-39	SFR • Tables 4.8 to 4.13 NOTE “Set the PM13 bit in the PM1 register to 1 (2 wait states for SFR area) before accessing the CAN-associated registers.” added
1.50	Oct 20, 2007	45	• Table 4.19 The PSL5 register added to the Address field of 03BBh item; the PSL7 register added to the Address field of 03BFh item • [Register names changed]
		27	002Fh Low Voltage Detection Interrupt Register → Vdet4 Detection Interrupt Register
		34	01C1h UART5 Bit Rate Register → UART5 Baud Rate Register 01C9h UART6 Bit Rate Register → UART6 Baud Rate Register 01D0h UART5, UART6 Transmit/Receive Control Register 2 → UART5, UART6 Transmit/Receive Control Register 01DBh to 01D8h Pulse Output Data Register → RTP Output Buffer Register
		41	0303h to 0302h Timer A1-1 Register → Timer A11 Register 0305h to 0304h Timer A2-1 Register → Timer A21 Register 0307h to 0306h Timer A4-1 Register → Timer A41 Register
		42	0340h Count Start Flag → Count Start Register 0341h Clock Prescaler Reset Flag → Clock Prescaler Reset Register

REVISION HISTORY		M32C/87 Group Datasheet	
Rev.	Date	Description	
		Page	Summary
		46	Special Function Registers (SFRs) • Table 4.20 A value of After Reset column in 03FFh modified

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