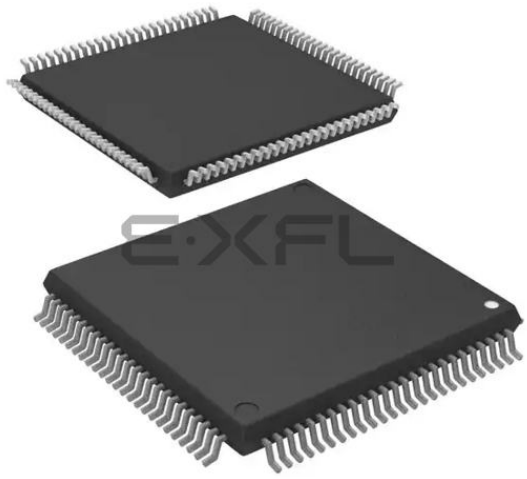

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M32C/80
Core Size	16/32-Bit
Speed	32MHz
Connectivity	CANbus, EBI/EMI, I²C, IEBus, IrDA, SIO, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	85
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30879flagp-u3

Table 1.3 Specifications (100-Pin Package) (1/2)

Item	Function	Specification
CPU	Central processing unit	M32C/80 core (multiplier: 16 bits × 16 bits → 32 bits multiply-addition operation instructions: 16 × 16 + 48 → 48 bits) • Basic instructions: 108 • Minimum instruction execution time: 31.3 ns (f(CPU) = 32 MHz, VCC1 = 4.2 to 5.5 V) 41.7 ns (f(CPU) = 24 MHz, VCC1 = 3.0 to 5.5 V) • Operating mode: Single-chip mode, memory expansion mode, and microprocessor mode
Memory	ROM, RAM, data flash	See **Tables 1.5 to 1.7 Product List**.
Power Supply Voltage Detection		Vdet3 detection function, Vdet4 detection function, cold start/warm start determination function
External Bus Expansion	Bus/memory expansion function	• Address space: 16 Mbytes • External bus interface: 1 to 7 wait states can be inserted, 4 chip select outputs, 3 V and 5 V interfaces • Bus format: Switchable between separate bus and multiplexed bus formats, switchable data bus width (8-bit or 16-bit)
Clock	Clock generation circuits	• 4 circuits: Main clock, sub clock, on-chip oscillator, PLL frequency synthesizer • Oscillation stop detection: Main clock oscillation stop detection function • Frequency divider circuit: Dividing ratio selectable among 1, 2, 3, 4, 6, 8, 10, 12, 14, 16 • Low power consumption features: Wait mode, stop mode
Interrupts		• Interrupt vectors: 70 • External interrupt inputs: 11 ($\overline{\text{NMI}}$, $\overline{\text{INT}}$ × 6, key input × 4) • Interrupt priority levels: 7
Watchdog Timer		15-bit × 1 channel (with prescaler)
DMA	DMAC	• 4 channels, cycle steal method • Trigger sources: 43 • Transfer modes: 2 (single transfer and repeat transfer)
	DMACII	• Can be activated by all peripheral function interrupt sources • Transfer modes: 2 (single transfer and burst transfer) • Immediate transfer, calculation transfer, and chain transfer functions
Timer	Timer A	16-bit timer × 5 Timer mode, event counter mode, one-shot timer mode, pulse width modulation (PWM) mode, Event counter 2-phase pulse signal processing (2-phase encoder input) × 3
	Timer B	16-bit timer × 6 Timer mode, event counter mode, pulse period measurement mode, pulse width measurement mode
	Timer function for 3-phase motor control	3-phase inverter control × 1 (using timer A1, timer A2, timer A4, and timer B2) On-chip dead time timer

1.2 Product List

Tables 1.5 to 1.7 list product information. Figure 1.1 shows product numbering system.

Table 1.5 M32C/87 Group (1) (M32C/87: 2-channel CAN module) Current as of Jul. 2008

Part Number	Package Code	ROM Capacity	RAM Capacity	Remarks
M3087BFLGP	PLQP0144KA-A (144P6Q-A)	1 MB + 4 KB(1)	48 KB	Flash memory
M30879FLFP	PRQP0100JB-A (100P6S-A)			
M30879FLGP	PLQP0100KB-A (100P6Q-A)			
M3087BFKGP	PLQP0144KA-A (144P6Q-A)	768 KB + 4 KB(1)		
M30879FKGP	PLQP0100KB-A (100P6Q-A)			
M30878FJGP	PLQP0144KA-A (144P6Q-A)	512 KB + 4 KB(1)	31 KB	
M30876FJGP	PLQP0100KB-A (100P6Q-A)			
M30875FHGP	PLQP0144KA-A (144P6Q-A)	384 KB + 4 KB(1)	24 KB	
M30873FHGP	PLQP0100KB-A (100P6Q-A)			
M30878MJ-XXXGP	PLQP0144KA-A (144P6Q-A)	512 KB	31 KB	Mask ROM
M30876MJ-XXXFP	PRQP0100JB-A (100P6S-A)			
M30876MJ-XXXGP	PLQP0100KB-A (100P6Q-A)			
M30875MH-XXXGP	PLQP0144KA-A (144P6Q-A)	384 KB	24 KB	
M30873MH-XXXGP	PLQP0100KB-A (100P6Q-A)			

NOTE:
1. Additional 4-Kbyte space is available for data flash memory.

Table 1.6 M32C/87 Group (2) (M32C/87A: 1-channel CAN module) Current as of Jul. 2008

Part Number	Package Code	ROM Capacity	RAM Capacity	Remarks
M3087BFLAGP	PLQP0144KA-A (144P6Q-A)	1 MB + 4 KB(1)	48 KB	Flash memory
M30879FLAFP	PRQP0100JB-A (100P6S-A)			
M30879FLAGP	PLQP0100KB-A (100P6Q-A)			
M3087BFKAGP	PLQP0144KA-A (144P6Q-A)	768 KB + 4 KB(1)		
M30879FKAGP	PLQP0100KB-A (100P6Q-A)			
M30878FJAGP	PLQP0144KA-A (144P6Q-A)	512 KB + 4 KB(1)	31 KB	
M30876FJAGP	PLQP0100KB-A (100P6Q-A)			
M30875FHAGP	PLQP0144KA-A (144P6Q-A)	384 KB + 4 KB(1)	24 KB	
M30873FHAGP	PLQP0100KB-A (100P6Q-A)			
M30878MJA-XXXGP	PLQP0144KA-A (144P6Q-A)	512 KB	31 KB	Mask ROM
M30876MJA-XXXFP	PRQP0100JB-A (100P6S-A)			
M30876MJA-XXXGP	PLQP0100KB-A (100P6Q-A)			
M30875MHA-XXXGP	PLQP0144KA-A (144P6Q-A)	384 KB	24 KB	
M30873MHA-XXXGP	PLQP0100KB-A (100P6Q-A)			

NOTE:
1. Additional 4-Kbyte space is available for data flash memory.

Table 1.10 144-Pin Package List of Pin Names (3/4)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
81		P3_5						A13,[A13/D13]
82		P3_4						A12,[A12/D12]
83		P3_3						A11,[A11/D11]
84		P3_2						A10,[A10/D10]
85		P3_1						A9,[A9/D9]
86		P12_4						
87		P12_3			$\overline{\text{CTS6}}$/$\overline{\text{RTS6}}$			
88		P12_2			RXD6			
89		P12_1			CLK6			
90		P12_0			TXD6			
91	VCC2							
92		P3_0						A8,[A8/D8]
93	VSS							
94		P2_7					AN2_7	A7,[A7/D7]
95		P2_6					AN2_6	A6,[A6/D6]
96		P2_5					AN2_5	A5,[A5/D5]
97		P2_4					AN2_4	A4,[A4/D4]
98		P2_3					AN2_3	A3,[A3/D3]
99		P2_2					AN2_2	A2,[A2/D2]
100		P2_1					AN2_1	A1,[A1/D1]
101		P2_0					AN2_0	A0,[A0/D0]
102		P1_7	$\overline{\text{INT5}}$					D15
103		P1_6	$\overline{\text{INT4}}$					D14
104		P1_5	$\overline{\text{INT3}}$					D13
105		P1_4						D12
106		P1_3						D11
107		P1_2						D10
108		P1_1						D9
109		P1_0						D8
110		P0_7					AN0_7	D7
111		P0_6					AN0_6	D6
112		P0_5					AN0_5	D5
113		P0_4					AN0_4	D4
114		P11_4						
115		P11_3				INPC1_3/OUTC1_3		
116		P11_2				INPC1_2/OUTC1_2/ ISRXD1		
117		P11_1				INPC1_1/OUTC1_1/ ISCLK1		
118		P11_0				INPC1_0/OUTC1_0/ ISTXD1		
119		P0_3					AN0_3	D3
120		P0_2					AN0_2	D2

Table 1.12 100-Pin Package List of Pin Names (1/3)

Pin No.		Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin(1)	Intelligent I/O Pin	Analog Pin	Bus Control Pin
FP	GP								
1	99		P9_6			TXD4/SDA4/SRXD4/ CAN1OUT		ANEX1	
2	100		P9_5			CLK4/CAN1IN/ CAN1WU		ANEX0	
3	1		P9_4		TB4IN	CTS4/RTS4/SS4		DA1	
4	2		P9_3		TB3IN	CTS3/RTS3/SS3		DA0	
5	3		P9_2		TB2IN	TXD3/SDA3/SRXD3	OUTC2_0/IEOUT/ISTXD2		
6	4		P9_1		TB1IN	RXD3/SCL3/STXD3	IEIN/ISRXD2		
7	5		P9_0		TB0IN	CLK3			
8	6	BYTE							
9	7	CNVSS							
10	8	XCIN	P8_7						
11	9	XCOUT	P8_6						
12	10	RESET							
13	11	XOUT							
14	12	VSS							
15	13	XIN							
16	14	VCC1							
17	15		P8_5	NMI					
18	16		P8_4	INT2					
19	17		P8_3	INT1		CAN0IN/CAN1IN			
20	18		P8_2	INT0		CAN0OUT/CAN1OUT			
21	19		P8_1		TA4IN/U/RTP2_3	CTS5/RTS5	INPC1_5/OUTC1_5		
22	20		P8_0		TA4OUT/U	RXD5	ISRXD0		
23	21		P7_7		TA3IN/RTP2_2	CLK5/CAN0IN	INPC1_4/OUTC1_4/ ISCLK0		
24	22		P7_6		TA3OUT	TXD5/CAN0OUT	INPC1_3/OUTC1_3/ ISTXD0		
25	23		P7_5		TA2IN/W/RTP2_1		INPC1_2/OUTC1_2 ISRXD1		
26	24		P7_4		TA2OUT/W/ RTP2_0		INPC1_1/OUTC1_1/ ISCLK1		
27	25		P7_3		TA1IN/V	CTS2/RTS2/SS2	INPC1_0/OUTC1_0/ ISTXD1		
28	26		P7_2		TA1OUT/V	CLK2			
29	27		P7_1		TA0IN/TB5IN/ RTP0_3	RXD2/SCL2/STXD2	INPC1_7/OUTC1_7/ OUTC2_2/ISRXD2/IEIN		
30	28		P7_0		TA0OUT/RTP0_2	TXD2/SDA2/SRXD2	INPC1_6/OUTC1_6/ OUTC2_0/ISTXD2/IEOUT		
31	29		P6_7			TXD1/SDA1/SRXD1			
32	30		P6_6			RXD1/SCL1/STXD1			
33	31		P6_5			CLK1			
34	32		P6_4			CTS1/RTS1/SS1	OUTC2_1/ISCLK2		
35	33		P6_3			TXD0/SDA0/SRXD0/ IrDAOUT			
36	34		P6_2			RXD0/SCL0/STXD0/ IrDAIN			
37	35		P6_1		RTP0_1	CLK0			
38	36		P6_0		RTP0_0	CTS0/RTS0/SS0			
39	37		P5_7						RDY
40	38		P5_6						ALE

NOTE:
1. The CAN pins cannot be used in M32C/87B. Only CAN0 pins can be used in M32C/87A.

Table 1.14 100-Pin Package List of Pin Names (3/3)

Pin No.		Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
FP	GP								
73	71		P1_7	$\overline{INT5}$					D15
74	72		P1_6	$\overline{INT4}$					D14
75	73		P1_5	$\overline{INT3}$					D13
76	74		P1_4						D12
77	75		P1_3						D11
78	76		P1_2						D10
79	77		P1_1						D9
80	78		P1_0						D8
81	79		P0_7					AN0_7	D7
82	80		P0_6					AN0_6	D6
83	81		P0_5					AN0_5	D5
84	82		P0_4					AN0_4	D4
85	83		P0_3					AN0_3	D3
86	84		P0_2					AN0_2	D2
87	85		P0_1					AN0_1	D1
88	86		P0_0					AN0_0	D0
89	87		P10_7	$\overline{KI3}$	RTP3_3			AN_7	
90	88		P10_6	$\overline{KI2}$	RTP3_2			AN_6	
91	89		P10_5	$\overline{KI1}$	RTP3_1			AN_5	
92	90		P10_4	$\overline{KI0}$	RTP3_0			AN_4	
93	91		P10_3		RTP1_3			AN_3	
94	92		P10_2		RTP1_2			AN_2	
95	93		P10_1		RTP1_1			AN_1	
96	94	AVSS							
97	95		P10_0		RTP1_0			AN_0	
98	96	VREF							
99	97	AVCC							
100	98		P9_7			RXD4/SCL4/STXD4		$\overline{ADTRG}$	

1.5 Pin Functions

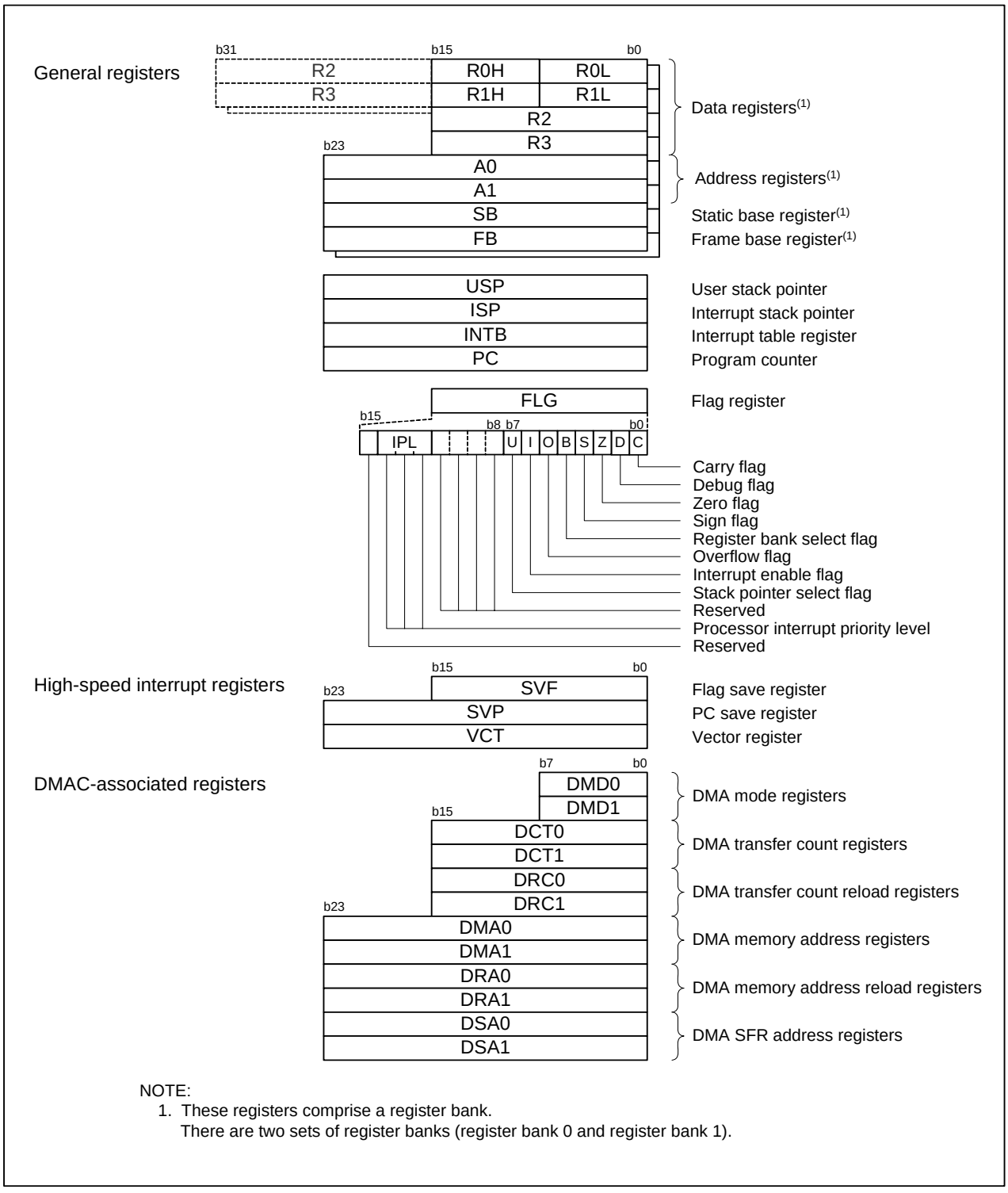
Table 1.15 Pin Functions (100-Pin and 144-Pin Packages) (1/4)

Type	Symbol	I/O Type	Supply Voltage	Description
Power supply	VCC1,VCC2 VSS	–	–	Apply 3.0 to 5.5 V to pins VCC1 and VCC2, and 0 V to the VSS pin. The input condition of VCC1 ≥ VCC2 must be met.
Analog power supply input	AVCC AVSS	–	VCC1	Power supply input pins to the A/D converter and D/A converter. Connect the AVCC pin to VCC1, and the AVSS pin to VSS.
Reset input	$\overline{\text{RESET}}$	I	VCC1	The MCU is placed in the reset state while applying an “L” signal to the $\overline{\text{RESET}}$ pin.
CNVSS	CNVSS	I	VCC1	This pin switches processor mode. Apply an “L” to the CNVSS pin to start up in single-chip mode, or an “H” to start up in microprocessor mode (mask ROM, flash memory version) and boot mode (flash memory version).
External data bus width select input	BYTE	I	VCC1	This pin switches a data bus width in external memory space 3. A data bus is 16 bits wide when the BYTE pin is held “L” and 8 bits wide when it is held “H”. Fix to either “L” or “H”. Apply an “L” to the BYTE pin in single-chip mode.
Bus control Pins	D0 to D7	I/O	VCC2	Data (D0 to D7) input/output pins while accessing an external memory space with separate bus.
	D8 to D15	I/O	VCC2	Data (D8 to D15) input/output pins while accessing an external memory space with 16-bit separate bus.
	A0 to A22	O	VCC2	Address bits (A0 to A22) output pins.
	$\overline{\text{A23}}$	O	VCC2	Inverted address bit (A23) output pin.
	A0/D0 to A7/D7	I/O	VCC2	Data (D0 to D7) input/output and 8 low-order address bits (A0 to A7) output are performed by time-sharing these pins while accessing an external memory space with multiplexed bus.
	A8/D8 to A15/D15	I/O	VCC2	Data (D8 to D15) input/output and 8 middle-order address bits (A8 to A15) output are performed by time-sharing these pins while accessing an external memory space with 16-bit multiplexed bus.
	$\overline{\text{CS0}}$ to $\overline{\text{CS3}}$	O	VCC2	Chip-select signal output pins used to specify external devices.
	$\overline{\text{WRL}}$/$\overline{\text{WR}}$ $\overline{\text{WRH}}$/$\overline{\text{BHE}}$ $\overline{\text{RD}}$	O	VCC2	$\overline{\text{WRL}}$, $\overline{\text{WRH}}$, ($\overline{\text{WR}}$, $\overline{\text{BHE}}$) and $\overline{\text{RD}}$ signal output pins. $\overline{\text{WRL}}$ and $\overline{\text{WRH}}$ can be switched with $\overline{\text{WR}}$ and $\overline{\text{BHE}}$ by a program. • $\overline{\text{WRL}}$, $\overline{\text{WRH}}$ and $\overline{\text{RD}}$ are selected: If external data bus is 16 bits wide, data is written to an even address in external memory space while an “L” is output from the $\overline{\text{WRL}}$ pin. Data is written to an odd address while an “L” is output from the $\overline{\text{WRH}}$ pin. Data is read while an “L” is output from the $\overline{\text{RD}}$ pin. • $\overline{\text{WR}}$, $\overline{\text{BHE}}$ and $\overline{\text{RD}}$ are selected: Data is written while an “L” is output from the $\overline{\text{WR}}$ pin. Data is read while an “L” is output from the $\overline{\text{RD}}$ pin. Data in odd address is accessed while an “L” is output from the $\overline{\text{BHE}}$ pin. Select $\overline{\text{WR}}$, $\overline{\text{BHE}}$ and $\overline{\text{RD}}$ when an external data bus is 8 bits wide.
	ALE	O	VCC2	ALE signal is used for the external devices to latch address signals when the multiplexed bus is selected.
	$\overline{\text{HOLD}}$	I	VCC2	The MCU is placed in a hold state while an “L” signal is applied to the $\overline{\text{HOLD}}$ pin.
	$\overline{\text{HLDA}}$	O	VCC2	The $\overline{\text{HLDA}}$ pin outputs an “L” while the MCU is placed in a hold state.
	$\overline{\text{RDY}}$	I	VCC2	Bus is placed in a wait state while an “L” signal is applied to the $\overline{\text{RDY}}$ pin.

I: Input O: Output I/O: Input and output

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers.
The register bank is comprised of eight registers (R0, R1, R2, R3, A0, A1, SB, and FB) out of 28 CPU registers. There are two sets of register banks.



NOTE:
1. These registers comprise a register bank.
There are two sets of register banks (register bank 0 and register bank 1).

Figure 2.1 CPU Register

2.1.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.
Interrupts are disabled when the I flag is set to 0 and enabled when it is set to 1. The I flag becomes 0 when an interrupt request is acknowledged.

2.1.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0. USP is selected when the U flag is set to 1.
The U flag becomes 0 when a hardware interrupt request is acknowledged or the INT instruction specifying software interrupt numbers 0 to 31 is executed.

2.1.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has higher priority level than IPL, the interrupt is enabled.

2.1.8.10 Reserved Space

Only write 0 to bits assigned to the reserved space. When read, the bits return undefined values.

2.2 High-Speed Interrupt Registers

Registers associated with the high-speed interrupt are as follows:

- Flag save register (SVF)
- PC save register (SVP)
- Vector register (VCT)

2.3 DMAC-Associated Registers

Registers associated with the DMAC are as follows:

- DMA mode register (DMD0, DMD1)
- DMA transfer count register (DCT0, DCT1)
- DMA transfer count reload register (DRC0, DRC1)
- DMA memory address register (DMA0, DMA1)
- DMA memory address reload register (DRA0, DRA1)
- DMA SFR address register (DSA0, DSA1)

Table 4.3 SFR Address Map (3/20)

Address	Register	Symbol	After Reset
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h	DMA0 Interrupt Control Register	DM0IC	XXXX X000b
0069h	Timer B5 Interrupt Control Register	TB5IC	XXXX X000b
006Ah	DMA2 Interrupt Control Register	DM2IC	XXXX X000b
006Bh	UART2 Receive/ACK Interrupt Control Register	S2RIC	XXXX X000b
006Ch	Timer A0 Interrupt Control Register	TA0IC	XXXX X000b
006Dh	UART3 Receive/ACK Interrupt Control Register	S3RIC	XXXX X000b
006Eh	Timer A2 Interrupt Control Register	TA2IC	XXXX X000b
006Fh	UART4 Receive/ACK Interrupt Control Register	S4RIC	XXXX X000b
0070h	Timer A4 Interrupt Control Register	TA4IC	XXXX X000b
0071h	UART0/UART3 Bus Conflict Detection Interrupt Control Register	BCN0IC/BCN3IC	XXXX X000b
0072h	UART0 Receive/ACK Interrupt Control Register	S0RIC	XXXX X000b
0073h	A/D0 Conversion Interrupt Control Register	AD0IC	XXXX X000b
0074h	UART1 Receive/ACK Interrupt Control Register	S1RIC	XXXX X000b
0075h	II/O Interrupt Control Register 0 / CAN1 interrupt Control Register 0	IIO0IC/CAN3IC	XXXX X000b
0076h	Timer B1 Interrupt Control Register	TB1IC	XXXX X000b
0077h	II/O Interrupt Control Register 2	IIO2IC	XXXX X000b
0078h	Timer B3 Interrupt Control Register	TB3IC	XXXX X000b
0079h	II/O Interrupt Control Register 4	IIO4IC	XXXX X000b
007Ah	$\overline{\text{INT5}}$ Interrupt Control Register	INT5IC	XX00 X000b
007Bh	II/O Interrupt Control Register 6	IIO6IC	XXXX X000b
007Ch	$\overline{\text{INT3}}$ Interrupt Control Register	INT3IC	XX00 X000b
007Dh	II/O Interrupt Control Register 8	IIO8IC	XXXX X000b
007Eh	$\overline{\text{INT1}}$ Interrupt Control Register	INT1IC	XX00 X000b
007Fh	II/O Interrupt Control Register 10 / CAN0 Interrupt Control Register 1	IIO10IC/CAN1IC	XXXX X000b
0080h			
0081h	II/O Interrupt Control Register 11 / CAN0 Interrupt Control Register 2	IIO11IC/CAN2IC	XXXX X000b
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h	DMA1 Interrupt Control Register	DM1IC	XXXX X000b
0089h	UART2 Transmit/NACK Interrupt Control Register	S2TIC	XXXX X000b
008Ah	DMA3 Interrupt Control Register	DM3IC	XXXX X000b
008Bh	UART3 Transmit/NACK Interrupt Control Register	S3TIC	XXXX X000b
008Ch	Timer A1 Interrupt Control Register	TA1IC	XXXX X000b
008Dh	UART4 Transmit/NACK Interrupt Control Register	S4TIC	XXXX X000b
008Eh	Timer A3 Interrupt Control Register	TA3IC	XXXX X000b
008Fh	UART2 Bus Conflict Detection Interrupt Control Register	BCN2IC	XXXX X000b

X: Undefined
Blank spaces are all reserved. No access is allowed.

Table 4.7 SFR Address Map (7/20)

Address	Register	Symbol	After Reset
0150h	Group 2 Waveform Generation Control Register 0	G2POCR0	00h
0151h	Group 2 Waveform Generation Control Register 1	G2POCR1	00h
0152h	Group 2 Waveform Generation Control Register 2	G2POCR2	00h
0153h	Group 2 Waveform Generation Control Register 3	G2POCR3	00h
0154h	Group 2 Waveform Generation Control Register 4	G2POCR4	00h
0155h	Group 2 Waveform Generation Control Register 5	G2POCR5	00h
0156h	Group 2 Waveform Generation Control Register 6	G2POCR6	00h
0157h	Group 2 Waveform Generation Control Register 7	G2POCR7	00h
0158h			
0159h			
015Ah			
015Bh			
015Ch			
015Dh			
015Eh			
015Fh			
0160h	Group 2 Base Timer Register	G2BT	XXXXh
0161h			
0162h	Group 2 Base Timer Control Register 0	G2BCR0	00h
0163h	Group 2 Base Timer Control Register 1	G2BCR1	00h
0164h	Base Timer Start Register	BTSR	XXXX 0000b
0165h			
0166h	Group 2 Function Enable Register	G2FE	00h
0167h	Group 2 RTP Output Buffer Register	G2RTP	00h
0168h			
0169h			
016Ah	Group 2 SI/O Communication Mode Register	G2MR	00XX X000b
016Bh	Group 2 SI/O Communication Control Register	G2CR	0000 X000b
016Ch	Group 2 SI/O Transmit Buffer Register	G2TB	XXXXh
016Dh			
016Eh	Group 2 SI/O Receive Buffer Register	G2RB	XXXXh
016Fh			
0170h	Group 2 IEBus Address Register	IEAR	XXXXh
0171h			
0172h	Group 2 IEBus Control Register	IECR	00XX X000b
0173h	Group 2 IEBus Transmit Interrupt Source Detection Register	IETIF	XXX0 0000b
0174h	Group 2 IEBus Receive Interrupt Source Detection Register	IERIF	XXX0 0000b
0175h			
0176h			
0177h	Input Function Select Register B	IPSB	00h
0178h	Input Function Select Register	IPS	00h
0179h	Input Function Select Register A	IPSA	00h
017Ah			
017Bh			
017Ch			
017Dh to 01BFh			

X: Undefined
Blank spaces are all reserved. No access is allowed.

Table 4.10 SFR Address Map (10/20)

Address	Register[3][4]	Symbol	After Reset
0220h	CAN0 Single Shot Control Register	C0SSCTLR	0000h[1][2]
0221h			
0222h			
0223h			
0224h	CAN0 Single Shot Status Register	C0SSSTR	0000h[1][2]
0225h			
0226h			
0227h			
0228h	CAN0 Global Mask Register Standard ID0	C0GMR0	XXX0 0000b[1][2]
0229h	CAN0 Global Mask Register Standard ID1	C0GMR1	XX00 0000b[1][2]
022Ah	CAN0 Global Mask Register Extended ID0	C0GMR2	XXXX 0000b[1][2]
022Bh	CAN0 Global Mask Register Extended ID1	C0GMR3	00h[1][2]
022Ch	CAN0 Global Mask Register Extended ID2	C0GMR4	XX00 0000b[1][2]
022Dh			
022Eh			
022Fh			
0230h	CAN0 Message Slot 0 Control Register / CAN0 Local Mask Register A Standard ID0	C0MCTL0 / C0LMAR0	0000 0000b[1][2]/ XXX0 0000b[1][2]
0231h	CAN0 Message Slot 1 Control Register / CAN0 Local Mask Register A Standard ID1	C0MCTL1 / C0LMAR1	0000 0000b[1][2]/ XX00 0000b[1][2]
0232h	CAN0 Message Slot 2 Control Register / CAN0 Local Mask Register A Extended ID0	C0MCTL2 / C0LMAR2	0000 0000b[1][2]/ XXXX 0000b[1][2]
0233h	CAN0 Message Slot 3 Control Register / CAN0 Local Mask Register A Extended ID1	C0MCTL3 / C0LMAR3	00h[1][2]/ 00h[1][2]
0234h	CAN0 Message Slot 4 Control Register / CAN0 Local Mask Register A Extended ID2	C0MCTL4 / C0LMAR4	0000 0000b[1][2]/ XX00 0000b[1][2]
0235h	CAN0 Message Slot 5 Control Register	C0MCTL5	00h[1][2]
0236h	CAN0 Message Slot 6 Control Register	C0MCTL6	00h[1][2]
0237h	CAN0 Message Slot 7 Control Register	C0MCTL7	00h[1][2]
0238h	CAN0 Message Slot 8 Control Register / CAN0 Local Mask Register B Standard ID0	C0MCTL8 / C0LMBR0	0000 0000b[1][2]/ XXX0 0000b[1][2]
0239h	CAN0 Message Slot 9 Control Register / CAN0 Local Mask Register B Standard ID1	C0MCTL9 / C0LMBR1	0000 0000b[1][2]/ XX00 0000b[1][2]
023Ah	CAN0 Message Slot 10 Control Register / CAN0 Local Mask Register B Extended ID0	C0MCTL10 / C0LMBR2	0000 0000b[1][2]/ XXXX 0000b[1][2]
023Bh	CAN0 Message Slot 11 Control Register / CAN0 Local Mask Register B Extended ID1	C0MCTL11 / C0LMBR3	00h[1][2]/ 00h[1][2]
023Ch	CAN0 Message Slot 12 Control Register / CAN0 Local Mask Register B Extended ID2	C0MCTL12 / C0LMBR4	0000 0000b[1][2]/ XX00 0000b[1][2]
023Dh	CAN0 Message Slot 13 Control Register	C0MCTL13	00h[1][2]
023Eh	CAN0 Message Slot 14 Control Register	C0MCTL14	00h[1][2]
023Fh	CAN0 Message Slot 15 Control Register	C0MCTL15	00h[1][2]
0240h	CAN0 Slot Buffer Select Register	C0SBS	00h[2]
0241h	CAN0 Control Register 1	C0CTLR1	X000 00XXb[2]
0242h	CAN0 Sleep Control Register	C0SLPR	XXXX XXX0b
0243h			
0244h	CAN0 Acceptance Filter Support Register	C0AFS	0000 0000b[2]
0245h			0000 0001b[2]
0246h			
0247h			
0248h			
0249h			
024Ah to 024Fh			

X: Undefined
Blank spaces are all reserved. No access is allowed.
NOTES:

1. The BANKSEL bit in the C0CTLR1 register can switch functions for addresses 0220h to 023Fh.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to “1” (sleep mode exited) after reset and supplying a clock to the CAN module.
3. The CAN-associated registers (allocated in addresses 01E0h to 02BFh) cannot be used in M32C/87B. In M32C/87A, only CAN0-associated registers can be used.
4. Set the PM13 bit in the PM1 register to 1 (2 wait states for SFR area) before accessing the CAN-associated registers.

Table 4.14 SFR Address Map (14/20)

Address	Register	Symbol	After Reset
02C0h	X0 Register, Y0 Register	X0R, Y0R	XXXXh
02C1h			
02C2h	X1 Register, Y1 Register	X1R, Y1R	XXXXh
02C3h			
02C4h	X2 Register, Y2 Register	X2R, Y2R	XXXXh
02C5h			
02C6h	X3 Register, Y3 Register	X3R, Y3R	XXXXh
02C7h			
02C8h	X4 Register, Y4 Register	X4R, Y4R	XXXXh
02C9h			
02CAh	X5 Register, Y5 Register	X5R, Y5R	XXXXh
02CBh			
02CCh	X6 Register, Y6 Register	X6R, Y6R	XXXXh
02CDh			
02CEh	X7 Register, Y7 Register	X7R, Y7R	XXXXh
02CFh			
02D0h	X8 Register, Y8 Register	X8R, Y8R	XXXXh
02D1h			
02D2h	X9 Register, Y9 Register	X9R, Y9R	XXXXh
02D3h			
02D4h	X10 Register, Y10 Register	X10R, Y10R	XXXXh
02D5h			
02D6h	X11 Register, Y11 Register	X11R, Y11R	XXXXh
02D7h			
02D8h	X12 Register, Y12 Register	X12R, Y12R	XXXXh
02D9h			
02DAh	X13 Register, Y13 Register	X13R, Y13R	XXXXh
02DBh			
02DCh	X14 Register, Y14 Register	X14R, Y14R	XXXXh
02DDh			
02DEh	X15 Register, Y15 Register	X15R, Y15R	XXXXh
02DFh			
02E0h	X/Y Control Register	XYC	XXXX XX00b
02E1h			
02E2h			
02E3h			
02E4h	UART1 Special Mode Register 4	U1SMR4	00h
02E5h	UART1 Special Mode Register 3	U1SMR3	00h
02E6h	UART1 Special Mode Register 2	U1SMR2	00h
02E7h	UART1 Special Mode Register	U1SMR	00h
02E8h	UART1 Transmit/Receive Mode Register	U1MR	00h
02E9h	UART1 Baud Rate Register	U1BRG	XXh
02EAh	UART1 Transmit Buffer Register	U1TB	XXXXh
02EBh			
02ECh	UART1 Transmit/Receive Control Register 0	U1C0	0000 1000b
02EDh	UART1 Transmit/Receive Control Register 1	U1C1	0000 0010b
02EEh	UART1 Receive Buffer Register	U1RB	XXXXh
02EFh			

X: Undefined
Blank spaces are all reserved. No access is allowed.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter		Condition	Value	Unit
VCC1, VCC2	Supply voltage		VCC1 = AVCC	-0.3 to 6.0	V
VCC2	Supply voltage		–	-0.3 to VCC1 + 0.1	V
AVCC	Analog supply voltage		VCC1 = AVCC	-0.3 to 6.0	V
VI	Input voltage	$\overline{\text{RESET}}$, CNVSS, BYTE, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P14_0 to P14_6, P15_0 to P15_7(1), VREF, XIN		-0.3 to VCC1 + 0.3	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7(1)		-0.3 to VCC2 + 0.3	
		P7_0, P7_1		-0.3 to 6.0	
VO	Output voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P14_0 to 14_6, P15_0 to P15_7(1), XOUT		-0.3 to VCC1 + 0.3	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7(1)		-0.3 to VCC2 + 0.3	
		P7_0, P7_1		-0.3 to 6.0	
Pd	Power consumption		-40°C≤Topr≤85°C	500	mW
Topr	Operating ambient temperature	during CPU operation		-20 to 85/ -40 to 85(2)	°C
		during programming or erasing Flash memory		0 to 60	°C
Tstg	Storage temperature			-65 to 150	°C

NOTES:
1. P11 to P15 are provided in the 144-pin package only.
2. Contact a Renesas sales office if temperature range of -40 to 85°C is required.

VCC1 = VCC2 = 5V

Table 5.7 Electrical Characteristics (3/3)
(VCC1 = VCC2 = 5.5 V, VSS = 0 V, Topr = 25°C)

Symbol	Parameter	Measurement Condition(1)		Standard			Unit
				Min.	Typ.	Max.	
ICC	Power supply current	Flash memory version	f(CPU) = 32 MHz		32	45	mA
			f(CPU) = 16 MHz		19		mA
			f(CPU) = 8 MHz		12		mA
			f(CPU) = f(Ring) In on-chip oscillator low-power consumption mode		2.6		mA
			f(CPU) = 32 kHz In low-power consumption mode While flash memory is operating		430		µA
			f(CPU) = 32 kHz In low-power consumption mode While flash memory is stopped(2)		30		µA
			Wait mode: f(CPU) = f(Ring) After entering wait mode from on-chip oscillator low-power consumption mode		50		µA
			Stop mode (while clock is stopped)		0.8	5	µA
			Stop mode (while clock is stopped) Topr = 85°C			50	µA
		Mask ROM version	f(CPU) = 32 MHz		32	45	mA
			f(CPU) = 16 MHz		19		mA
			f(CPU) = 8 MHz		12		mA
			f(CPU) = f(Ring) In on-chip oscillator low-power consumption mode		1		mA
			f(CPU) = 32 kHz In low-power consumption mode		30		µA
			Wait mode: f(CPU) = f(Ring) After entering wait mode from on-chip oscillator low-power consumption mode		50		µA
			Stop mode (while clock is stopped)		0.8	5	µA
			Stop mode (while clock is stopped) Topr = 85°C			50	µA

NOTES:
1. In single-chip mode, leave the output pins open and connect the input pins to VSS.
2. Value is obtained when setting the FMSTP bit in the FMR0 register to 1 (flash memory stopped) and running the program on RAM.

VCC1 = VCC2 = 5V

Table 5.10 Flash Memory Electrical Characteristics (VCC1 = 4.5 V to 5.5 V, 3.0 to 3.6 V, Topr = 0 to 60°C unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
–	Erase and program endurance(1)		100			times
–	Word program time (16 bits) (VCC1 = 5.0 V, Topr = 25°C)			25	300	µs
–	Lock bit program time			25	300	µs
–	Block erase time (VCC1 = 5.0 V, Topr = 25°C)	4-Kbyte block		0.3	4	s
		8-Kbyte block		0.3	4	s
		32-Kbyte block		0.5	4	s
		64-Kbyte block		0.8	4	s
tps	Wait time to stabilize flash memory circuit				15	µs
–	Data hold time (Topr = -40 to 85°C)		10			years

NOTE:
1. If erase and program endurance is n times (n = 100), each block can be erased n times. For example, if a 4-Kbyte block A is erased after programming a word data 2,048 times, each to a different address, this counts as one erase and program time. Data can not be programmed to the same address more than once without erasing the block. (rewrite prohibited)

VCC1 = VCC2 = 3.3 V

Table 5.31 Electrical Characteristics (1/3)

(VCC1 = VCC2 = 3.0 to 3.6 V, VSS = 0 V, Topr = -20 to 85°C, f(CPU) = 24 MHz unless otherwise specified)

Symbol	Parameter		Measurement Condition	Standard			Unit
				Min.	Typ.	Max.	
VOH	Output high “H” voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7(1)	IOH = -1 mA	VCC2 - 0.6		VCC2	V
		P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7,P10_0 to P10_7, P14_0 to P14_6, P15_0 to P15_7(1)		VCC1 - 0.6		VCC1	
		XOUT	IOH = -0.1 mA	2.7		VCC1	V
		XCOUT Drive capability = high	No load applied		2.5		V
		XCOUT Drive capability = low	No load applied		1.6		V
VOL	Output low “L” voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7,P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7(1)	IOL = 1 mA			0.5	V
		XOUT	IOL = 0.1 mA			0.5	V
		XCOUT Drive capability = high	No load applied		0		V
		XCOUT Drive capability = low	No load applied		0		V
VT+ - VT-	Hysteresis	$\overline{\text{HOLD}}$, $\overline{\text{RDY}}$, TA0IN to TA4IN, $\overline{\text{TB0IN}}$ to $\overline{\text{TB5IN}}$, $\overline{\text{INT0}}$ to $\overline{\text{INT8}}$, $\overline{\text{ADTRG}}$, $\overline{\text{CTS0}}$ to $\overline{\text{CTS6}}$, CLK0 to CLK6, TA0OUT to TA4OUT, $\overline{\text{NMI}}$, $\overline{\text{KI0}}$ to $\overline{\text{KI3}}$, RXD0 to RXD6, SCL0 to SCL4, SDA0 to SDA4, INPC1_0 to INPC1_7, ISCLK0 to ISCLK2, ISRXD0 to ISRXD2, IEIN, CAN0IN, CAN1IN, $\overline{\text{CAN1WU}}$		0.2		1.0	V
		$\overline{\text{RESET}}$		0.2		1.8	V

NOTE:

1. P11 to P15 are provided in the 144-pin package only.

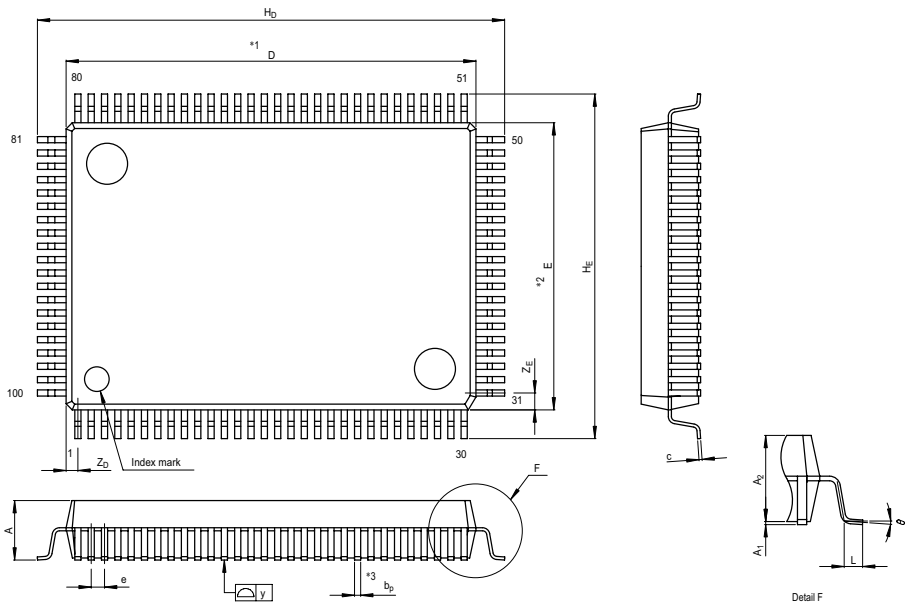
VCC1 = VCC2 = 3.3 V

Table 5.33 Electrical Characteristics (3/3)
(VCC1 = VCC2 = 3.3 V, VSS = 0 V, Topr = 25°C)

Symbol	Parameter	Measurement Condition(1)		Standard			Unit
				Min.	Typ.	Max.	
ICC	Power supply current	Flash memory version	f(CPU) = 24 MHz		23	33	mA
			f(CPU) = 16 MHz		17		mA
			f(CPU) = 8 MHz		11		mA
			f(CPU) = f(Ring) In on-chip oscillator low-power consumption mode		2.6		mA
			f(CPU) = 32 kHz In low-power consumption mode While flash memory is operating		430		µA
			f(CPU) = 32 kHz In low-power consumption mode While flash memory is stopped(2)		30		µA
			Wait mode: f(CPU) = f(Ring) After entering wait mode from on-chip oscillator low-power consumption mode		45		µA
			Stop mode (while clock is stopped)		0.8	5	µA
			Stop mode (while clock is stopped) Topr = 85°C			50	µA
		Mask ROM version	f(CPU) = 24 MHz		23	33	mA
			f(CPU) = 16 MHz		17		mA
			f(CPU) = 8 MHz		11		mA
			f(CPU) = f(Ring) In on-chip oscillator low-power consumption mode		1		mA
			f(CPU) = 32 kHz In low-power consumption mode		30		µA
			Wait mode: f(CPU) = f(Ring) After entering wait mode from on-chip oscillator low-power consumption mode		45		µA
			Stop mode (while clock is stopped)		0.8	5	µA
			Stop mode (while clock is stopped) Topr = 85°C			50	µA

NOTES:
1. In single-chip mode, leave the output pins open and connect the input pins to VSS.
2. Value is obtained when setting the FMSTP bit in the FMR0 register to 1 (flash memory stopped) and running the program on RAM.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-QFP100-14x20-0.65	PRQP0100JB-A	100P6S-A	1.6g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.8	20.0	20.2
E	13.8	14.0	14.2
A_2	—	2.8	—
H_D	22.5	22.8	23.1
H_E	16.5	16.8	17.1
A	—	—	3.05
A_1	0	0.1	0.2
b_p	0.25	0.3	0.4
c	0.13	0.15	0.2
θ	0°	—	10°
e	0.5	0.65	0.8
y	—	—	0.10
Z_D	—	0.575	—
Z_E	—	0.825	—
L	0.4	0.6	0.8

REVISION HISTORY	M32C/87 Group Datasheet

Rev.	Date	Description	
		Page	Summary
		46	**Special Function Registers (SFRs)** • **Table 4.20** A value of After Reset column in 03FFh modified

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