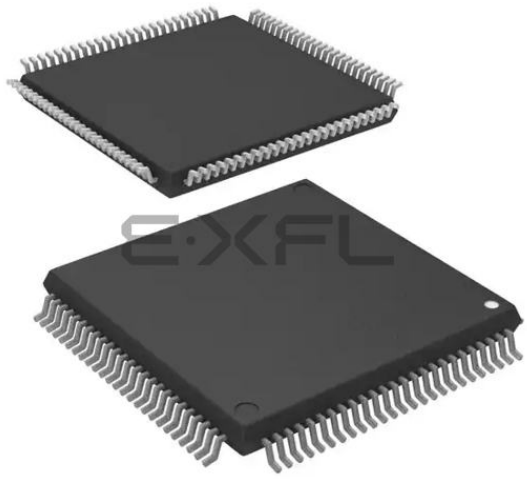
Renesas Electronics America Inc - M30879FLGP#U5 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	M32C/80
Core Size	16/32-Bit
Speed	32MHz
Connectivity	CANbus, EBI/EMI, I²C, IEBus, IrDA, SIO, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	85
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30879flgp-u5

Table 1.4 Specifications (100-Pin Package) (2/2)

Item	Function	Specification
Serial Interface	UART0 to UART4	Clock synchronous/asynchronous × 5 I^2C bus, special mode 2, GCI mode, SIM mode, IrDA mode(2), IEBus (optional)(1)(3)
	UART5	Clock synchronous/asynchronous × 1
A/D Converter		10-bit resolution × 26 channels (in single-chip mode) 10-bit resolution × 10 channels (in memory expansion mode and microprocessor mode) Including sample and hold function
D/A Converter		8-bit resolution × 2 channels
CRC Calculation Circuit		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) compliant
X/Y Converter		16 bits x 16 bits
Intelligent I/O		16-bit timer × 2 • Time measurement function (input capture): 8 channels • Waveform generation function (output compare): 10 channels • Communication function: Clock synchronous mode, clock asynchronous mode, HDLC data processing mode, IEBus (optional)(1)(3) • 2-phase pulse signal processing (2-phase encoder input) × 1
ROM Correction Function		Address match interrupt × 8
CAN modules		Supporting CAN 2.0B specification M32C/87: 16 slots × 2 channels, M32C/87A: 16 slots × 1 channel M32C/87B: none
I/O Ports	Programmable I/O ports	• Input only: 1 • CMOS I/O: 85, selectable pull-up resistor • N channel open drain ports: 2
Flash Memory		• Erase and program voltage: 3.3 V ± 0.3 V or 5.0 V ± 0.5 V • Erase and program endurance: 100 times (all areas) • Program security: ROM code protect and ID code check • Debug functions: On-chip debug and on-board flash reprogram
Operating Frequency/Supply Voltage		32 MHz: VCC1 = 4.2 to 5.5 V, VCC2 = 3.0 V to VCC1 24 MHz: VCC1 = 3.0 to 5.5 V, VCC2 = 3.0 V to VCC1
Current Consumption		32 mA (32 MHz, VCC1 = VCC2 = 5 V) 23 mA (24 MHz, VCC1 = VCC2 = 3.3 V) 45 μA (approx. 1 MHz, VCC1 = VCC2 = 3.3 V, on-chip oscillator low-power consumption mode → wait mode) 0.8 μA (VCC1 = VCC2 = 3.3 V, stop mode)
Operating Ambient Temperature (°C)		-20 to 85°C, -40 to 85°C (optional)(3)
Package		100-pin LQFP (PLQP0100KB-A) 100-pin QFP (PRQP0100JB-A)

NOTES:
1. IEBus is a registered trademark of NEC Electronics Corporation.
2. Available in UART0.
3. Please contact a Renesas sales office for optional features.

1.2 Product List

Tables 1.5 to 1.7 list product information. Figure 1.1 shows product numbering system.

Table 1.5 M32C/87 Group (1) (M32C/87: 2-channel CAN module) Current as of Jul. 2008

Part Number	Package Code	ROM Capacity	RAM Capacity	Remarks
M3087BFLGP	PLQP0144KA-A (144P6Q-A)	1 MB + 4 KB(1)	48 KB	Flash memory
M30879FLFP	PRQP0100JB-A (100P6S-A)			
M30879FLGP	PLQP0100KB-A (100P6Q-A)			
M3087BFKGP	PLQP0144KA-A (144P6Q-A)	768 KB + 4 KB(1)		
M30879FKGP	PLQP0100KB-A (100P6Q-A)			
M30878FJGP	PLQP0144KA-A (144P6Q-A)	512 KB + 4 KB(1)	31 KB	
M30876FJGP	PLQP0100KB-A (100P6Q-A)			
M30875FHGP	PLQP0144KA-A (144P6Q-A)	384 KB + 4 KB(1)	24 KB	
M30873FHGP	PLQP0100KB-A (100P6Q-A)			
M30878MJ-XXXGP	PLQP0144KA-A (144P6Q-A)	512 KB	31 KB	Mask ROM
M30876MJ-XXXFP	PRQP0100JB-A (100P6S-A)			
M30876MJ-XXXGP	PLQP0100KB-A (100P6Q-A)			
M30875MH-XXXGP	PLQP0144KA-A (144P6Q-A)	384 KB	24 KB	
M30873MH-XXXGP	PLQP0100KB-A (100P6Q-A)			

NOTE:
1. Additional 4-Kbyte space is available for data flash memory.

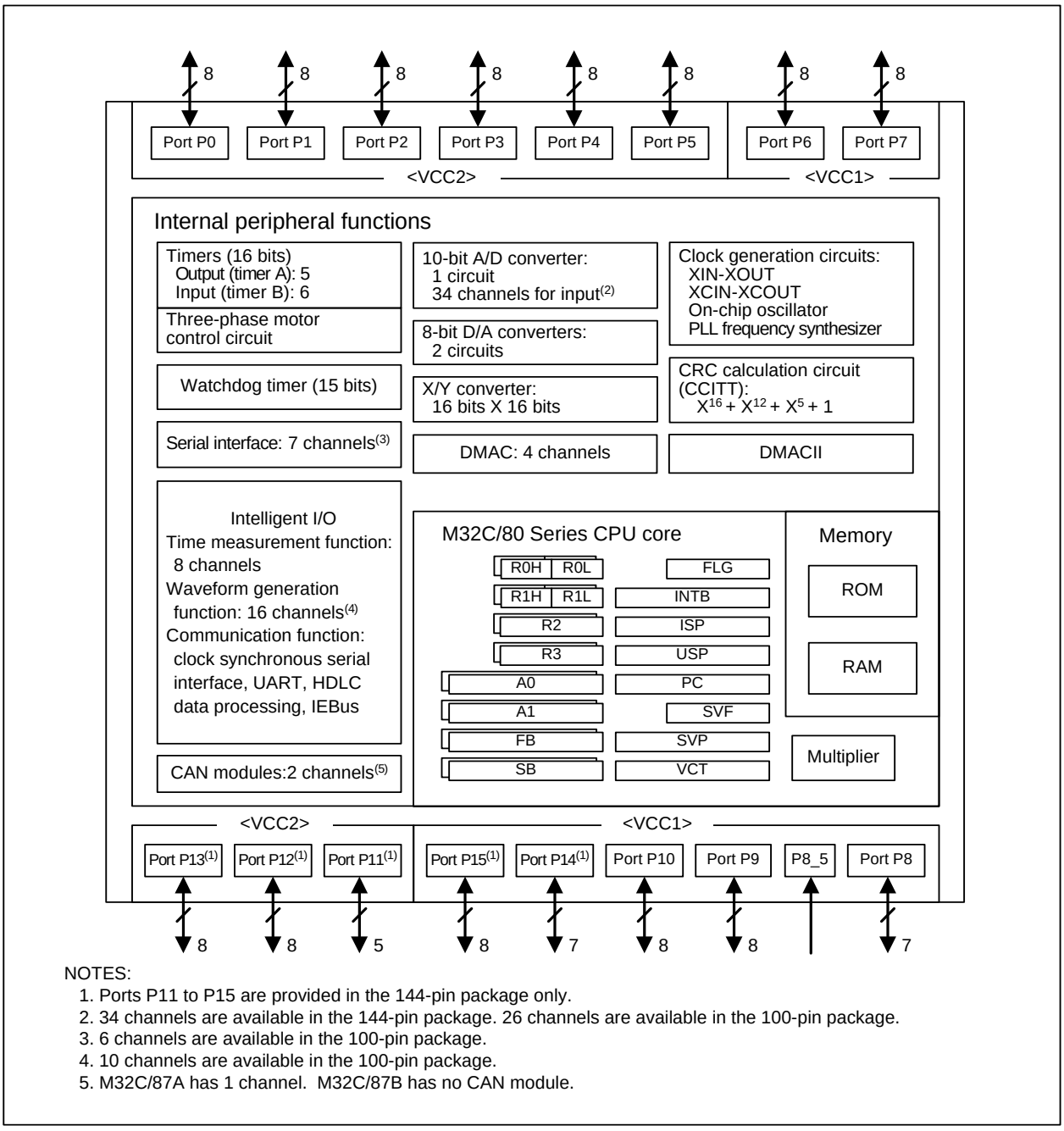
Table 1.6 M32C/87 Group (2) (M32C/87A: 1-channel CAN module) Current as of Jul. 2008

Part Number	Package Code	ROM Capacity	RAM Capacity	Remarks
M3087BFLAGP	PLQP0144KA-A (144P6Q-A)	1 MB + 4 KB(1)	48 KB	Flash memory
M30879FLAFP	PRQP0100JB-A (100P6S-A)			
M30879FLAGP	PLQP0100KB-A (100P6Q-A)			
M3087BFKAGP	PLQP0144KA-A (144P6Q-A)	768 KB + 4 KB(1)		
M30879FKAGP	PLQP0100KB-A (100P6Q-A)			
M30878FJAGP	PLQP0144KA-A (144P6Q-A)	512 KB + 4 KB(1)	31 KB	
M30876FJAGP	PLQP0100KB-A (100P6Q-A)			
M30875FHAGP	PLQP0144KA-A (144P6Q-A)	384 KB + 4 KB(1)	24 KB	
M30873FHAGP	PLQP0100KB-A (100P6Q-A)			
M30878MJA-XXXGP	PLQP0144KA-A (144P6Q-A)	512 KB	31 KB	Mask ROM
M30876MJA-XXXFP	PRQP0100JB-A (100P6S-A)			
M30876MJA-XXXGP	PLQP0100KB-A (100P6Q-A)			
M30875MHA-XXXGP	PLQP0144KA-A (144P6Q-A)	384 KB	24 KB	
M30873MHA-XXXGP	PLQP0100KB-A (100P6Q-A)			

NOTE:
1. Additional 4-Kbyte space is available for data flash memory.

1.3 Block Diagram

Figure 1.2 shows a block diagram of the M32C/87 Group (M32C/87, M32C/87A, M32C/87B).



NOTES:
1. Ports P11 to P15 are provided in the 144-pin package only.
2. 34 channels are available in the 144-pin package. 26 channels are available in the 100-pin package.
3. 6 channels are available in the 100-pin package.
4. 10 channels are available in the 100-pin package.
5. M32C/87A has 1 channel. M32C/87B has no CAN module.

Figure 1.2 M32C/87 Group (M32C/87, M32C/87A, M32C/87B) Block Diagram

Table 1.9 144-Pin Package List of Pin Names (2/4)

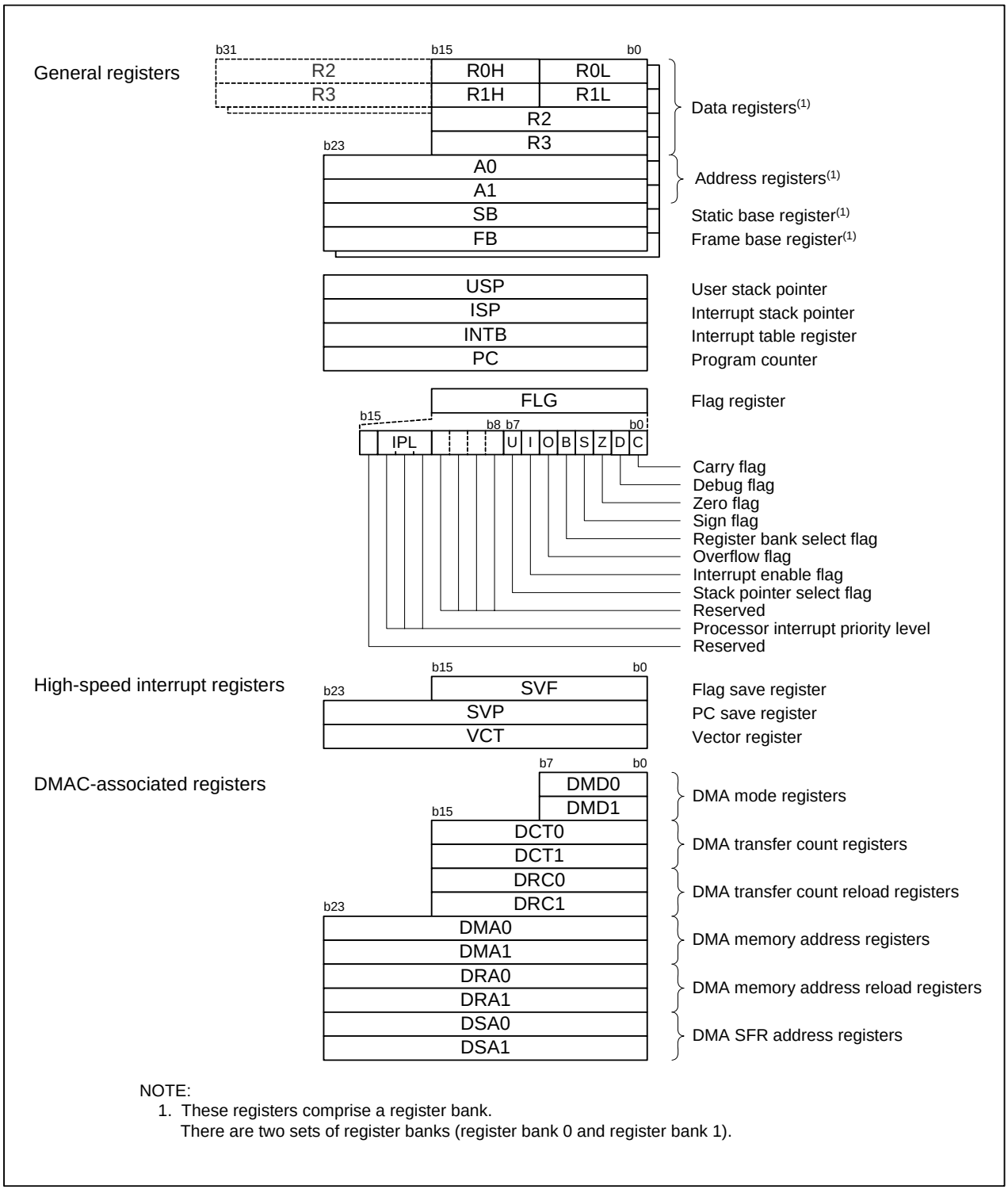
Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
41	VSS							
42		P6_5			CLK1			
43		P6_4			$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$/$\overline{\text{SS1}}$	OUTC2_1/ISCLK2		
44		P6_3			TXD0/SDA0/SRXD0/ IrDAOUT			
45		P6_2			RXD0/SCL0/STXD0/ IrDAIN			
46		P6_1		RTP0_1	CLK0			
47		P6_0		RTP0_0	$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$/$\overline{\text{SS0}}$			
48		P13_7				OUTC2_7		
49		P13_6				OUTC2_1/ISCLK2		
50		P13_5				OUTC2_2/ISRXD2/ IEIN		
51		P13_4				OUTC2_0/ISTXD2/ IEOUT		
52		P5_7						$\overline{\text{RDY}}$
53		P5_6						ALE
54		P5_5						$\overline{\text{HOLD}}$
55		P5_4						$\overline{\text{HLDA}}$/ALE
56		P13_3				OUTC2_3		
57	VSS							
58		P13_2				OUTC2_6		
59	VCC2							
60		P13_1				OUTC2_5		
61		P13_0				OUTC2_4		
62	CLKOUT	P5_3						BCLK/ALE
63		P5_2						$\overline{\text{RD}}$
64		P5_1						$\overline{\text{WRH}}$/$\overline{\text{BHE}}$
65		P5_0						$\overline{\text{WRL}}$/$\overline{\text{WR}}$
66		P12_7						
67		P12_6						
68		P12_5						
69		P4_7						$\overline{\text{CS0}}$/A23
70		P4_6						$\overline{\text{CS1}}$/A22
71		P4_5						$\overline{\text{CS2}}$/A21
72		P4_4						$\overline{\text{CS3}}$/A20
73		P4_3						A19
74	VCC2							
75		P4_2						A18
76	VSS							
77		P4_1						A17
78		P4_0						A16
79		P3_7						A15,[A15/D15]
80		P3_6						A14,[A14/D14]

Table 1.14 100-Pin Package List of Pin Names (3/3)

Pin No.		Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
FP	GP								
73	71		P1_7	$\overline{INT5}$					D15
74	72		P1_6	$\overline{INT4}$					D14
75	73		P1_5	$\overline{INT3}$					D13
76	74		P1_4						D12
77	75		P1_3						D11
78	76		P1_2						D10
79	77		P1_1						D9
80	78		P1_0						D8
81	79		P0_7					AN0_7	D7
82	80		P0_6					AN0_6	D6
83	81		P0_5					AN0_5	D5
84	82		P0_4					AN0_4	D4
85	83		P0_3					AN0_3	D3
86	84		P0_2					AN0_2	D2
87	85		P0_1					AN0_1	D1
88	86		P0_0					AN0_0	D0
89	87		P10_7	$\overline{KI3}$	RTP3_3			AN_7	
90	88		P10_6	$\overline{KI2}$	RTP3_2			AN_6	
91	89		P10_5	$\overline{KI1}$	RTP3_1			AN_5	
92	90		P10_4	$\overline{KI0}$	RTP3_0			AN_4	
93	91		P10_3		RTP1_3			AN_3	
94	92		P10_2		RTP1_2			AN_2	
95	93		P10_1		RTP1_1			AN_1	
96	94	AVSS							
97	95		P10_0		RTP1_0			AN_0	
98	96	VREF							
99	97	AVCC							
100	98		P9_7			RXD4/SCL4/STXD4		$\overline{ADTRG}$	

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers.
The register bank is comprised of eight registers (R0, R1, R2, R3, A0, A1, SB, and FB) out of 28 CPU registers. There are two sets of register banks.



NOTE:
1. These registers comprise a register bank.
There are two sets of register banks (register bank 0 and register bank 1).

Figure 2.1 CPU Register

Table 4.2 SFR Address Map (2/20)

Address	Register	Symbol	After Reset
0030h			
0031h			
0032h			
0033h			
0034h			
0035h			
0036h			
0037h			
0038h	Address Match Interrupt Register 6	RMAD6	000000h
0039h			
003Ah			
003Bh			
003Ch	Address Match Interrupt Register 7	RMAD7	000000h
003Dh			
003Eh			
003Fh			
0040h			
0041h			
0042h			
0043h			
0044h			
0045h			
0046h			
0047h			
0048h	External Space Wait Control Register 0	EWCR0	X0X0 0011b
0049h	External Space Wait Control Register 1	EWCR1	X0X0 0011b
004Ah	External Space Wait Control Register 2	EWCR2	X0X0 0011b
004Bh	External Space Wait Control Register 3	EWCR3	X0X0 0011b
004Ch			
004Dh			
004Eh			
004Fh			
0050h			
0051h			
0052h			
0053h			
0054h			
0055h	Flash Memory Control Register 1	FMR1	0000 0X0Xb
0056h			
0057h	Flash Memory Control Register 0	FMR0	0000 0001b(Flash Memory) XXXX XXX0b(Mask ROM)
0058h			
0059h			
005Ah			
005Bh			
005Ch			
005Dh			
005Eh			
005Fh			

X: Undefined
Blank spaces are all reserved. No access is allowed.

Table 4.9 SFR Address Map (9/20)

Address	Register[2][3]	Symbol	After Reset
01F0h	CAN0 Message Slot Buffer 1 Standard ID0	C0SLOT1_0	XXh
01F1h	CAN0 Message Slot Buffer 1 Standard ID1	C0SLOT1_1	XXh
01F2h	CAN0 Message Slot Buffer 1 Extended ID0	C0SLOT1_2	XXh
01F3h	CAN0 Message Slot Buffer 1 Extended ID1	C0SLOT1_3	XXh
01F4h	CAN0 Message Slot Buffer 1 Extended ID2	C0SLOT1_4	XXh
01F5h	CAN0 Message Slot Buffer 1 Data Length Code	C0SLOT1_5	XXh
01F6h	CAN0 Message Slot Buffer 1 Data 0	C0SLOT1_6	XXh
01F7h	CAN0 Message Slot Buffer 1 Data 1	C0SLOT1_7	XXh
01F8h	CAN0 Message Slot Buffer 1 Data 2	C0SLOT1_8	XXh
01F9h	CAN0 Message Slot Buffer 1 Data 3	C0SLOT1_9	XXh
01FAh	CAN0 Message Slot Buffer 1 Data 4	C0SLOT1_10	XXh
01FBh	CAN0 Message Slot Buffer 1 Data 5	C0SLOT1_11	XXh
01FCh	CAN0 Message Slot Buffer 1 Data 6	C0SLOT1_12	XXh
01FDh	CAN0 Message Slot Buffer 1 Data 7	C0SLOT1_13	XXh
01FEh	CAN0 Message Slot Buffer 1 Time Stamp High-Order	C0SLOT1_14	XXh
01FFh	CAN0 Message Slot Buffer 1 Time Stamp Low-Order	C0SLOT1_15	XXh
0200h	CAN0 Control Register 0	C0CTLR0	XX01 0X01b[1]
0201h			XXXX 0000b[1]
0202h	CAN0 Status Register	C0STR	0000 0000b[1]
0203h			X000 0X01b[1]
0204h	CAN0 Extended ID Register	C0IDR	0000h[1]
0205h			
0206h	CAN0 Configuration Register	C0CONR	0000 XXXXb[1]
0207h			0000 0000b[1]
0208h	CAN0 Time Stamp Register	C0TSR	0000h[1]
0209h			
020Ah	CAN0 Transmit Error Count Register	C0TEC	00h[1]
020Bh	CAN0 Receive Error Count Register	C0REC	00h[1]
020Ch	CAN0 Slot Interrupt Status Register	C0SISTR	0000h[1]
020Dh			
020Eh			
020Fh			
0210h	CAN0 Slot Interrupt Mask Register	C0SIMKR	0000h[1]
0211h			
0212h			
0213h			
0214h	CAN0 Error Interrupt Mask Register	C0EIMKR	XXXX X000b[1]
0215h	CAN0 Error Interrupt Status Register	C0EISTR	XXXX X000b[1]
0216h	CAN0 Error Source Register	C0EFR	00h[1]
0217h	CAN0 Baud Rate Prescaler	C0BRP	0000 0001b[1]
0218h			
0219h	CAN0 Mode Register	C0MDR	XXXX XX00b[1]
021Ah			
021Bh			
021Ch			
021Dh			
021Eh			
021Fh			

X: Undefined
Blank spaces are all reserved. No access is allowed.
NOTES:
1. Values are obtained by setting the SLEEP bit in the C0SLPR register to “1” (sleep mode exited) after reset and supplying a clock to the CAN module.
2. The CAN-associated registers (allocated in addresses 01E0h to 02BFh) cannot be used in M32C/87B. In M32C/87A, only CAN0-associated registers can be used.
3. Set the PM13 bit in the PM1 register to 1 (2 wait states for SFR area) before accessing the CAN-associated registers.

Table 4.20 SFR Address Map (20/20)

Address	Register	Symbol	After Reset
03D0h	Port P14 Register(1)	P14	XXh
03D1h	Port P15 Register(1)	P15	XXh
03D2h	Port P14 Direction Register(1)(2)	PD14	X000 0000b
03D3h	Port P15 Direction Register(1)(2)	PD15	00h
03D4h			
03D5h			
03D6h			
03D7h			
03D8h			
03D9h			
03DAh	Pull-Up Control Register 2	PUR2	00h
03DBh	Pull-Up Control Register 3	PUR3	00h
03DCh	Pull-Up Control Register 4(1)(3)	PUR4	XXXX 0000b
03DDh			
03DEh			
03DFh			
03E0h	Port P0 Register	P0	XXh
03E1h	Port P1 Register	P1	XXh
03E2h	Port P0 Direction Register	PD0	00h
03E3h	Port P1 Direction Register	PD1	00h
03E4h	Port P2 Register	P2	XXh
03E5h	Port P3 Register	P3	XXh
03E6h	Port P2 Direction Register	PD2	00h
03E7h	Port P3 Direction Register	PD3	00h
03E8h	Port P4 Register	P4	XXh
03E9h	Port P5 Register	P5	XXh
03EAh	Port P4 Direction Register	PD4	00h
03EBh	Port P5 Direction Register	PD5	00h
03ECh			
03EDh			
03EEh			
03EFh			
03F0h	Pull-Up Control Register 0	PUR0	00h
03F1h	Pull-Up Control Register 1	PUR1	XXXX 0000b
03F2h			
03F3h			
03F4h			
03F5h			
03F6h			
03F7h			
03F8h			
03F9h			
03FAh			
03FBh			
03FCh			
03FDh			
03FEh			
03FFh	Port Control Register	PCR	XXXX X000b

X: Undefined
Blank spaces are all reserved. No access is allowed.
NOTES:
1. These registers cannot be used in the 100-pin package.
2. Set to FFh in the 100-pin package.
3. Set to 00h in the 100-pin package.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter		Condition	Value	Unit
VCC1, VCC2	Supply voltage		VCC1 = AVCC	-0.3 to 6.0	V
VCC2	Supply voltage		–	-0.3 to VCC1 + 0.1	V
AVCC	Analog supply voltage		VCC1 = AVCC	-0.3 to 6.0	V
VI	Input voltage	$\overline{\text{RESET}}$, CNVSS, BYTE, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P14_0 to P14_6, P15_0 to P15_7(1), VREF, XIN		-0.3 to VCC1 + 0.3	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7(1)		-0.3 to VCC2 + 0.3	
		P7_0, P7_1		-0.3 to 6.0	
VO	Output voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P14_0 to 14_6, P15_0 to P15_7(1), XOUT		-0.3 to VCC1 + 0.3	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7(1)		-0.3 to VCC2 + 0.3	
		P7_0, P7_1		-0.3 to 6.0	
Pd	Power consumption		-40°C≤Topr≤85°C	500	mW
Topr	Operating ambient temperature	during CPU operation		-20 to 85/ -40 to 85(2)	°C
		during programming or erasing Flash memory		0 to 60	°C
Tstg	Storage temperature			-65 to 150	°C

NOTES:
1. P11 to P15 are provided in the 144-pin package only.
2. Contact a Renesas sales office if temperature range of -40 to 85°C is required.

Table 5.4 Recommended Operating Conditions (3/3)
(VCC1 = VCC2 = 3.0 to 5.5 V, Topr = -20 to 85°C unless otherwise specified)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
f(CPU)	CPU clock frequency (same frequency as f(BCLK))	VCC1 = 4.2 to 5.5V	0		32	MHz
		VCC1 = 3.0 to 5.5V	0		24	MHz
f(XIN)	Main clock input oscillation frequency	VCC1 = 4.2 to 5.5V	0		32	MHz
		VCC1 = 3.0 to 5.5V	0		24	MHz
f(XCIN)	Sub clock frequency			32.768	50	kHz
f(Ring)	On-chip oscillator frequency			1		MHz
f(VCO)	VCO clock frequency (PLL frequency synthesizer)		20		80	MHz
f(PLL)	PLL clock frequency	VCC1 = 4.2 to 5.5V	10		32	MHz
		VCC1 = 3.0 to 5.5V	10		24	MHz
tsu(PLL)	Wait time to stabilize PLL frequency synthesizer	VCC1 = 5.0V			5	ms
		VCC1 = 3.3V			10	ms

VCC1 = VCC2 = 5V

Timing Requirements
(VCC1 = VCC2 = 4.2 to 5.5 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.18 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(UP)	TAiOUT input cycle time	2000		ns
tw(UPH)	TAiOUT input high (“H”) pulse width	1000		ns
tw(UPL)	TAiOUT input low (“L”) pulse width	1000		ns
tsu(UP-TIN)	TAiOUT input setup time	400		ns
th(TIN-UP)	TAiOUT input hold time	400		ns

i = 0 to 4

Table 5.19 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	800		ns
tsu(TAIN-TAOUT)	TAiOUT input setup time	200		ns
tsu(TAOUT-TAIN)	TAiIN input setup time	200		ns

i = 0 to 4

Table 5.20 Timer B Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TB)	TBiIN input cycle time (counted on one edge)	100		ns
tw(TBH)	TBiIN input high (“H”) pulse width (counted on one edge)	40		ns
tw(TBL)	TBiIN input low (“L”) pulse width (counted on one edge)	40		ns
tc(TB)	TBiIN input cycle time (counted on both edges)	200		ns
tw(TBH)	TBiIN input high (“H”) pulse width (counted on both edges)	80		ns
tw(TBL)	TBiIN input low (“L”) pulse width (counted on both edges)	80		ns

i = 0 to 5

Table 5.21 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TB)	TBiIN input cycle time	400		ns
tw(TBH)	TBiIN input high (“H”) pulse width	200		ns
tw(TBL)	TBiIN input low (“L”) pulse width	200		ns

i = 0 to 5

Table 5.22 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TB)	TBiIN input cycle time	400		ns
tw(TBH)	TBiIN input high (“H”) pulse width	200		ns
tw(TBL)	TBiIN input low (“L”) pulse width	200		ns

i = 0 to 5

VCC1 = VCC2 = 5V

Timing Requirements
(VCC1 = VCC2 = 4.2 to 5.5 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.27 External Interrupt $\overline{INTi}$ Input (Edge Sensitive)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tw(INH)	$\overline{INTi}$ input high (“H”) pulse width	250		ns
tw(INL)	$\overline{INTi}$ input low (“L”) pulse width	250		ns

i = 0 to 8(1)

NOTE:
1. $\overline{INT6}$ to $\overline{INT8}$ are provided in the 144-pin package only.

VCC1 = VCC2 = 5V

Timing Requirements
(VCC1 = VCC2 = 4.2 to 5.5 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.28 Memory Expansion mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tac1(RD-DB)	Data input access time (RD standard)		(note 1)	ns
tac1(AD-DB)	Data input access time (AD standard, CS standard)		(note 1)	ns
tac2(RD-DB)	Data input access time (RD standard, when accessing a space with the multiplexed bus)		(note 1)	ns
tac2(AD-DB)	Data input access time (AD standard, when accessing a space with the multiplexed bus)		(note 1)	ns
tsu(DB-BCLK)	Data input setup time	26		ns
tsu(RDY-BCLK)	$\overline{\text{RDY}}$ input setup time	26		ns
tsu(HOLD-BCLK)	$\overline{\text{HOLD}}$ input setup time	30		ns
th(RD-DB)	Data input hold time	0		ns
th(BCLK-RDY)	$\overline{\text{RDY}}$ input hold time	0		ns
th(BCLK-HOLD)	$\overline{\text{HOLD}}$ input hold time	0		ns
td(BCLK-HLDA)	$\overline{\text{HLDA}}$ output delay time		25	ns

NOTE:
1. Values, which depend on BCLK frequency and external bus cycles, can be obtained from the following equations. Insert wait states or lower the operation frequency, f(BCLK), if the calculated value is negative.

$$\text{tac1(RD-DB)} = \frac{10^9 \times m}{f(BCLK) \times 2} - 35\ [ns]$$ (if external bus cycle is $a\phi + b\phi$, $m = (b \times 2) + 1$)

$$\text{tac1(AD-DB)} = \frac{10^9 \times n}{f(BCLK)} - 35\ [ns]$$ (if external bus cycle is $a\phi + b\phi$, $n = a + b$)

$$\text{tac2(RD-DB)} = \frac{10^9 \times m}{f(BCLK) \times 2} - 35\ [ns]$$ (if external bus cycle is $a\phi + b\phi$, $m = (b \times 2) - 1$)

$$\text{tac2(AD-DB)} = \frac{10^9 \times p}{f(BCLK) \times 2} - 35\ [ns]$$ (if external bus cycle is $a\phi + b\phi$, $p = \{(a + b - 1) \times 2\} + 1$)

VCC1 = VCC2 = 3.3 V

Table 5.33 Electrical Characteristics (3/3)
(VCC1 = VCC2 = 3.3 V, VSS = 0 V, Topr = 25°C)

Symbol	Parameter	Measurement Condition(1)		Standard			Unit
				Min.	Typ.	Max.	
ICC	Power supply current	Flash memory version	f(CPU) = 24 MHz		23	33	mA
			f(CPU) = 16 MHz		17		mA
			f(CPU) = 8 MHz		11		mA
			f(CPU) = f(Ring) In on-chip oscillator low-power consumption mode		2.6		mA
			f(CPU) = 32 kHz In low-power consumption mode While flash memory is operating		430		µA
			f(CPU) = 32 kHz In low-power consumption mode While flash memory is stopped(2)		30		µA
			Wait mode: f(CPU) = f(Ring) After entering wait mode from on-chip oscillator low-power consumption mode		45		µA
			Stop mode (while clock is stopped)		0.8	5	µA
			Stop mode (while clock is stopped) Topr = 85°C			50	µA
		Mask ROM version	f(CPU) = 24 MHz		23	33	mA
			f(CPU) = 16 MHz		17		mA
			f(CPU) = 8 MHz		11		mA
			f(CPU) = f(Ring) In on-chip oscillator low-power consumption mode		1		mA
			f(CPU) = 32 kHz In low-power consumption mode		30		µA
			Wait mode: f(CPU) = f(Ring) After entering wait mode from on-chip oscillator low-power consumption mode		45		µA
			Stop mode (while clock is stopped)		0.8	5	µA
			Stop mode (while clock is stopped) Topr = 85°C			50	µA

NOTES:
1. In single-chip mode, leave the output pins open and connect the input pins to VSS.
2. Value is obtained when setting the FMSTP bit in the FMR0 register to 1 (flash memory stopped) and running the program on RAM.

VCC1 = VCC2 = 3.3 V

Table 5.34 A/D Conversion Characteristics (VCC1 = VCC2 = AVCC = VREF = 3.0 to 3.6 V, VSS = AVSS = 0 V, Topr = -20 to 85°C, f(CPU) = 24MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
–	Resolution	VREF = VCC1			10	Bits
INL	Integral nonlinearity error (8-bit)	VREF = VCC1 = VCC2 = 3.3 V			±2	LSB
DNL	Differential nonlinearity error (8-bit)				±1	LSB
–	Offset error (8-bit)				±2	LSB
–	Gain error (8-bit)				±2	LSB
RLADDER	Resistor ladder	VREF = VCC1	8		40	kΩ
tCONV	8-bit conversion time(1)(2)		4.9			µs
VREF	Reference voltage		3		VCC1	V
VIA	Analog input voltage		0		VREF	V

NOTES:
1. The value when ϕAD frequency is at 10 MHz. Keep ϕAD frequency at 10 MHz or lower. If f(CPU) (=fAD) is 24 MHz, divide f(CPU) by 3 to make it 8 MHz. The conversion time in this case is 6.1 µs.
2. Sample and hold function is not available.

Table 5.35 D/A Conversion Characteristics (VCC1 = VCC2 = VREF = 3.0 to 3.6 V, VSS = AVSS = 0 V, Topr = -20 to 85°C, f(CPU) = 24MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
–	Resolution				8	Bits
–	Absolute accuracy				1.0	%
tsu	Setup time				3	µs
RO	Output resistance		4	10	20	kΩ
IVREF	Reference power supply input current	(note 1)			1.0	mA

NOTE:
1. Measurement when one D/A converter is used, and the DAi register (i = 0, 1) of the unused D/A converter is set to 00h. The current flown into the resistor ladder in the A/D converter is excluded. IVREF flows even if VCUT bit in the AD0CON1 register is set to 0 (VREF not connected)

VCC1 = VCC2 = 3.3 V

Timing Requirements
(VCC1 = VCC2 = 3.0 to 3.6 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.41 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(UP)	TAiOUT input cycle time	2000		ns
tw(UPH)	TAiOUT input high (“H”) pulse width	1000		ns
tw(UPL)	TAiOUT input low (“L”) pulse width	1000		ns
tsu(UP-TIN)	TAiOUT input setup time	400		ns
th(TIN-UP)	TAiOUT input hold time	400		ns

i = 0 to 4

Table 5.42 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	2		µs
tsu(TAIN-TAOUT)	TAiOUT input setup time	500		ns
tsu(TAOUT-TAIN)	TAiIN input setup time	500		ns

i = 0 to 4

Table 5.43 Timer B Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TB)	TBiIN input cycle time (counted on one edge)	100		ns
tw(TBH)	TBiIN input high (“H”) pulse width (counted on one edge)	40		ns
tw(TBL)	TBiIN input low (“L”) pulse width (counted on one edge)	40		ns
tc(TB)	TBiIN input cycle time (counted on both edges)	200		ns
tw(TBH)	TBiIN input high (“H”) pulse width (counted on both edges)	80		ns
tw(TBL)	TBiIN input low (“L”) pulse width (counted on both edges)	80		ns

i = 0 to 5

Table 5.44 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TB)	TBiIN input cycle time	400		ns
tw(TBH)	TBiIN input high (“H”) pulse width	200		ns
tw(TBL)	TBiIN input low (“L”) pulse width	200		ns

i = 0 to 5

Table 5.45 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TB)	TBiIN input cycle time	400		ns
tw(TBH)	TBiIN input high (“H”) pulse width	200		ns
tw(TBL)	TBiIN input low (“L”) pulse width	200		ns

i = 0 to 5

VCC1 = VCC2 = 3.3 V

Timing Requirements
(VCC1 = VCC2 = 3.0 to 3.6 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.50 External Interrupt $\overline{INTi}$ Input (Edge Sensitive)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tw(INH)	$\overline{INTi}$ input high (“H”) pulse width	250		ns
tw(INL)	$\overline{INTi}$ input low (“L”) pulse width	250		ns

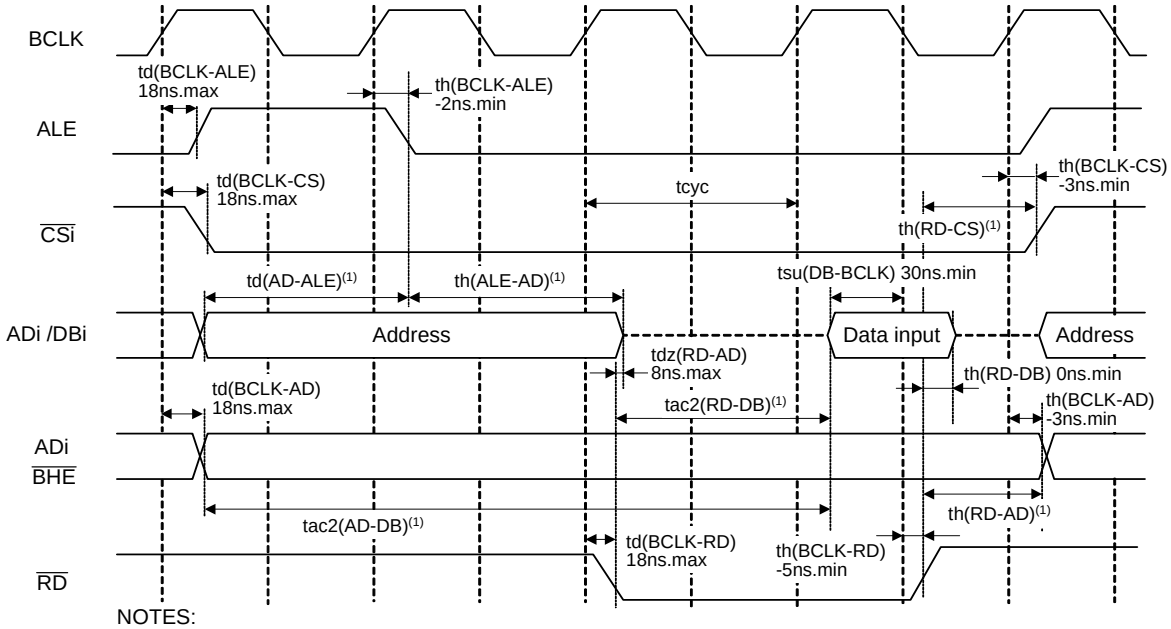
i = 0 to 8(1)

NOTE:
1. $\overline{INT6}$ to $\overline{INT8}$ are provided in the 144-pin package only.

Memory Expansion Mode and Microprocessor Mode
(when accessing an external memory space with the multiplexed bus)

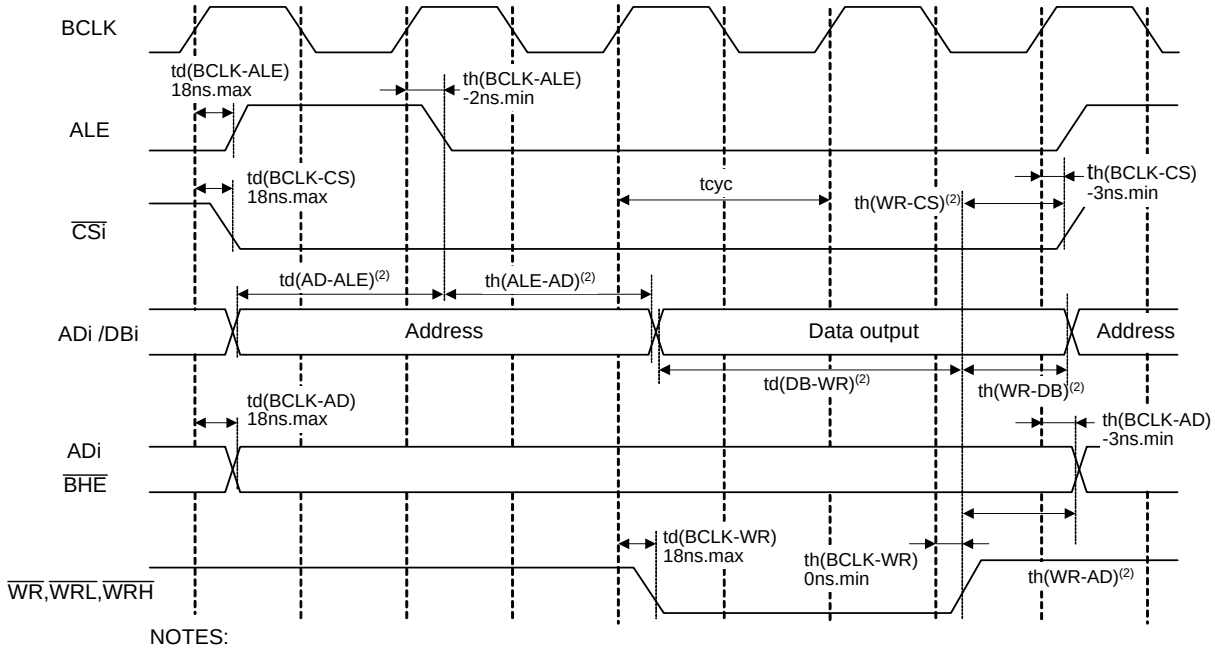
VCC1=VCC2=3.3V

Read Timing (2ϕ + 2ϕ Bus Cycle)



NOTES:
1. Varies with operation frequency:
td(AD-ALE) = (tcyc / 2 x n - 20) ns.min (if external bus cycle aϕ + bϕ, n = a)
th(ALE-AD) = (tcyc / 2 x n - 20) ns.min (if external bus cycle aϕ + bϕ, n = a)
th(RD-AD) = (tcyc / 2 - 10) ns.min, th(RD-CS) = (tcyc / 2 - 10) ns.min
tac2(RD-DB) = (tcyc / 2 x m - 35) ns.max (if external bus cycle aϕ + bϕ, m = (b x 2) - 1)
tac2(AD-DB) = (tcyc / 2 x p - 35) ns.max (if external bus cycle aϕ + bϕ, p = {(a + b - 1) x 2} + 1)

Write Timing (2ϕ + 2ϕ Bus Cycle)



NOTES:
1. Varies with operation frequency:
td(AD-ALE) = (tcyc / 2 x n - 20) ns.min (if external bus cycle aϕ + bϕ, n = a)
th(ALE-AD) = (tcyc / 2 x n - 20) ns.min (if external bus cycle aϕ + bϕ, n = a)
th(WR-AD) = (tcyc / 2 - 15) ns.min, th(WR-CS) = (tcyc / 2 - 10) ns.min
th(WR-DB) = (tcyc / 2 - 20) ns.min
td(DB-WR) = (tcyc / 2 x m - 25) ns.min (if external bus cycle aϕ + bϕ, m = (b x 2) - 1)

$$tcyc = \frac{10^9}{f(BCLK)}$$

Measurement Conditions:
- VCC1 = VCC2 = 3.0 to 3.6 V
- Input high and low voltage VIH = 1.5 V, VIL = 0.5 V
- Output high and low voltage VOH = 1.5 V, VOL = 1.5 V

Figure 5.10 VCC1 = VCC2 = 3.3 V Timing Diagram (4/4)

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