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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M32C/80
Core Size	16/32-Bit
Speed	32MHz
Connectivity	EBI/EMI, I²C, IEBus, IrDA, SIO, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	121
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 34x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m3087bfkbgp-u5

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Table 1.10 144-Pin Package List of Pin Names (3/4)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
81		P3_5						A13,[A13/D13]
82		P3_4						A12,[A12/D12]
83		P3_3						A11,[A11/D11]
84		P3_2						A10,[A10/D10]
85		P3_1						A9,[A9/D9]
86		P12_4						
87		P12_3			$\overline{\text{CTS6}}$/$\overline{\text{RTS6}}$			
88		P12_2			RXD6			
89		P12_1			CLK6			
90		P12_0			TXD6			
91	VCC2							
92		P3_0						A8,[A8/D8]
93	VSS							
94		P2_7					AN2_7	A7,[A7/D7]
95		P2_6					AN2_6	A6,[A6/D6]
96		P2_5					AN2_5	A5,[A5/D5]
97		P2_4					AN2_4	A4,[A4/D4]
98		P2_3					AN2_3	A3,[A3/D3]
99		P2_2					AN2_2	A2,[A2/D2]
100		P2_1					AN2_1	A1,[A1/D1]
101		P2_0					AN2_0	A0,[A0/D0]
102		P1_7	$\overline{\text{INT5}}$					D15
103		P1_6	$\overline{\text{INT4}}$					D14
104		P1_5	$\overline{\text{INT3}}$					D13
105		P1_4						D12
106		P1_3						D11
107		P1_2						D10
108		P1_1						D9
109		P1_0						D8
110		P0_7					AN0_7	D7
111		P0_6					AN0_6	D6
112		P0_5					AN0_5	D5
113		P0_4					AN0_4	D4
114		P11_4						
115		P11_3				INPC1_3/OUTC1_3		
116		P11_2				INPC1_2/OUTC1_2/ ISRXD1		
117		P11_1				INPC1_1/OUTC1_1/ ISCLK1		
118		P11_0				INPC1_0/OUTC1_0/ ISTXD1		
119		P0_3					AN0_3	D3
120		P0_2					AN0_2	D2

Table 1.14 100-Pin Package List of Pin Names (3/3)

Pin No.		Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
FP	GP								
73	71		P1_7	$\overline{INT5}$					D15
74	72		P1_6	$\overline{INT4}$					D14
75	73		P1_5	$\overline{INT3}$					D13
76	74		P1_4						D12
77	75		P1_3						D11
78	76		P1_2						D10
79	77		P1_1						D9
80	78		P1_0						D8
81	79		P0_7					AN0_7	D7
82	80		P0_6					AN0_6	D6
83	81		P0_5					AN0_5	D5
84	82		P0_4					AN0_4	D4
85	83		P0_3					AN0_3	D3
86	84		P0_2					AN0_2	D2
87	85		P0_1					AN0_1	D1
88	86		P0_0					AN0_0	D0
89	87		P10_7	$\overline{KI3}$	RTP3_3			AN_7	
90	88		P10_6	$\overline{KI2}$	RTP3_2			AN_6	
91	89		P10_5	$\overline{KI1}$	RTP3_1			AN_5	
92	90		P10_4	$\overline{KI0}$	RTP3_0			AN_4	
93	91		P10_3		RTP1_3			AN_3	
94	92		P10_2		RTP1_2			AN_2	
95	93		P10_1		RTP1_1			AN_1	
96	94	AVSS							
97	95		P10_0		RTP1_0			AN_0	
98	96	VREF							
99	97	AVCC							
100	98		P9_7			RXD4/SCL4/STXD4		$\overline{ADTRG}$	

Table 1.17 Pin Functions (100-Pin and 144-Pin Package) (3/4)

Type	Symbol	I/O Type	Supply Voltage	Description
Intelligent I/O	INPC1_0 to INPC1_3	I	VCC1/ VCC2(1)	Input pins for the time measurement function.
	INPC1_4 to INPC1_7	I	VCC1	
	OUTC1_0 to OUTC1_3	O	VCC1/ VCC2(1)	Output pins for the waveform generation function. (OUTC1_6/OUTC2_0 and OUTC1_7/OUTC2_2 assigned to ports 7_0 and 7_1 are N-channel open drain output.)
	OUTC1_4 to OUTC1_7	O	VCC1	
	OUTC2_0 to OUTC2_2	O	VCC1/ VCC2(1)	
	ISCLK0	I/O	VCC1	Clock input/output pins for the intelligent I/O communication function.
	ISCLK1, ISCLK2	I/O	VCC1/ VCC2(1)	
	ISRXD0	I	VCC1	Data input pins for the intelligent I/O communication function.
	ISRXD1, ISRXD2	I	VCC1/ VCC2(1)	
	ISTXD0	O	VCC1	Data output pins for the intelligent I/O communication function. (ISTXD2 assigned to port 7_0 is N-channel open drain output.)
	ISTXD1, ISTXD2	O	VCC1/ VCC2(1)	
	IEIN	I	VCC1/ VCC2(1)	Data input pin for the intelligent I/O communication function.
	IEOUT	O	VCC1/ VCC2(1)	Data output pin for the intelligent I/O communication function. (IEOUT assigned to port 7_0 is N-channel open drain output.)
Reference voltage input	VREF	I	–	The VREF pin supplies the reference voltage to the A/D converter and D/A converter.
A/D converter	AN_0 to AN_7	I	VCC1	Analog input pins for the A/D converter.
	AN0_0 to AN0_7, AN2_0 to AN2_7	I	VCC2	
	$\overline{\text{ADTRG}}$	I	VCC1	External trigger input pin for the A/D converter.
	ANEX0	I/O	VCC1	Extended analog input pin for the A/D converter or output pin in external op-amp connection mode.
	ANEX1	I	VCC1	Extended analog input pin for the A/D converter.
D/A converter	DA0, DA1	O	VCC1	Output pins for the D/A converter.
Real-time port	RTP0_0 to RTP0_3 RTP1_0 to RTP1_3 RTP2_0 to RTP2_3 RTP3_0 to RTP3_3	O	VCC1	These pins function as real-time ports. (RTP0_2 and RTP0_3 are N-channel open drain output.)

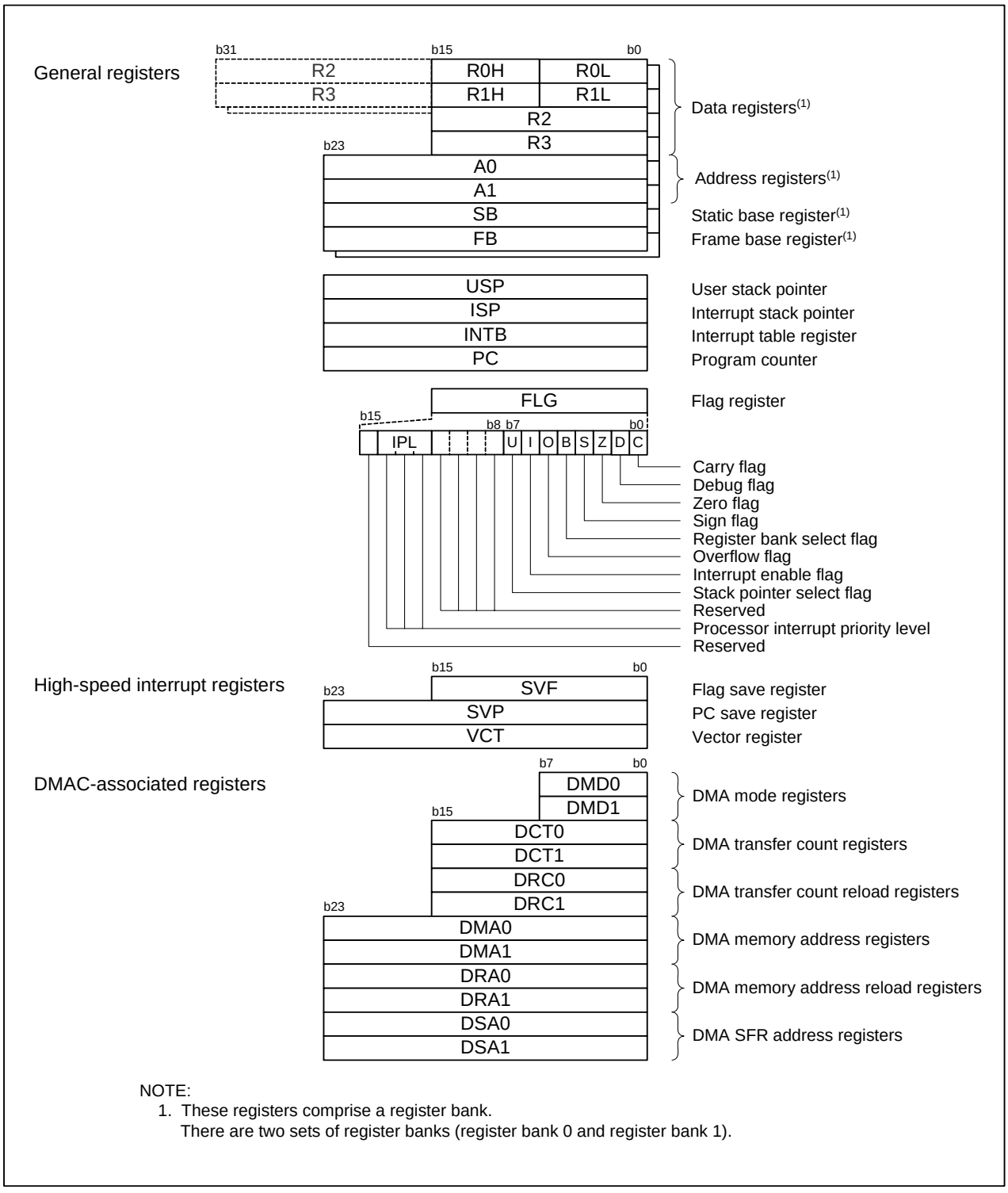
I: Input O: Output I/O: Input and output

NOTE:

1. Only VCC1 can be used in the 100-pin package.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers.
The register bank is comprised of eight registers (R0, R1, R2, R3, A0, A1, SB, and FB) out of 28 CPU registers. There are two sets of register banks.



NOTE:
1. These registers comprise a register bank.
There are two sets of register banks (register bank 0 and register bank 1).

Figure 2.1 CPU Register

Table 4.6 SFR Address Map (6/20)

Address	Register	Symbol	After Reset
011Ah	Group 1 Time Measurement Control Register 2	G1TMCR2	00h
011Bh	Group 1 Time Measurement Control Register 3	G1TMCR3	00h
011Ch	Group 1 Time Measurement Control Register 4	G1TMCR4	00h
011Dh	Group 1 Time Measurement Control Register 5	G1TMCR5	00h
011Eh	Group 1 Time Measurement Control Register 6	G1TMCR6	00h
011Fh	Group 1 Time Measurement Control Register 7	G1TMCR7	00h
0120h 0121h	Group 1 Base Timer Register	G1BT	XXXXh
0122h	Group 1 Base Timer Control Register 0	G1BCR0	00h
0123h	Group 1 Base Timer Control Register 1	G1BCR1	X000 000Xb
0124h	Group 1 Time Measurement Prescaler Register 6	G1TPR6	00h
0125h	Group 1 Time Measurement Prescaler Register 7	G1TPR7	00h
0126h	Group 1 Function Enable Register	G1FE	00h
0127h	Group 1 Function Select Register	G1FS	00h
0128h 0129h	Group 1 SI/O Receive Buffer Register	G1RB	XXXX XXXXb X000 XXXXb
012Ah	Group 1 Transmit Buffer/Receive Data Register	G1TB/G1DR	XXh
012Bh			
012Ch	Group 1 Receive Input Register	G1RI	XXh
012Dh	Group 1 SI/O Communication Mode Register	G1MR	00h
012Eh	Group 1 Transmit Output Register	G1TO	XXh
012Fh	Group 1 SI/O Communication Control Register	G1CR	0000 X011b
0130h	Group 1 Data Compare Register 0	G1CMP0	XXh
0131h	Group 1 Data Compare Register 1	G1CMP1	XXh
0132h	Group 1 Data Compare Register 2	G1CMP2	XXh
0133h	Group 1 Data Compare Register 3	G1CMP3	XXh
0134h	Group 1 Data Mask Register 0	G1MSK0	XXh
0135h	Group 1 Data Mask Register 1	G1MSK1	XXh
0136h			
0137h			
0138h 0139h	Group 1 Receive CRC Code Register	G1RCRC	XXXXh
013Ah 013Bh	Group 1 Transmit CRC Code Register	G1TCRC	0000h
013Ch	Group 1 SI/O Expansion Mode Register	G1EMR	00h
013Dh	Group 1 SI/O Extended Receive Control Register	G1ERC	00h
013Eh	Group 1 SI/O Special Communication Interrupt Detection Register	G1IRF	0000 XXXXb
013Fh	Group 1 SI/O Extended Transmit Control Register	G1ETC	0000 0XXXb
0140h 0141h	Group 2 Waveform Generation Register 0	G2PO0	XXXXh
0142h 0143h	Group 2 Waveform Generation Register 1	G2PO1	XXXXh
0144h 0145h	Group 2 Waveform Generation Register 2	G2PO2	XXXXh
0146h 0147h	Group 2 Waveform Generation Register 3	G2PO3	XXXXh
0148h 0149h	Group 2 Waveform Generation Register 4	G2PO4	XXXXh
014Ah 014Bh	Group 2 Waveform Generation Register 5	G2PO5	XXXXh
014Ch 014Dh	Group 2 Waveform Generation Register 6	G2PO6	XXXXh
014Eh 014Fh	Group 2 Waveform Generation Register 7	G2PO7	XXXXh

X: Undefined
Blank spaces are all reserved. No access is allowed.

Table 4.10 SFR Address Map (10/20)

Address	Register[3][4]	Symbol	After Reset
0220h	CAN0 Single Shot Control Register	C0SSCTLR	0000h[1][2]
0221h			
0222h			
0223h			
0224h	CAN0 Single Shot Status Register	C0SSSTR	0000h[1][2]
0225h			
0226h			
0227h			
0228h	CAN0 Global Mask Register Standard ID0	C0GMR0	XXX0 0000b[1][2]
0229h	CAN0 Global Mask Register Standard ID1	C0GMR1	XX00 0000b[1][2]
022Ah	CAN0 Global Mask Register Extended ID0	C0GMR2	XXXX 0000b[1][2]
022Bh	CAN0 Global Mask Register Extended ID1	C0GMR3	00h[1][2]
022Ch	CAN0 Global Mask Register Extended ID2	C0GMR4	XX00 0000b[1][2]
022Dh			
022Eh			
022Fh			
0230h	CAN0 Message Slot 0 Control Register / CAN0 Local Mask Register A Standard ID0	C0MCTL0 / C0LMAR0	0000 0000b[1][2]/ XXX0 0000b[1][2]
0231h	CAN0 Message Slot 1 Control Register / CAN0 Local Mask Register A Standard ID1	C0MCTL1 / C0LMAR1	0000 0000b[1][2]/ XX00 0000b[1][2]
0232h	CAN0 Message Slot 2 Control Register / CAN0 Local Mask Register A Extended ID0	C0MCTL2 / C0LMAR2	0000 0000b[1][2]/ XXXX 0000b[1][2]
0233h	CAN0 Message Slot 3 Control Register / CAN0 Local Mask Register A Extended ID1	C0MCTL3 / C0LMAR3	00h[1][2]/ 00h[1][2]
0234h	CAN0 Message Slot 4 Control Register / CAN0 Local Mask Register A Extended ID2	C0MCTL4 / C0LMAR4	0000 0000b[1][2]/ XX00 0000b[1][2]
0235h	CAN0 Message Slot 5 Control Register	C0MCTL5	00h[1][2]
0236h	CAN0 Message Slot 6 Control Register	C0MCTL6	00h[1][2]
0237h	CAN0 Message Slot 7 Control Register	C0MCTL7	00h[1][2]
0238h	CAN0 Message Slot 8 Control Register / CAN0 Local Mask Register B Standard ID0	C0MCTL8 / C0LMBR0	0000 0000b[1][2]/ XXX0 0000b[1][2]
0239h	CAN0 Message Slot 9 Control Register / CAN0 Local Mask Register B Standard ID1	C0MCTL9 / C0LMBR1	0000 0000b[1][2]/ XX00 0000b[1][2]
023Ah	CAN0 Message Slot 10 Control Register / CAN0 Local Mask Register B Extended ID0	C0MCTL10 / C0LMBR2	0000 0000b[1][2]/ XXXX 0000b[1][2]
023Bh	CAN0 Message Slot 11 Control Register / CAN0 Local Mask Register B Extended ID1	C0MCTL11 / C0LMBR3	00h[1][2]/ 00h[1][2]
023Ch	CAN0 Message Slot 12 Control Register / CAN0 Local Mask Register B Extended ID2	C0MCTL12 / C0LMBR4	0000 0000b[1][2]/ XX00 0000b[1][2]
023Dh	CAN0 Message Slot 13 Control Register	C0MCTL13	00h[1][2]
023Eh	CAN0 Message Slot 14 Control Register	C0MCTL14	00h[1][2]
023Fh	CAN0 Message Slot 15 Control Register	C0MCTL15	00h[1][2]
0240h	CAN0 Slot Buffer Select Register	C0SBS	00h[2]
0241h	CAN0 Control Register 1	C0CTLR1	X000 00XXb[2]
0242h	CAN0 Sleep Control Register	C0SLPR	XXXX XXX0b
0243h			
0244h	CAN0 Acceptance Filter Support Register	C0AFS	0000 0000b[2]
0245h			0000 0001b[2]
0246h			
0247h			
0248h			
0249h			
024Ah to 024Fh			

X: Undefined
Blank spaces are all reserved. No access is allowed.
NOTES:

1. The BANKSEL bit in the C0CTLR1 register can switch functions for addresses 0220h to 023Fh.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to “1” (sleep mode exited) after reset and supplying a clock to the CAN module.
3. The CAN-associated registers (allocated in addresses 01E0h to 02BFh) cannot be used in M32C/87B. In M32C/87A, only CAN0-associated registers can be used.
4. Set the PM13 bit in the PM1 register to 1 (2 wait states for SFR area) before accessing the CAN-associated registers.

Table 4.11 SFR Address Map (11/20)

Address	Register[2][3]	Symbol	After Reset
0250h	CAN1 Slot Buffer Select Register	C1SBS	00h[1]
0251h	CAN1 Control Register 1	C1CTLR1	X000 00XXb[1]
0252h	CAN1 Sleep Control Register	C1SLPR	XXXX XXX0b[1]
0253h			
0254h	CAN1 Acceptance Filter Support Register	C1AFS	0000 0000b[1]
0255h			0000 0001b[1]
0256h			
0257h			
0258h			
0259h			
025Ah			
025Bh			
025Ch			
025Dh			
025Eh			
025Fh			
0260h	CAN1 Message Slot Buffer 0 Standard ID0	C1SLOT0_0	XXh
0261h	CAN1 Message Slot Buffer 0 Standard ID1	C1SLOT0_1	XXh
0262h	CAN1 Message Slot Buffer 0 Extended ID0	C1SLOT0_2	XXh
0263h	CAN1 Message Slot Buffer 0 Extended ID1	C1SLOT0_3	XXh
0264h	CAN1 Message Slot Buffer 0 Extended ID2	C1SLOT0_4	XXh
0265h	CAN1 Message Slot Buffer 0 Data Length Code	C1SLOT0_5	XXh
0266h	CAN1 Message Slot Buffer 0 Data 0	C1SLOT0_6	XXh
0267h	CAN1 Message Slot Buffer 0 Data 1	C1SLOT0_7	XXh
0268h	CAN1 Message Slot Buffer 0 Data 2	C1SLOT0_8	XXh
0269h	CAN1 Message Slot Buffer 0 Data 3	C1SLOT0_9	XXh
026Ah	CAN1 Message Slot Buffer 0 Data 4	C1SLOT0_10	XXh
026Bh	CAN1 Message Slot Buffer 0 Data 5	C1SLOT0_11	XXh
026Ch	CAN1 Message Slot Buffer 0 Data 6	C1SLOT0_12	XXh
026Dh	CAN1 Message Slot Buffer 0 Data 7	C1SLOT0_13	XXh
026Eh	CAN1 Message Slot Buffer 0 Time Stamp High-Order	C1SLOT0_14	XXh
026Fh	CAN1 Message Slot Buffer 0 Time Stamp Low-Order	C1SLOT0_15	XXh
0270h	CAN1 Message Slot Buffer 1 Standard ID0	C1SLOT1_0	XXh
0271h	CAN1 Message Slot Buffer 1 Standard ID1	C1SLOT1_1	XXh
0272h	CAN1 Message Slot Buffer 1 Extended ID0	C1SLOT1_2	XXh
0273h	CAN1 Message Slot Buffer 1 Extended ID1	C1SLOT1_3	XXh
0274h	CAN1 Message Slot Buffer 1 Extended ID2	C1SLOT1_4	XXh
0275h	CAN1 Message Slot Buffer 1 Data Length Code	C1SLOT1_5	XXh
0276h	CAN1 Message Slot Buffer 1 Data 0	C1SLOT1_6	XXh
0277h	CAN1 Message Slot Buffer 1 Data 1	C1SLOT1_7	XXh
0278h	CAN1 Message Slot Buffer 1 Data 2	C1SLOT1_8	XXh
0279h	CAN1 Message Slot Buffer 1 Data 3	C1SLOT1_9	XXh
027Ah	CAN1 Message Slot Buffer 1 Data 4	C1SLOT1_10	XXh
027Bh	CAN1 Message Slot Buffer 1 Data 5	C1SLOT1_11	XXh
027Ch	CAN1 Message Slot Buffer 1 Data 6	C1SLOT1_12	XXh
027Dh	CAN1 Message Slot Buffer 1 Data 7	C1SLOT1_13	XXh
027Eh	CAN1 Message Slot Buffer 1 Time Stamp High-Order	C1SLOT1_14	XXh
027Fh	CAN1 Message Slot Buffer 1 Time Stamp Low-Order	C1SLOT1_15	XXh

X: Undefined
Blank spaces are all reserved. No access is allowed.
NOTES:
1. Values are obtained by setting the SLEEP bit in the C1SLPR register to “1” (sleep mode exited) after reset and supplying a clock to the CAN module.
2. The CAN-associated registers (allocated in addresses 01E0h to 02BFh) cannot be used in M32C/87B. In M32C/87A, only CAN0-associated registers can be used.
3. Set the PM13 bit in the PM1 register to 1 (2 wait states for SFR area) before accessing the CAN-associated registers.

Table 4.17 SFR Address Map (17/20)

Address	Register	Symbol	After Reset
0350h	Timer B0 Register	TB0	XXXXh
0351h			
0352h	Timer B1 Register	TB1	XXXXh
0353h			
0354h	Timer B2 Register	TB2	XXXXh
0355h			
0356h	Timer A0 Mode Register	TA0MR	00h
0357h	Timer A1 Mode Register	TA1MR	00h
0358h	Timer A2 Mode Register	TA2MR	00h
0359h	Timer A3 Mode Register	TA3MR	00h
035Ah	Timer A4 Mode Register	TA4MR	00h
035Bh	Timer B0 Mode Register	TB0MR	00XX 0000b
035Ch	Timer B1 Mode Register	TB1MR	00XX 0000b
035Dh	Timer B2 Mode Register	TB2MR	00XX 0000b
035Eh	Timer B2 Special Mode Register	TB2SC	XXXX XXX0b
035Fh	Count Source Prescaler Register(1)	TCSPR	0XXX 0000b
0360h			
0361h			
0362h			
0363h			
0364h	UART0 Special Mode Register 4	U0SMR4	00h
0365h	UART0 Special Mode Register 3	U0SMR3	00h
0366h	UART0 Special Mode Register 2	U0SMR2	00h
0367h	UART0 Special Mode Register	U0SMR	00h
0368h	UART0 Transmit/Receive Mode Register	U0MR	00h
0369h	UART0 Baud Rate Register	U0BRG	XXh
036Ah	UART0 Transmit Buffer Register	U0TB	XXXXh
036Bh			
036Ch	UART0 Transmit/Receive Control Register 0	U0C0	0000 1000b
036Dh	UART0 Transmit/Receive Control Register 1	U0C1	0000 0010b
036Eh	UART0 Receive Buffer Register	U0RB	XXXXh
036Fh			
0370h			
0371h			
0372h	IrDA Control Register	IRCON	X000 0000b
0373h			
0374h			
0375h			
0376h			
0377h			
0378h	DMA0 Request Source Select Register	DM0SL	0X00 0000b
0379h	DMA1 Request Source Select Register	DM1SL	0X00 0000b
037Ah	DMA2 Request Source Select Register	DM2SL	0X00 0000b
037Bh	DMA3 Request Source Select Register	DM3SL	0X00 0000b
037Ch	CRC Data Register	CRCD	XXXXh
037Dh			
037Eh	CRC Input Register	CRCIN	XXh
037Fh			

X: Undefined
Blank spaces are all reserved. No access is allowed.
NOTE:
1. The TCSPR register maintains values set before reset, even after software reset or watchdog timer reset has been performed.

VCC1 = VCC2 = 5V

Table 5.5 Electrical Characteristics (1/3)
(VCC1 = VCC2 = 4.2 to 5.5 V, VSS = 0 V, Topr = -20 to 85°C, f(CPU) = 32 MHz unless otherwise specified)

Symbol	Parameter		Measurement Condition	Standard			Unit
				Min.	Typ.	Max.	
VOH	Output high “H” voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7(1)	IOH = -5 mA	VCC2 - 2.0		VCC2	V
		P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7,P10_0 to P10_7, P14_0 to P14_6, P15_0 to P15_7(1)	IOH = -5 mA	VCC1 - 2.0		VCC1	
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7 P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7(1)	IOH = -200 µA	VCC2 - 0.3		VCC2	V
		P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7,P10_0 to P10_7, P14_0 to P14_6, P15_0 to P15_7(1)	IOH = -200 µA	VCC1 - 0.3		VCC1	
		XOUT	IOH = -1 mA	3.0		VCC1	V
		XCOUT Drive capability = high	No load applied		2.5		V
		XCOUT Drive capability = low	No load applied		1.6		V
VOL	Output low “L” voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7,P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7(1)	IOL = 5 mA			2.0	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7,P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7(1)	IOL = 200 µA			0.45	V
		XOUT	IOL = 1 mA			2.0	V
		XCOUT Drive capability = high	No load applied		0		V
		XCOUT Drive capability = low	No load applied		0		V
VT+ - VT-	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, TA0IN to TA4IN, $\overline{TB0IN}$ to $\overline{TB5IN}$, $\overline{INT0}$ to $\overline{INT8}$, $\overline{ADTRG}$, $\overline{CTS0}$ to $\overline{CTS6}$, CLK0 to $\overline{CLK6}$, TA0OUT to TA4OUT, $\overline{NMI}$, $\overline{KI0}$ to $\overline{KI3}$, RXD0 to RXD6, SCL0 to SCL4, SDA0 to SDA4, INPC1_0 to INPC1_7, ISCLK0 to ISCLK2, ISRXD0 to ISRXD2, IEIN, CAN0IN, CAN1IN, $\overline{CAN1WU}$		0.2		1.0	V
		$\overline{RESET}$		0.2		1.8	V

NOTE:
1. P11 to P15 are provided in the 144-pin package only.

VCC1 = VCC2 = 5V

Table 5.6 Electrical Characteristics (2/3)
(VCC1 = VCC2 = 4.2 to 5.5 V, VSS = 0 V, Topr = -20 to 85°C, f(CPU) = 32 MHz unless otherwise specified)

Symbol	Parameter		Measurement Condition	Standard			Unit
				Min.	Typ.	Max.	
IIH	Input high "H" current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7(1), XIN, $\overline{\text{RESET}}$, CNVSS, BYTE	VI = 5 V			5.0	µA
IIL	Input low "L" current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7(1), XIN, $\overline{\text{RESET}}$, CNVSS, BYTE	VI = 0V			-5.0	µA
RPULLUP	Pull-up resistance	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7,P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7(1)	VI = 0V	30	50	167	kΩ
RfXIN	Feedback resistance	XIN			1.5		MΩ
RfXCIN	Feedback resistance	XCIN			10		MΩ
VRAM	RAM data retention voltage	In stop mode		2.0			V

NOTE:
1. P11 to P15 are provided in the 144-pin package only.

VCC1 = VCC2 = 5V

Table 5.7 Electrical Characteristics (3/3)
(VCC1 = VCC2 = 5.5 V, VSS = 0 V, Topr = 25°C)

Symbol	Parameter	Measurement Condition(1)		Standard			Unit
				Min.	Typ.	Max.	
ICC	Power supply current	Flash memory version	f(CPU) = 32 MHz		32	45	mA
			f(CPU) = 16 MHz		19		mA
			f(CPU) = 8 MHz		12		mA
			f(CPU) = f(Ring) In on-chip oscillator low-power consumption mode		2.6		mA
			f(CPU) = 32 kHz In low-power consumption mode While flash memory is operating		430		µA
			f(CPU) = 32 kHz In low-power consumption mode While flash memory is stopped(2)		30		µA
			Wait mode: f(CPU) = f(Ring) After entering wait mode from on-chip oscillator low-power consumption mode		50		µA
			Stop mode (while clock is stopped)		0.8	5	µA
			Stop mode (while clock is stopped) Topr = 85°C			50	µA
		Mask ROM version	f(CPU) = 32 MHz		32	45	mA
			f(CPU) = 16 MHz		19		mA
			f(CPU) = 8 MHz		12		mA
			f(CPU) = f(Ring) In on-chip oscillator low-power consumption mode		1		mA
			f(CPU) = 32 kHz In low-power consumption mode		30		µA
			Wait mode: f(CPU) = f(Ring) After entering wait mode from on-chip oscillator low-power consumption mode		50		µA
			Stop mode (while clock is stopped)		0.8	5	µA
			Stop mode (while clock is stopped) Topr = 85°C			50	µA

NOTES:
1. In single-chip mode, leave the output pins open and connect the input pins to VSS.
2. Value is obtained when setting the FMSTP bit in the FMR0 register to 1 (flash memory stopped) and running the program on RAM.

VCC1 = VCC2 = 5V

Table 5.10 Flash Memory Electrical Characteristics (VCC1 = 4.5 V to 5.5 V, 3.0 to 3.6 V, Topr = 0 to 60°C unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
–	Erase and program endurance(1)		100			times
–	Word program time (16 bits) (VCC1 = 5.0 V, Topr = 25°C)			25	300	µs
–	Lock bit program time			25	300	µs
–	Block erase time (VCC1 = 5.0 V, Topr = 25°C)	4-Kbyte block		0.3	4	s
		8-Kbyte block		0.3	4	s
		32-Kbyte block		0.5	4	s
		64-Kbyte block		0.8	4	s
tps	Wait time to stabilize flash memory circuit				15	µs
–	Data hold time (Topr = -40 to 85°C)		10			years

NOTE:
1. If erase and program endurance is n times (n = 100), each block can be erased n times. For example, if a 4-Kbyte block A is erased after programming a word data 2,048 times, each to a different address, this counts as one erase and program time. Data can not be programmed to the same address more than once without erasing the block. (rewrite prohibited)

VCC1 = VCC2 = 5V

Timing Requirements
(VCC1 = VCC2 = 4.2 to 5.5 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.23 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(AD)	$\overline{\text{ADTRG}}$ input cycle time (required for trigger)	1000		ns
tw(ADL)	$\overline{\text{ADTRG}}$ input low (“L”) pulse width	125		ns

Table 5.24 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CK)	CLKi input cycle time	200		ns
tw(CKH)	CLKi input high (“H”) pulse width	100		ns
tw(CKL)	CLKi input low (“L”) pulse width	100		ns
td(C-Q)	TXDi output delay time		80	ns
th(C-Q)	TXDi output hold time	0		ns
tsu(D-C)	RXDi input setup time	70		ns
th(C-D)	RXDi input hold time	90		ns

i = 0 to 6

Table 5.25 Intelligent I/O Communication Function (Groups 0 and 1)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CK)	ISCLKi input cycle time	600		ns
tw(CKH)	ISCLKi input high (“H”) pulse width	300		ns
tw(CKL)	ISCLKi input low (“L”) pulse width	300		ns
td(C-Q)	ISTXDi output delay time		100	ns
th(C-Q)	ISTXDi output hold time	0		ns
tsu(D-C)	ISRXDi input setup time	100		ns
th(C-D)	ISRXDi input hold time	100		ns

i = 0, 1

Table 5.26 Intelligent I/O Communication Function (Group 2)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CK)	ISCLK2 input cycle time	600		ns
tw(CKH)	ISCLK2 input high (“H”) pulse width	300		ns
tw(CKL)	ISCLK2 input low (“L”) pulse width	300		ns
td(C-Q)	ISTXD2 output delay time		180	ns
th(C-Q)	ISTXD2 output hold time	0		ns
tsu(D-C)	ISRXD2 input setup time	150		ns
th(C-D)	ISRXD2 input hold time	100		ns

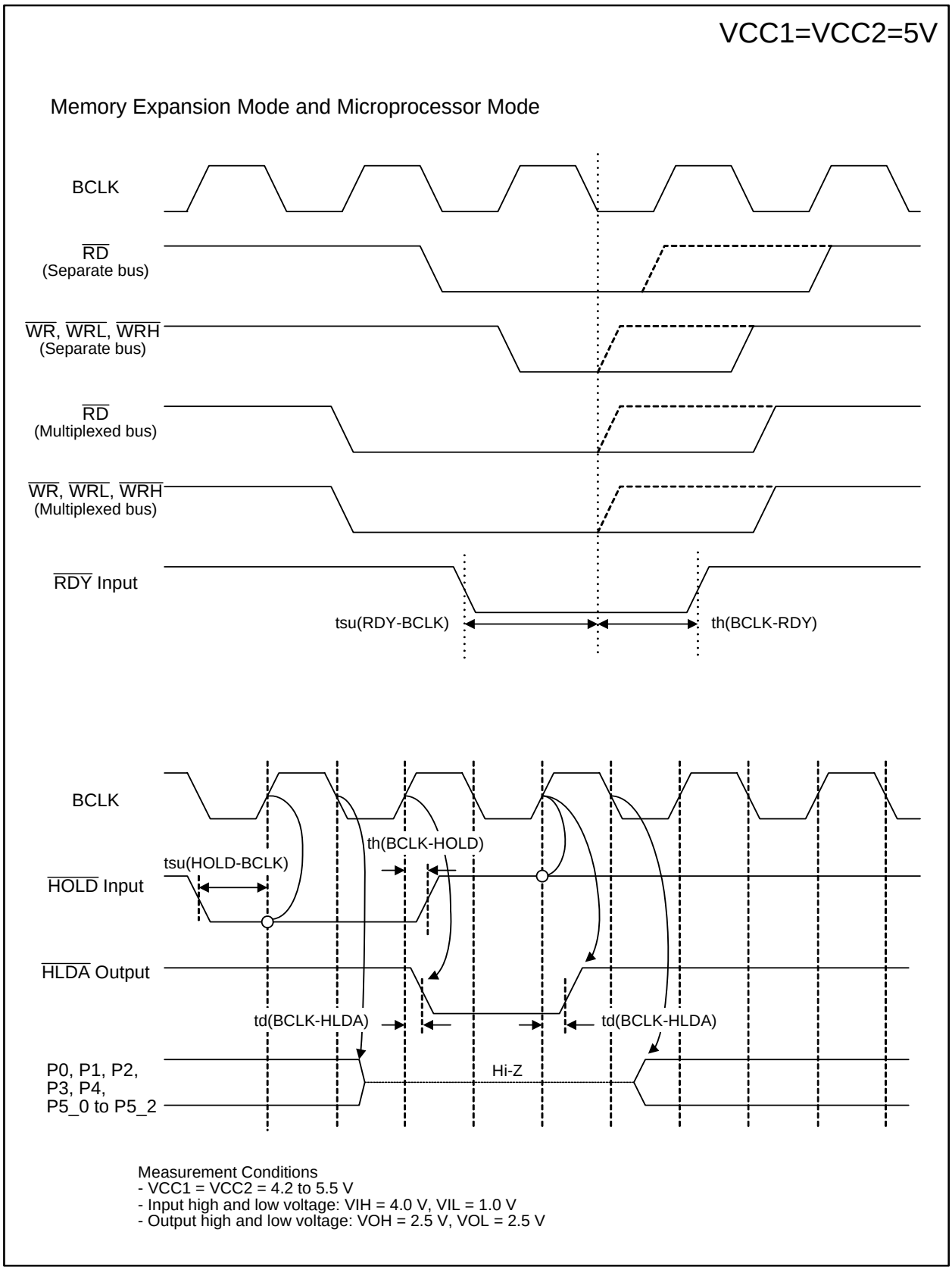


Figure 5.4 VCC1 = VCC2 = 5 V Timing Diagram (2/4)

VCC1 = VCC2 = 3.3 V

Timing Requirements
(VCC1 = VCC2 = 3.0 to 3.6 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.46 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(AD)	$\overline{\text{ADTRG}}$ input cycle time (required for trigger)	1000		ns
tw(ADL)	$\overline{\text{ADTRG}}$ input low (“L”) pulse width	125		ns

Table 5.47 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CK)	CLKi input cycle time	200		ns
tw(CKH)	CLKi input high (“H”) pulse width	100		ns
tw(CKL)	CLKi input low (“L”) pulse width	100		ns
td(C-Q)	TXDi output delay time		80	ns
th(C-Q)	TXDi output hold time	0		ns
tsu(D-C)	RXDi input setup time	70		ns
th(C-D)	RXDi input hold time	90		ns

i = 0 to 6

Table 5.48 Intelligent I/O Communication Function (Groups 0 and 1)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CK)	ISCLKi input cycle time	600		ns
tw(CKH)	ISCLKi input high (“H”) pulse width	300		ns
tw(CKL)	ISCLKi input low (“L”) pulse width	300		ns
td(C-Q)	ISTXDi output delay time		100	ns
th(C-Q)	ISTXDi output hold time	0		ns
tsu(D-C)	ISRXDi input setup time	100		ns
th(C-D)	ISRXDi input hold time	100		ns

i = 0, 1

Table 5.49 Intelligent I/O Communication Function (Group 2)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CK)	ISCLK2 input cycle time	600		ns
tw(CKH)	ISCLK2 input high (“H”) pulse width	300		ns
tw(CKL)	ISCLK2 input low (“L”) pulse width	300		ns
td(C-Q)	ISTXD2 output delay time		180	ns
th(C-Q)	ISTXD2 output hold time	0		ns
tsu(D-C)	ISRXD2 input setup time	150		ns
th(C-D)	ISRXD2 input hold time	100		ns

VCC1 = VCC2 = 3.3 V

Timing Requirements
(VCC1 = VCC2 = 3.0 to 3.6 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.50 External Interrupt $\overline{INTi}$ Input (Edge Sensitive)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tw(INH)	$\overline{INTi}$ input high (“H”) pulse width	250		ns
tw(INL)	$\overline{INTi}$ input low (“L”) pulse width	250		ns

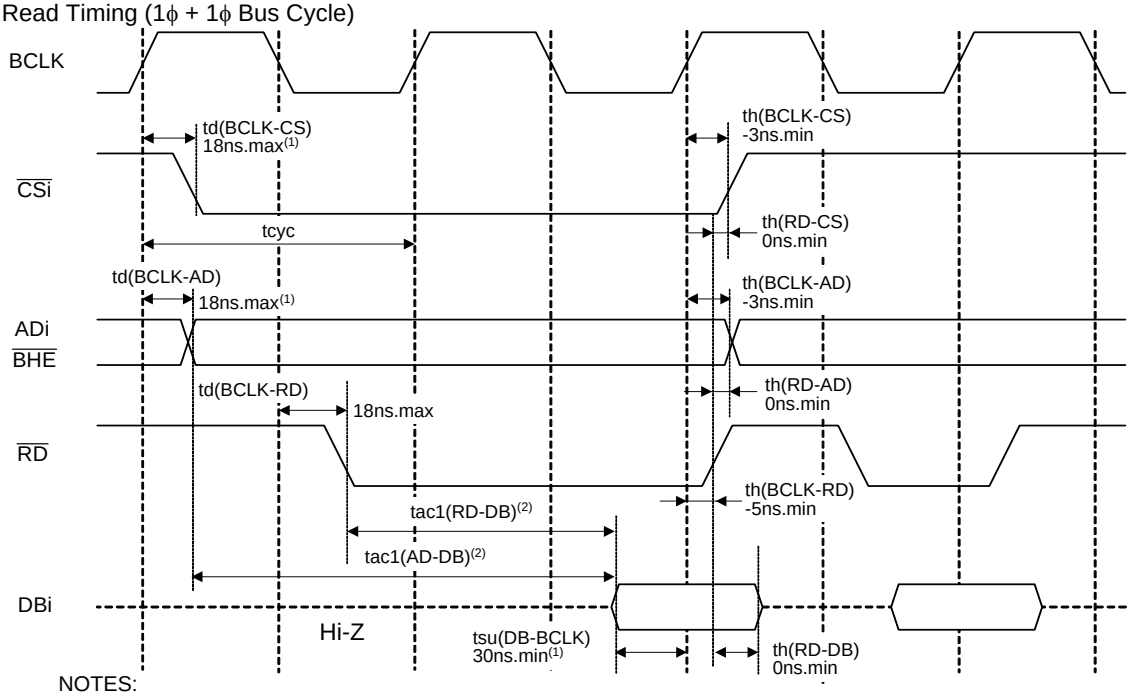
i = 0 to 8(1)

NOTE:
1. $\overline{INT6}$ to $\overline{INT8}$ are provided in the 144-pin package only.

Memory Expansion Mode and Microprocessor Mode
(when accessing an external memory space)

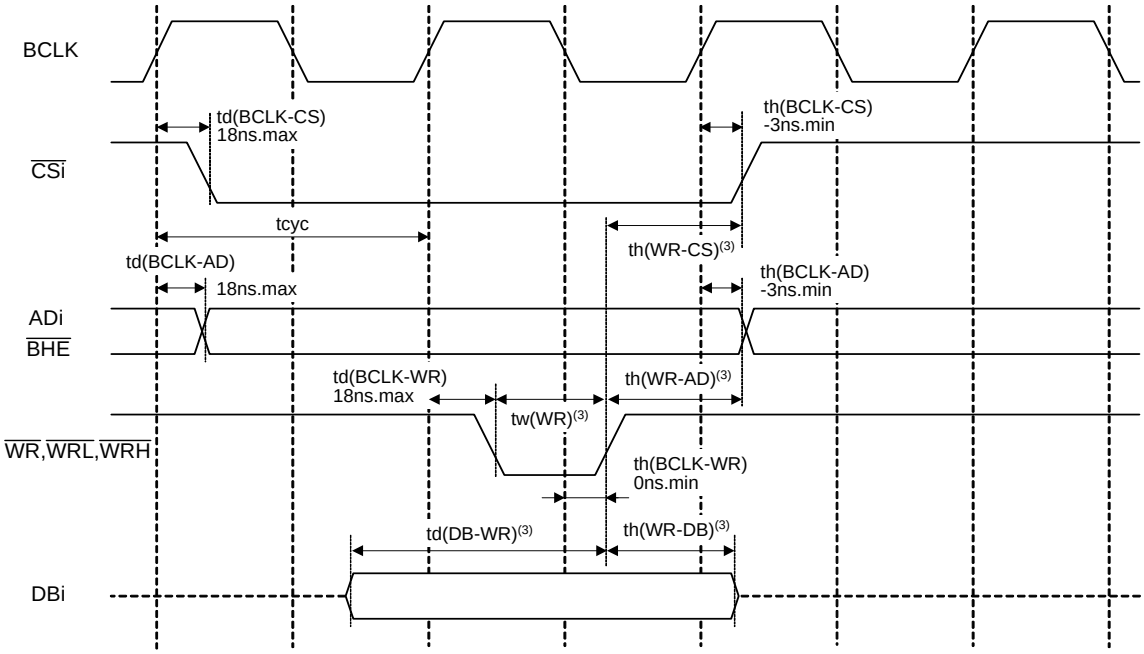
VCC1=VCC2=3.3V

Read Timing (1ϕ + 1ϕ Bus Cycle)



NOTES:
1. Values guaranteed only when the MCU is used stand-alone.
   A maximum of 35 ns is guaranteed for td(BCLK-AD) + tsu(DB-BCLK).
2. Varies with operation frequency:
   tac1(RD-DB) = (tcyc / 2 x m - 35) ns.max (if external bus cycle aϕ + bϕ, m = (b x 2) + 1)
   tac1(AD-DB) = (tcyc x n - 35) ns.max (if external bus cycle aϕ + bϕ, n = a + b)

Write Timing (1ϕ + 1ϕ Bus Cycle)



NOTES:
3. Varies with operation frequency:
   td(DB-WR) = (tcyc x m - 20) ns.min
   (if external bus cycle aϕ + bϕ, m = b)
   th(WR-DB) = (tcyc / 2 - 20) ns.min
   th(WR-AD) = (tcyc / 2 - 15) ns.min
   th(WR-CS) = (tcyc / 2 - 10) ns.min
   tw(WR) = (tcyc / 2 x n - 15) ns.min
   (if external bus cycle aϕ + bϕ, n = (b x 2) - 1)

Measurement Conditions:
- VCC1 = VCC2 = 3.0 to 3.6 V
- Input high and low voltage: VIH = 1.5 V, VIL = 0.5 V
- Output high and low voltage: VOH = 1.5 V, VOL = 1.5 V

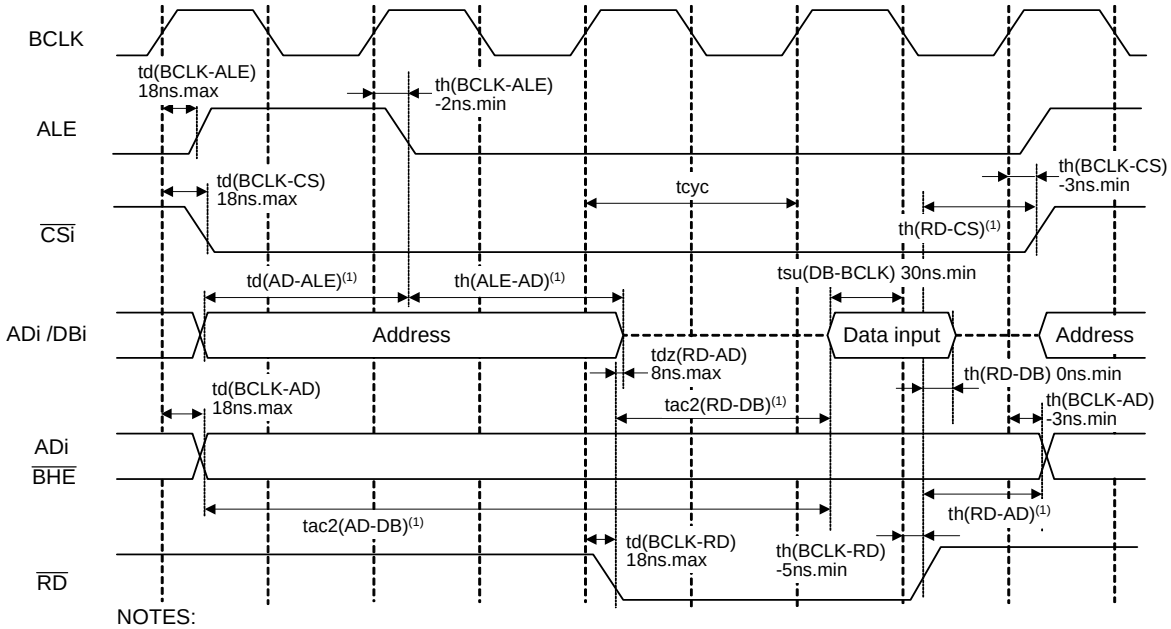
$$tcyc = \frac{10^9}{f(BCLK)}$$

Figure 5.9 VCC1 = VCC2 = 3.3 V Timing Diagram (3/4)

Memory Expansion Mode and Microprocessor Mode
(when accessing an external memory space with the multiplexed bus)

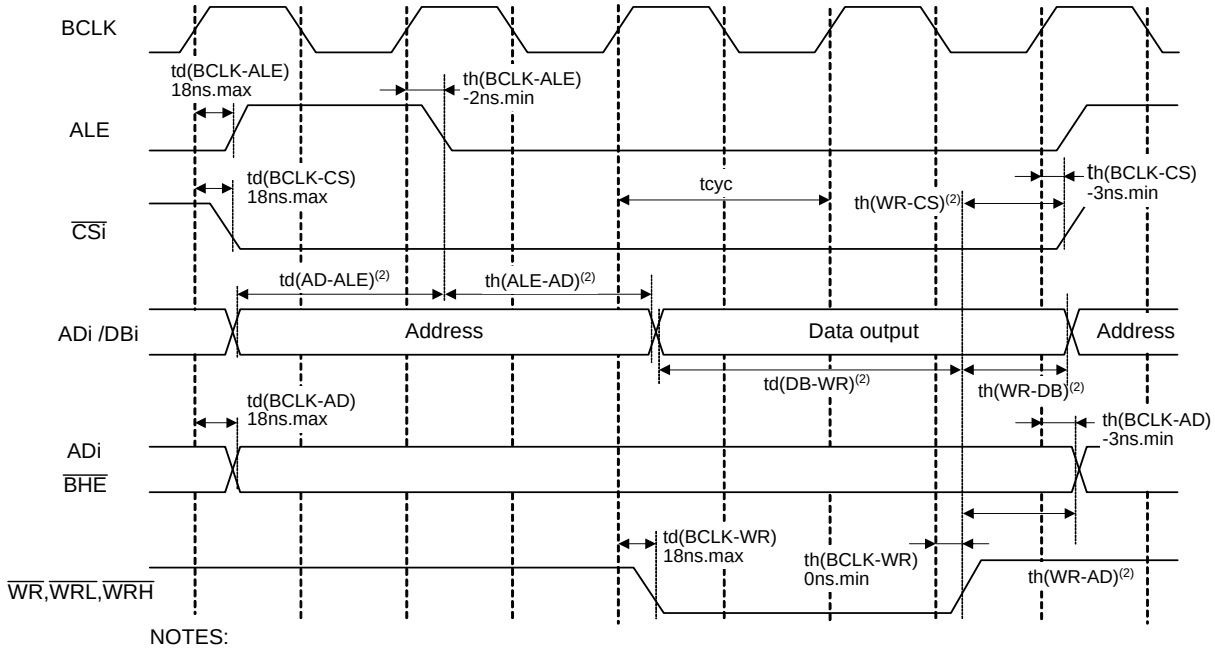
VCC1=VCC2=3.3V

Read Timing (2ϕ + 2ϕ Bus Cycle)



NOTES:
1. Varies with operation frequency:
td(AD-ALE) = (tcyc / 2 x n - 20) ns.min (if external bus cycle aϕ + bϕ, n = a)
th(ALE-AD) = (tcyc / 2 x n - 20) ns.min (if external bus cycle aϕ + bϕ, n = a)
th(RD-AD) = (tcyc / 2 - 10) ns.min, th(RD-CS) = (tcyc / 2 - 10) ns.min
tac2(RD-DB) = (tcyc / 2 x m - 35) ns.max (if external bus cycle aϕ + bϕ, m = (b x 2) - 1)
tac2(AD-DB) = (tcyc / 2 x p - 35) ns.max (if external bus cycle aϕ + bϕ, p = {(a + b - 1) x 2} + 1)

Write Timing (2ϕ + 2ϕ Bus Cycle)



NOTES:
1. Varies with operation frequency:
td(AD-ALE) = (tcyc / 2 x n - 20) ns.min (if external bus cycle aϕ + bϕ, n = a)
th(ALE-AD) = (tcyc / 2 x n - 20) ns.min (if external bus cycle aϕ + bϕ, n = a)
th(WR-AD) = (tcyc / 2 - 15) ns.min, th(WR-CS) = (tcyc / 2 - 10) ns.min
th(WR-DB) = (tcyc / 2 - 20) ns.min
td(DB-WR) = (tcyc / 2 x m - 25) ns.min (if external bus cycle aϕ + bϕ, m = (b x 2) - 1)

$$tcyc = \frac{10^9}{f(BCLK)}$$

Measurement Conditions:
- VCC1 = VCC2 = 3.0 to 3.6 V
- Input high and low voltage VIH = 1.5 V, VIL = 0.5 V
- Output high and low voltage VOH = 1.5 V, VOL = 1.5 V

Figure 5.10 VCC1 = VCC2 = 3.3 V Timing Diagram (4/4)

REVISION HISTORY	M32C/87 Group Datasheet

Rev.	Date	Description	
		Page	Summary
			Electrical Characteristics
		57	• **Table 5.22 Memory Expansion Mode and Microprocessor Mode** *th(WR-DB)* expression on note 1 modified
		58	• **Table 5.23 Memory Expansion Mode and Microprocessor Mode** *th(WR-DB)* expression on note 1 modified; *th(ALE-AD)* expression on note 4 modified
		60	• **Figure 5.3 Vcc1=Vcc2=5V Timing Diagram (1)** *tac1(RD-DB)* expression on note 2 modified; *th(WR-DB)* and *tw(ER)* expressions on note 3 modified; *tcyc* expression added
		61	• **Figure 5.4 Vcc1=Vcc2=5V Timing Diagram (2)** *tac2(RD-DB) and tac2(AD-DB)* expressions on note 1 modified; *th(ALE-AD)* expressions on notes 1 and 2 modified; *td(DB-WR)* expression on note 2 modified; *tcyc* expression added
		62	• **Figure 5.5 Vcc1=Vcc2=5V Timing Diagram (3)** $\overline{\text{NMI}}$ input diagram added
		64	• **Table 5.24 Electrical Characteristics** V_{OH} values changed**;** R_{PULLUP} and Icc values modified
		65	• **Table 5.25 A/D Conversion Characteristics** tCONV value modified
		66	• **Table 5.28 Memory Expansion Mode and Microprocessor Mode** *tac1(RD-DB)* expression on note 1 modified; *tac2(RD-DB)* expression on note 1 added
		69	• **Table 5.40 Memory Expansion Mode and Microprocessor Mode** *th(BCLK-AD), th(BCLK-CS)* and *th(BCLK-RD)* values modified; *th(WR-AD)* expression on note 1 modified
		70	• **Table 5.41 Memory Expansion Mode and Microprocessor Mode** *th(BCLK-AD), th(BCLK-CS)* and *th(BCLK-RD)* values modified; *th(WR-AD)* expression on note 1 modified; *th(ALE-AD)* expression on note 4 modified
		71	• **Figure 5.7 Vcc1=Vcc2=3.3V Timing Diagram (1)** *th(BCLK-AD), th(BCLK-CS)* and *th(BCLK-RD)* values modified; *tac1(AD-DB)* expression on note 2 modified; *th(WR-DB)*, *th(WR-AD) and tw(WR)* expression on note 3 modified; *tcyc* expression added
		72	• **Figure 5.8 Vcc1=Vcc2=3.3V Timing Diagram (2)** *tac2(RD-DB) and tac1(AD-DB)* expressions on note 1 modified; *th(ALE-AD)* expressions on notes 1 and 2 modified; *td(WR-AD)*, *td(DB-WR) and th(WR-DB)* expressions on note 2 modified; *tcyc* expression added
		73	• **Figure 5.9 Vcc1=Vcc2=3.3V Timing Diagram (3)** $\overline{\text{NMI}}$ input diagram added
1.01	Aug. 29, 05		Overview
		17	• **Tables 1.6 Pin Description** Intelligent I/O functions modified
			Special Function Register (SFR)
		29	• The G1BCR0 register Value after reset modified
		29	• The G1BCR1 register Value after reset modified
			Electrical Characteristics
		49	• **Table 5.3 Electrical Characteristics** Icc standard value modified