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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, Cap Sense, DMA, I²S, POR, PWM, WDT
Number of I/O	37
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l151c8t6

HSE crystal oscillators are disabled. The voltage regulator is in the low power mode. The device can be woken up from Stop mode by any of the EXTI line, in 8 µs. The EXTI line source can be one of the 16 external lines. It can be the PVD output, the Comparator 1 event or Comparator 2 event (if internal reference voltage is on). It can also be wakened by the USB wakeup.

Stop mode consumption: refer to *Table 22: Typical and maximum current consumptions in Stop mode*.

- **Standby** mode with RTC

  Standby mode is used to achieve the lowest power consumption and real time clock. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSI RC and HSE crystal oscillators are also switched off. The LSE or LSI is still running. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC_CSR).

  The device exits Standby mode in 60 µs when an external reset (NRST pin), an IWDG reset, a rising edge on one of the three WKUP pins, RTC alarm (Alarm A or Alarm B), RTC tamper event, RTC timestamp event or RTC Wakeup event occurs.

- **Standby** mode without RTC

  Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI, RC, HSI and LSI RC, HSE and LSE crystal oscillators are also switched off. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC_CSR).

  The device exits Standby mode in 60 µs when an external reset (NRST pin) or a rising edge on one of the three WKUP pin occurs.

  Standby mode consumption: refer to *Table 23*.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering the Stop or Standby mode.

Table 3. Functionalities depending on the operating power supply range

Operating power supply range	Functionalities depending on the operating power supply range			
	DAC and ADC operation	USB	Dynamic voltage scaling range	I/O operation
V_{DD} = 1.65 to 1.71 V	Not functional	Not functional	Range 2 or Range 3	Degraded speed performance
V_{DD} = 1.71 to 1.8 V(1)	Not functional	Not functional	Range 1, Range 2 or Range 3	Degraded speed performance
V_{DD} = 1.8 to 2.0 V(1)	Conversion time up to 500 Ksps	Not functional	Range 1, Range 2 or Range 3	Degraded speed performance

Table 5. Working mode-dependent functionalities (from Run/active down to standby) (continued)

Ips	Run/Active	Sleep	Low-power Run	Low-power Sleep	Stop		Standby	
						Wakeup capability		Wakeup capability
DAC	Y	Y	Y	Y	Y	-	-	-
Temperature sensor	Y	Y	Y	Y	Y	-	-	-
Comparators	Y	Y	Y	Y	Y	Y	-	-
16-bit and 32-bit Timers	Y	Y	Y	Y	-	-	-	-
IWDG	Y	Y	Y	Y	Y	Y	Y	Y
WWDG	Y	Y	Y	Y	-	-	-	-
Touch sensing	Y	-	-	-	-	-	-	-
Systick Timer	Y	Y	Y	Y	-	-	-	-
GPIOs	Y	Y	Y	Y	Y	Y	-	3 Pins
Wakeup time to Run mode	0 µs	0.36 µs	3 µs	32 µs	< 8 µs		50 µs	
Consumption V_{DD}=1.8V to 3.6V (Typ)	Down to 214 µA/MHz (from Flash)	Down to 50 µA/MHz (from Flash)	Down to 9 µA	Down to 4.4 µA	0.5 µA (No RTC) V_{DD}=1.8V		0.3 µA (No RTC) V_{DD}=1.8V	
					1.4 µA (with RTC) V_{DD}=1.8V		1 µA (with RTC) V_{DD}=1.8V	
					0.5 µA (No RTC) V_{DD}=3.0V		0.3 µA (No RTC) V_{DD}=3.0V	
					1.6 µA (with RTC) V_{DD}=3.0V		1.3 µA (with RTC) V_{DD}=3.0V	

1. The startup on communication line wakes the CPU which was made possible by an EXTI, this induces a delay before entering run mode.

3.2 ARM® Cortex®-M3 core with MPU

The ARM® Cortex®-M3 processor is the industry leading processor for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM® Cortex®-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The memory protection unit (MPU) improves system reliability by defining the memory attributes (such as read/write access permissions) for different memory regions. It provides up to eight different regions and an optional predefined background region.

Owing to its embedded ARM core, the STM32L151x6/8/B and STM32L152x6/8/B devices are compatible with all ARM tools and software.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channels' independent or simultaneous conversions
- DMA capability for each channel (including the underrun interrupt)
- external triggers for conversion
- input reference voltage V_{REF+}

Eight DAC trigger inputs are used in the STM32L151x6/8/B and STM32L152x6/8/B devices. The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

3.12 Ultra-low-power comparators and reference voltage

The STM32L151x6/8/B and STM32L152x6/8/B devices embed two comparators sharing the same current bias and reference voltage. The reference voltage can be internal or external (coming from an I/O).

- one comparator with fixed threshold
- one comparator with rail-to-rail inputs, fast or slow mode. The threshold can be one of the following:
  - DAC output
  - External I/O
  - Internal reference voltage (V_{REFINT}) or V_{REFINT} submultiple (1/4, 1/2, 3/4)

Both comparators can wake up from Stop mode, and be combined into a window comparator.

The internal reference voltage is available externally via a low power / low current output buffer (driving current capability of 1 µA typical).

3.13 Routing interface

This interface controls the internal routing of I/Os to TIM2, TIM3, TIM4 and to the comparator and reference voltage output.

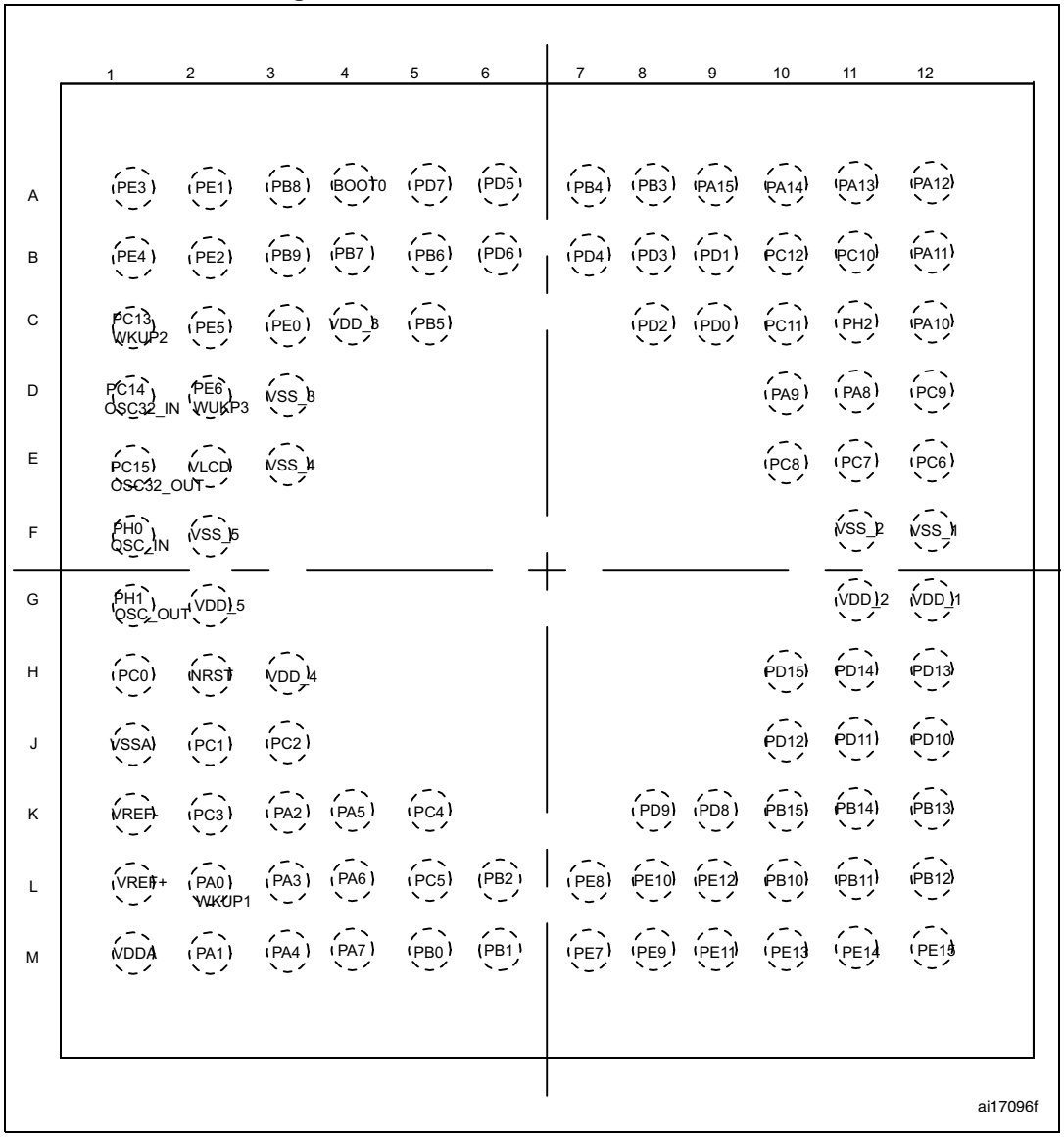
3.14 Touch sensing

The STM32L151x6/8/B and STM32L152x6/8/B devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 20 capacitive sensing channels distributed over 10 analog I/O groups. Only software capacitive sensing acquisition mode is supported.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (glass, plastic, ...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven

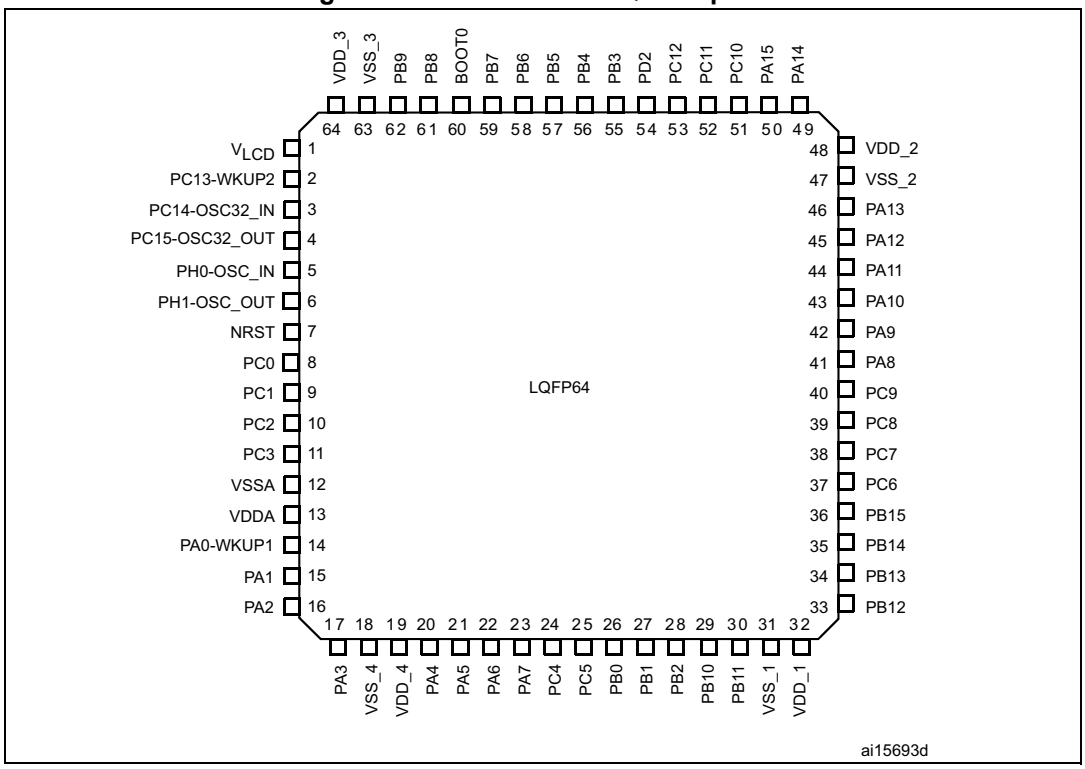
4 Pin descriptions

Figure 3. STM32L15xVx UFBGA100 ballout



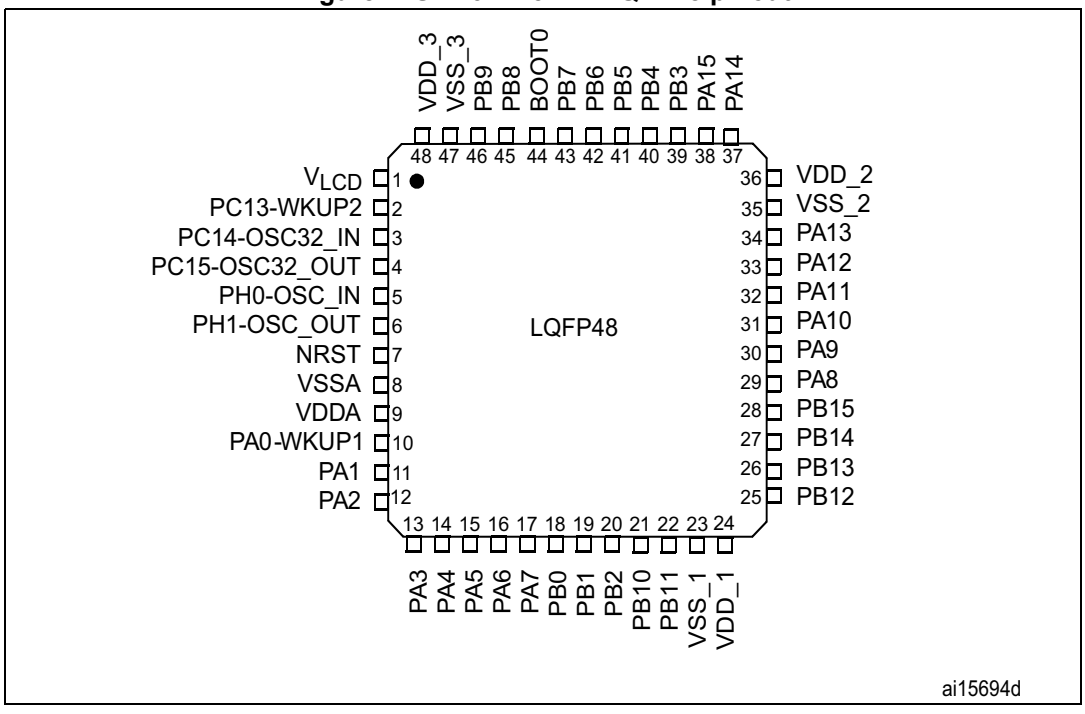
1. This figure shows the package top view.

Figure 6. STM32L15xRx LQFP64 pinout



1. This figure shows the package top view.

Figure 7. STM32L15xCx LQFP48 pinout



1. This figure shows the package top view.

Table 8. STM32L151x6/8/B and STM32L152x6/8/B pin definitions (continued)

Pins					Pin name	Pin type[1]	I/O structure	Main function[2] (after reset)	Pins functions	
LQFP100	LQFP64	TFBGA64	UFBGA100	LQFP48 or UFQFPN48					Alternate functions	Additional functions
90	56	A4	A7	40	PB4	I/O	FT	NJTRST	TIM3_CH1/PB4/ SPI1_MISO/LCD_SEG8/ NJTRST	COMP2_INP
91	57	C4	C5	41	PB5	I/O	FT	PB5	I2C1_SMBA/TIM3_CH2/ SPI1_MOSI/LCD_SEG9	COMP2_INP
92	58	D3	B5	42	PB6	I/O	FT	PB6	I2C1_SCL/TIM4_CH1/ USART1_TX	
93	59	C3	B4	43	PB7	I/O	FT	PB7	I2C1_SDA/TIM4_CH2/ USART1_RX	PVD_IN
94	60	B4	A4	44	BOOT0	I	B	BOOT0	-	-
95	61	B3	A3	45	PB8	I/O	FT	PB8	TIM4_CH3/I2C1_SCL/ LCD_SEG16/TIM10_CH1	-
96	62	A3	B3	46	PB9	I/O	FT	PB9	TIM4_CH4/I2C1_SDA/ LCD_COM3/TIM11_CH1	-
97	-	-	C3	-	PE0	I/O	FT	PE0	TIM4_ETR/LCD_SEG36/ TIM10_CH1	-
98	-	-	A2	-	PE1	I/O	FT	PE1	LCD_SEG37/TIM11_CH1	-
99	63	D4	D3	47	V_{SS_3}	S	-	V_{SS_3}	-	-
100	64	E4	C4	48	V_{DD_3}	S	-	V_{DD_3}	-	-

1. I = input, O = output, S = supply.
2. Function availability depends on the chosen device. For devices having reduced peripheral counts, it is always the lower number of peripheral that is included. For example, if a device has only one SPI and two USARTs, they will be called SPI1 and USART1 & USART2, respectively. Refer to *Table 2 on page 11*.
3. Applicable to STM32L152xx devices only. In STM32L151xx devices, this pin should be connected to V_{DD}.
4. The PC14 and PC15 I/Os are only configured as OSC32_IN/OSC32_OUT when the LSE oscillator is on (by setting the LSEON bit in the RCC_CSR register). The LSE oscillator pins OSC32_IN/OSC32_OUT can be used as general-purpose PC14/PC15 I/Os, respectively, when the LSE oscillator is off (after reset, the LSE oscillator is off). The LSE has priority over the GPIO function. For more details, refer to Using the OSC32_IN/OSC32_OUT pins as GPIO PC14/PC15 port pins section in the STM32L1xxxx reference manual (RM0038).
5. The PH0 and PH1 I/Os are only configured as OSC_IN/OSC_OUT when the HSE oscillator is on (by setting the HSEON bit in the RCC_CR register). The HSE oscillator pins OSC_IN/OSC_OUT can be used as general-purpose PH0/PH1 I/Os, respectively, when the HSE oscillator is off (after reset, the HSE oscillator is off). The HSE has priority over the GPIO function.
6. Unlike in the LQFP64 package, there is no PC3 in the TFBGA64 package. The V_{REF+} functionality is provided instead.

Table 9. Alternate function input/output (continued)

Port name	Digital alternate function number														
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFOI6	AFIO7	AFIO8	AFIO9	AFIO11	AFIO12	AFIO13	AFIO14	AFIO15
	Alternate function														
	SYSTEM	TIM2	TIM3/4	TIM9/10/11	I2C1/2	SPI1/2	N/A	USART1/2/3	N/A	N/A	LCD	N/A	N/A	RI	SYSTEM
PH1-OSC_OUT	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PH2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

6.1.6 Power supply scheme

Figure 12. Power supply scheme

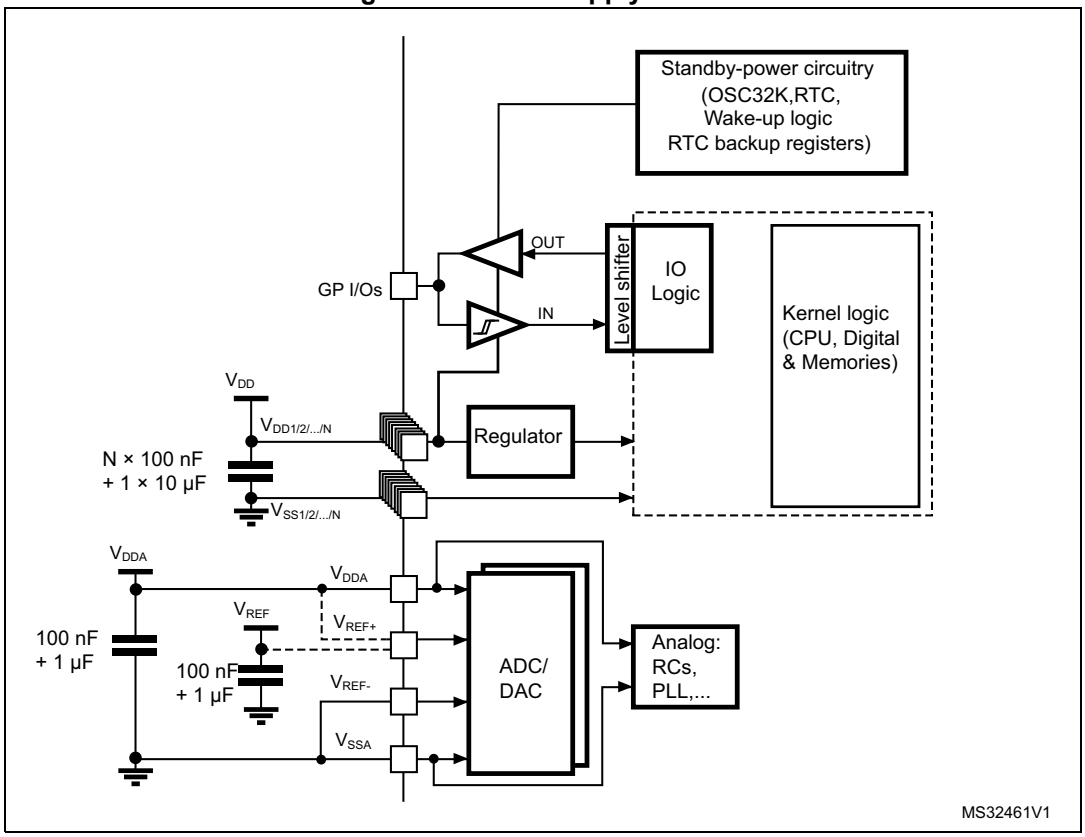


Table 19. Current consumption in Sleep mode

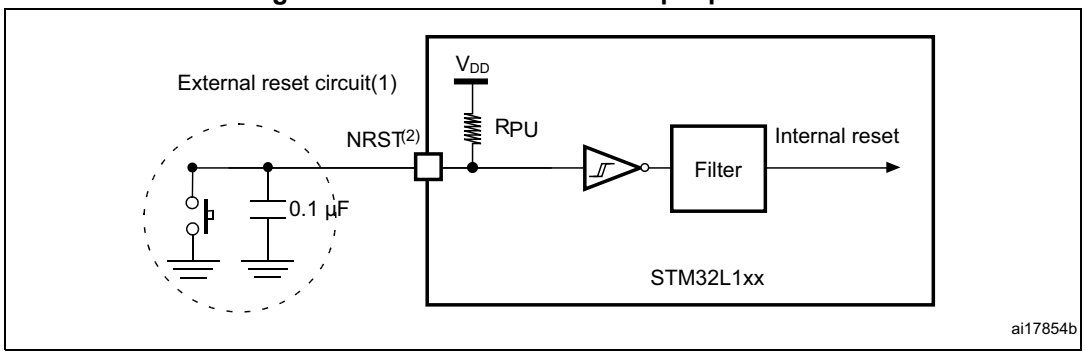
Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max(1)			Unit
						55 °C	85 °C	105 °C	
I_{DD} (Sleep)	Supply current in Sleep mode, code executed from RAM, Flash switched OFF	f_{HSE} = f_{HCLK} up to 16 MHz included, f_{HSE} = f_{HCLK}/2 above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	1 MHz	80	140	140	140	µA
				2 MHz	150	210	210	210	
				4 MHz	280	330	330	330(3)	
			Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	4 MHz	280	400	400	400	
				8 MHz	450	550	550	550	
				16 MHz	900	1050	1050	1050	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	8 MHz	550	650	650	650	
				16 MHz	1050	1200	1200	1200	
				32 MHz	2300	2500	2500	2500	
		HSI clock source (16 MHz)	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	16 MHz	1000	1100	1100	1100	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	32 MHz	2300	2500	2500	2500	
		MSI clock, 65 kHz	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	65 kHz	30	50	50	60	
		MSI clock, 524 kHz		524 kHz	50	70	70	80	
		MSI clock, 4.2 MHz		4.2 MHz	200	240	240	250	
	Supply current in Sleep mode, code executed from Flash	f_{HSE} = f_{HCLK} up to 16 MHz included, f_{HSE} = f_{HCLK}/2 above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	1 MHz	80	140	140	140	µA
				2 MHz	150	210	210	210	
				4 MHz	290	350	350	350	
			Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	4 MHz	300	400	400	400	
				8 MHz	500	600	600	600	
				16 MHz	1000	1100	1100	1100	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	8 MHz	550	650	650	650	
				16 MHz	1050	1200	1200	1200	
				32 MHz	2300	2500	2500	2500	
		HSI clock source (16 MHz)	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	16 MHz	1000	1100	1100	1100	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	32 MHz	2300	2500	2500	2500	

Table 20. Current consumption in Low power run mode

Symbol	Parameter	Conditions			Typ	Max (1)	Unit
$I_{DD\ (LP\ Run)}$	Supply current in Low power run mode	All peripherals OFF, code executed from RAM, Flash switched OFF, V_{DD} from 1.65 V to 3.6 V	MSI clock, 65 kHz f_{HCLK} = 32 kHz	T_A = -40 °C to 25 °C	9	12	µA
				T_A = 85 °C	17.5	24	
				T_A = 105 °C	31	46	
			MSI clock, 65 kHz f_{HCLK} = 65 kHz	T_A = -40 °C to 25 °C	14	17	
				T_A = 85 °C	22	29	
				T_A = 105 °C	35	51	
			MSI clock, 131 kHz f_{HCLK} = 131 kHz	T_A = -40 °C to 25 °C	37	42	
				T_A = 55 °C	37	42	
				T_A = 85 °C	37	42	
				T_A = 105 °C	48	65	
		All peripherals OFF, code executed from Flash, V_{DD} from 1.65 V to 3.6 V	MSI clock, 65 kHz f_{HCLK} = 32 kHz	T_A = -40 °C to 25 °C	24	32	
				T_A = 85 °C	33	42	
				T_A = 105 °C	48	64	
			MSI clock, 65 kHz f_{HCLK} = 65 kHz	T_A = -40 °C to 25 °C	31	40	
				T_A = 85 °C	40	48	
				T_A = 105 °C	54	70	
			MSI clock, 131 kHz f_{HCLK} = 131 kHz	T_A = -40 °C to 25 °C	48	58	
				T_A = 55 °C	54	63	
				T_A = 85 °C	56	65	
				T_A = 105 °C	70	90	
I_{DD} Max (LP Run)(2)	Max allowed current in Low power run mode	V_{DD} from 1.65 V to 3.6 V	-	-	-	200	

1. Guaranteed by characterization results, unless otherwise specified.
2. This limitation is related to the consumption of the CPU core and the peripherals that are powered by the regulator. Consumption of the I/Os is not included in this limitation.

Figure 20. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 45*. Otherwise the reset will not be taken into account by the device.

6.3.15 TIM timer characteristics

The parameters given in *Table 46* are guaranteed by design.

Refer to *Section 6.3.13: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 46. TIMx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 32 MHz	31.25	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 32 MHz	0	16	MHz
Res_{TIM}	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected (timer's prescaler disabled)	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 32 MHz	0.0312	2048	µs
t_{MAX_COUNT}	Maximum possible count	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 32 MHz	-	134.2	s

1. TIMx is used as a general term to refer to the TIM2, TIM3 and TIM4 timers.

6.3.16 Communication interfaces

I²C interface characteristics

The STM32L151x6/8/B and STM32L152x6/8/B product line I²C interface meets the requirements of the standard I²C communication protocol with the following restrictions: SDA and SCL are not “true” open-drain I/O pins. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

The I²C characteristics are described in *Table 47*. Refer also to *Section 6.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

Table 47. I²C characteristics

Symbol	Parameter	Standard mode I²C(1)		Fast mode I²C(1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0	-	0	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	20 + 0.1C_b	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	Stop condition setup time	4.0	-	0.6	-	µs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7	-	1.3	-	µs
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. Guaranteed by design.
2. f_{PCLK1} must be at least 2 MHz to achieve standard mode I²C frequencies. It must be at least 4 MHz to achieve fast mode I²C frequencies. It must be a multiple of 10 MHz to reach the 400 kHz maximum I²C fast mode clock.
3. The maximum Data hold time has only to be met if the interface does not stretch the low period of SCL signal.

6.3.18 DAC electrical specifications

Data guaranteed by design, unless otherwise specified.

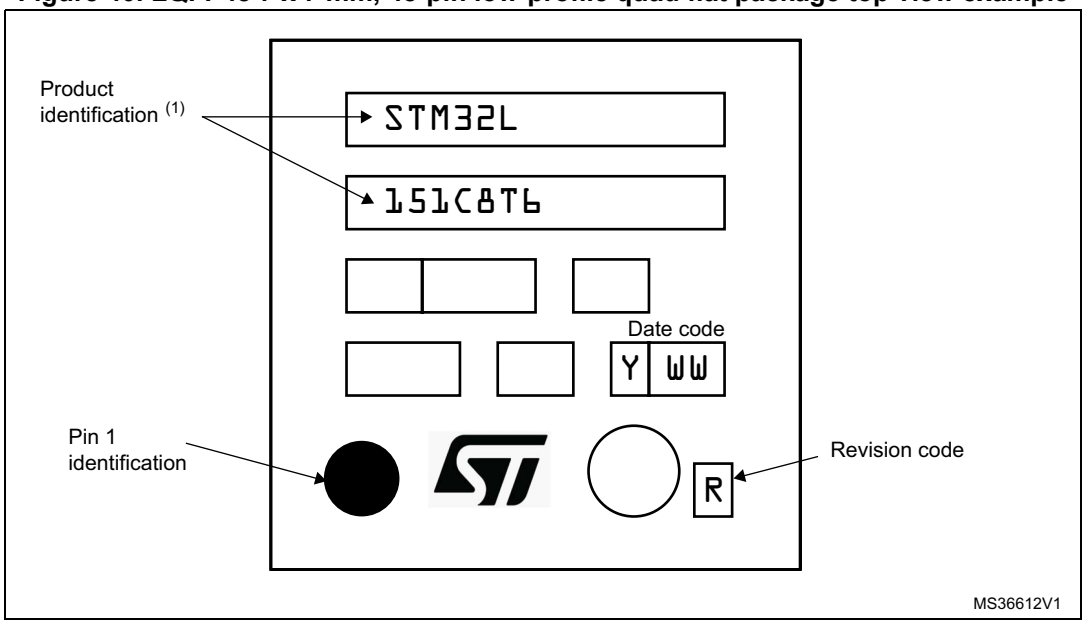
Table 57. DAC characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		1.8	-	3.6	V
V_{REF+}	Reference supply voltage	V_{REF+} must always be below V_{DDA}		1.8	-	3.6	V
V_{REF-}	Lower reference voltage	-			V_{SSA}		V
$I_{DDVREF+}$(1)	Current consumption on V_{REF+} supply V_{REF+} = 3.3 V	No load, middle code (0x800)		-	130	220	µA
		No load, worst code (0x000)		-	220	350	µA
I_{DDA}(1)	Current consumption on V_{DDA} supply V_{DDA} = 3.3 V	No load, middle code (0x800)		-	210	320	µA
		No load, worst code (0xF1C)		-	320	520	µA
R_L	Resistive load	DAC output buffer ON	Connected to V_{SSA}	5	-	-	kΩ
			Connected to V_{DDA}	25	-	-	
C_L	Capacitive load	DAC output buffer ON		-	-	50	pF
R_O	Output impedance	DAC output buffer OFF		12	16	20	kΩ
V_{DAC_OUT}	Voltage on DAC_OUT output	DAC output buffer ON		0.2	-	V_{DDA} – 0.2	V
		DAC output buffer OFF		0.5	-	V_{REF+} – 1LSB	mV
DNL(1)	Differential non linearity(2)	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON		-	1.5	3	LSB
		No R_{LOAD}, $C_L \leq 50$ pF DAC output buffer OFF		-	1.5	3	
INL(1)	Integral non linearity(3)	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON		-	2	4	
		No R_{LOAD}, $C_L \leq 50$ pF DAC output buffer OFF		-	2	4	
Offset(1)	Offset error at code 0x800 (4)	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON		-	±10	±25	
		No R_{LOAD}, $C_L \leq 50$ pF DAC output buffer OFF		-	±5	±8	
Offset1(1)	Offset error at code 0x001(5)	No R_{LOAD}, $C_L \leq 50$ pF DAC output buffer OFF		-	±1.5	±5	

LQFP48 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 40. LQFP48 7 x 7 mm, 48-pin low-profile quad flat package top view example



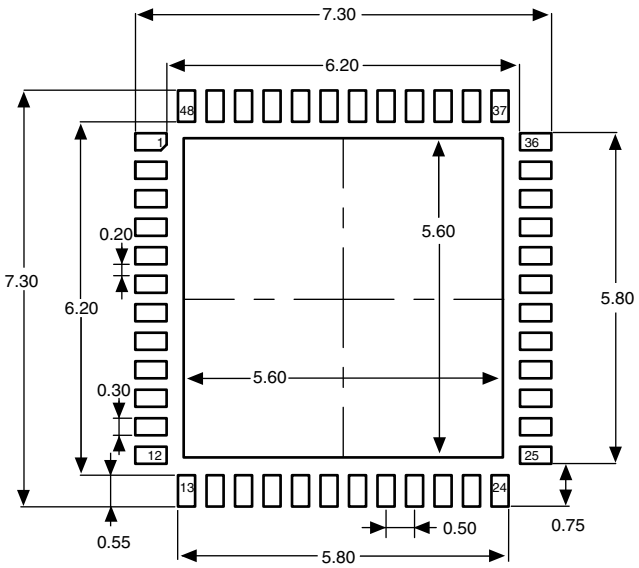
1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 66. UFQFPN48 7 x 7 mm, 0.5 mm pitch, package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 42. UFQFPN48 7 x 7 mm, 0.5 mm pitch, package recommended footprint



1. Dimensions are in millimeters.

Table 69. TFBGA64 5 x 5 mm, 0.5 mm pitch, package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
eee	-	-	0.15	-	-	0.0059
fff	-	-	0.05	-	-	0.002

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 48. TFBGA64, 5 x 5 mm, 0.5 mm pitch, recommended footprint

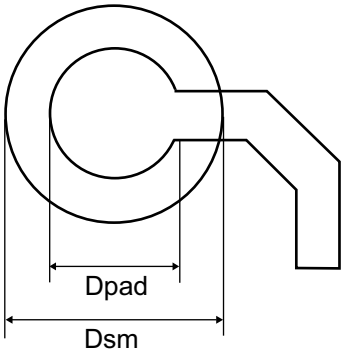


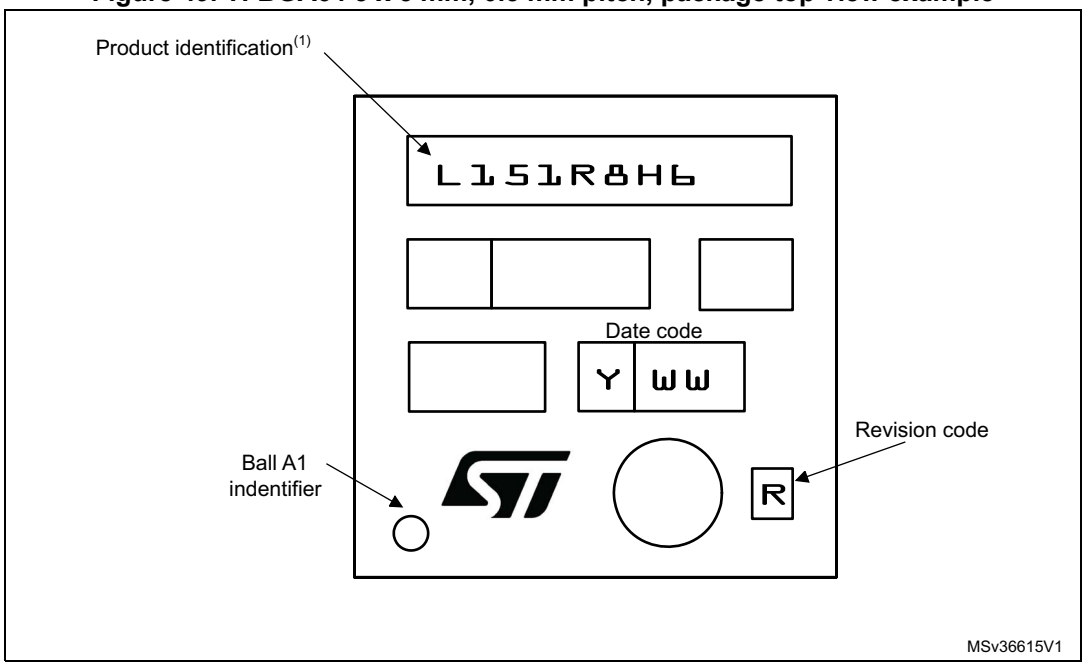
Table 70. TFBGA64 5 x 5 mm, 0.5 mm pitch, recommended PCB design rules

Dimension	Recommended values
Pitch	0.5
Dpad	0.27 mm
Dsm	0.35 mm typ. (depends on the soldermask registration tolerance)
Solder paste	0.27 mm aperture diameter.

TFBGA64 device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Figure 49. TFBGA64 5 x 5 mm, 0.5 mm pitch, package top view example



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 73. Document revision history (continued)

Date	Revision	Changes
12-Nov-2013	9 (continued)	Updated *Table 54: ADC characteristics* and *Figure 27: Typical connection diagram using the ADC*. *Table 58: Temperature sensor calibration values* was previously in *Section 3.10.1: Temperature sensor*. Updated *Table 59: Temperature sensor characteristics*. In *Table 61: Comparator 2 characteristics*, parameter dThreshold/dt, replaced any occurrence of “VREF+” by “V_{REFINT}”Updated *Table 63: LQPF100 14 x 14 mm, 100-pin low-profile quad flat package mechanical data*, *Table 64: LQFP64 10 x 10 mm 64-pin low-profile quad flat package mechanical data*, *Table 65: LQFP48 7 x 7 mm, 48-pin low-profile quad flat package mechanical data* and *Table 66: UFQFPN48 7 x 7 mm, 0.5 mm pitch, ultra thin fine-pitch quad flat no-lead package mechanical data*. Updated *Figure 33: LQFP100 recommended footprint*. Updated *Figure 46: TFBGA64 - 5.0x5.0x1.2 mm, 0.5 mm pitch, thin fine-pitch ball grid array package outline* title. Remove minimum and typical values of A dimension in *Table 67: UFBGA100 7 x 7 x 0.6 mm 0.5 mm pitch, ultra thin fine-pitch ball grid array package mechanical data* Deleted second footnote in *Figure 42: UFQFPN48 recommended footprint*. Updated *Section 8: Ordering information* title and added first sentence. Changed BOR disabled option identifier in *Table 72: Ordering information scheme*.
22-Jul-2014	10	Updated *Figure 14*, *Figure 15*. Updated *Table 5*. Updated *Figure 6.3.4*. Updated note *5* inside *Table 54*. Updated Ro value inside *Table 54*.

Table 73. Document revision history (continued)

Date	Revision	Changes
30-Jan-2015	11	Updated DMIPS features in cover page and *Section 2: Description*. Updated *Table 8: STM32L151x6/8/B and STM32L152x6/8/B pin definitions* and *Table 9: Alternate function input/output* putting additional functions. Updated package top view marking in *Section 7.1: Package mechanical data*. Updated *Figure 9: Memory map*. Updated *Table 56: Maximum source impedance RAIN max* adding note 2. Updated *Table 72: Ordering information scheme*.
28-Apr-2016	12	Updated *Section 7: Package information* structure: Paragraph titles and paragraph heading level. Updated *Section 7: Package information* for all package device markings, adding text for device orientation versus pin 1/ ball A1 identifier. Updated *Figure 34: LQFP100 14 x 14 mm, 100-pin package top view example* removing gate mark. Updated *Table 64: LQFP64 10 x 10 mm, 64-pin low-profile quad flat package mechanical data*. Updated *Section 7.5: UFBGA100 7 x 7 mm, 0.5 mm pitch, ultra thin fine-pitch ball grid array package information* adding *Table 68: UFBGA100 7 x 7 mm, 0.5 mm pitch, recommended PCB design rules* and *Figure 45: UFBGA100 7 x 7 mm, 0.5 mm pitch, package recommended footprint*. Updated *Section 7.6: TFBGA64 5 x 5 mm, 0.5 mm pitch, thin fine-pitch ball grid array package information* adding *Table 70: TFBGA64 5 x 5 mm, 0.5 mm pitch, recommended PCB design rules* and changing *Figure 48: TFBGA64, 5 x 5 mm, 0.5 mm pitch, recommended footprint*. Updated *Table 16: Embedded internal reference voltage* temperature coefficient at 100ppm/°C. Updated note 3 below *Table 16*. Updated *Table 61: Comparator 2 characteristics* new maximum threshold voltage temperature coefficient at 100ppm/°C. Updated *Table 39: ESD absolute maximum ratings* CDM class. Updated all the notes, removing ‘not tested in production’. Updated *Table 10: Voltage characteristics* adding note about V_{REF-} pin. Updated *Table 5: Working mode-dependent functionalities (from Run/active down to standby)* LSI and LSE functionalities putting “Y” in Standby mode. Removed note 1 below *Figure 2: Clock tree*. Updated *Table 57: DAC characteristics* resistive load.