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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, Cap Sense, DMA, I²S, POR, PWM, WDT
Number of I/O	37
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l151cbt6tr

List of tables

2.2 Ultra-low-power device continuum

The ultra-low-power STM32L151x6/8/B and STM32L152x6/8/B devices are fully pin-to-pin and software compatible. Besides the full compatibility within the family, the devices are part of STMicroelectronics microcontrollers ultra-low-power strategy which also includes STM8L101xx and STM8L15xx devices. The STM8L and STM32L families allow a continuum of performance, peripherals, system architecture and features.

They are all based on STMicroelectronics ultra-low leakage process.

Note: The ultra-low-power STM32L and general-purpose STM32Fxxxx families are pin-to-pin compatible. The STM8L15xxx devices are pin-to-pin compatible with the STM8L101xx devices. Please refer to the STM32F and STM8L documentation for more information on these devices.

2.2.1 Performance

All families incorporate highly energy-efficient cores with both Harvard architecture and pipelined execution: advanced STM8 core for STM8L families and ARM® Cortex®-M3 core for STM32L family. In addition specific care for the design architecture has been taken to optimize the mA/DMIPS and mA/MHz ratios.

This allows the ultra-low-power performance to range from 5 up to 33.3 DMIPs.

2.2.2 Shared peripherals

STM8L15xxx and STM32L1xxxx share identical peripherals which ensure a very easy migration from one family to another:

- Analog peripherals: ADC, DAC and comparators
- Digital peripherals: RTC and some communication interfaces

2.2.3 Common system strategy

To offer flexibility and optimize performance, the STM8L15xx and STM32L1xxxx families use a common architecture:

- Same power supply range from 1.65 V to 3.6 V, (1.65 V at power down only for STM8L15xx devices)
- Architecture optimized to reach ultra-low consumption both in low power modes and Run mode
- Fast startup strategy from low power modes
- Flexible system clock
- Ultrasafe reset: same reset strategy including power-on reset, power-down reset, brownout reset and programmable voltage detector.

2.2.4 Features

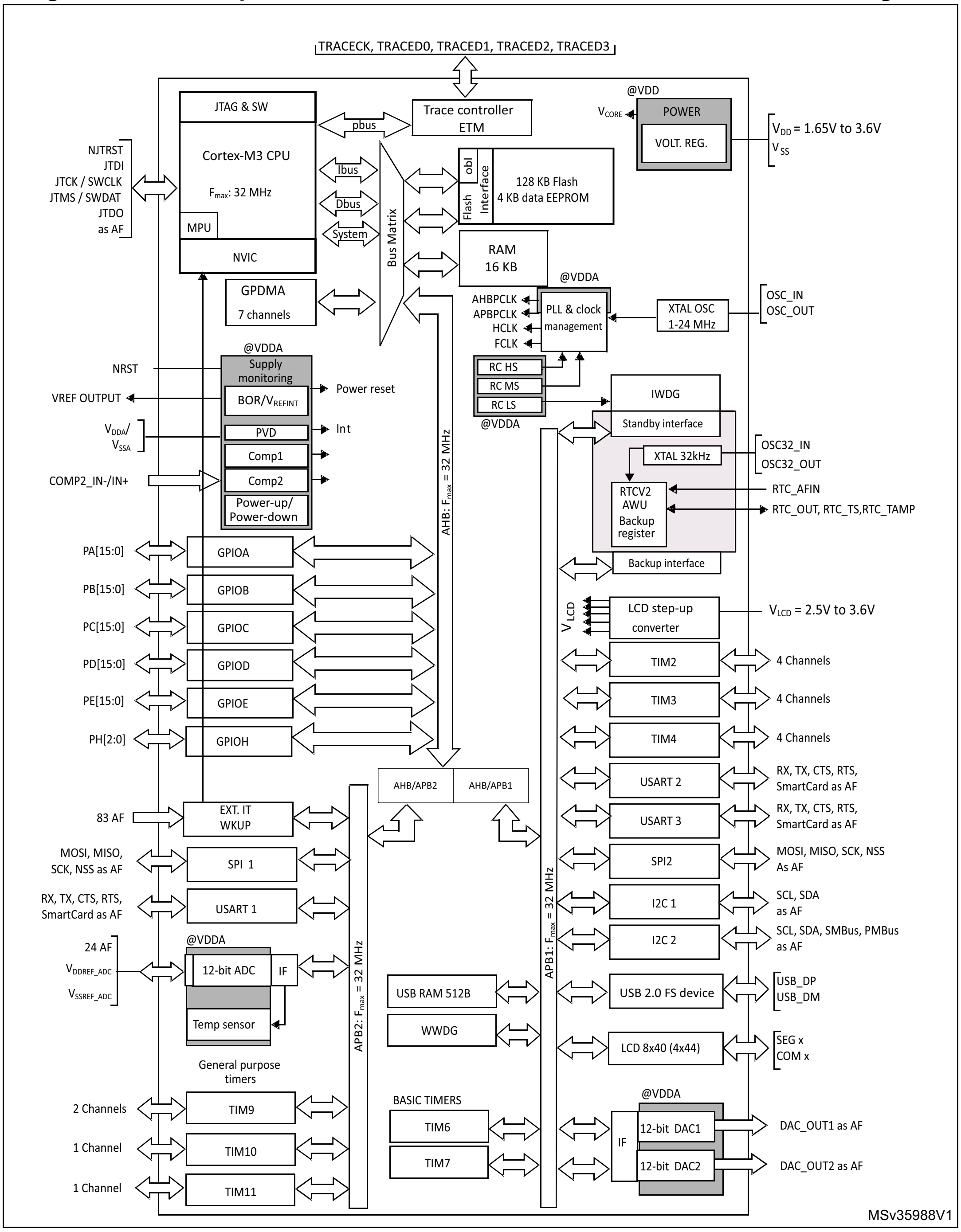
ST ultra-low-power continuum also lies in feature compatibility:

- More than 10 packages with pin count from 20 to 144 pins and size down to 3 x 3 mm
- Memory density ranging from 4 to 384 Kbytes

3 Functional overview

Figure 1 shows the block diagram.

Figure 1. Ultra-low-power STM32L151x6/8/B and STM32L152x6/8/B block diagram



1. AF = alternate function on I/O port pin.

Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Stop mode, it is possible to automatically switch off the internal reference voltage (V_{REFINT}) in Stop mode. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for any external reset circuit.

Note: The start-up time at power-on is typically 3.3 ms when BOR is active at power-up, the start-up time at power-on can be decreased down to 1 ms typically for devices with BOR inactive at power-up.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.3.3 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in Run mode (nominal regulation)
- LPR is used in the Low-power run, Low-power sleep and Stop modes
- Power down is used in Standby mode. The regulator output is high impedance, the kernel circuitry is powered down, inducing zero consumption but the contents of the registers and RAM are lost are lost except for the standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE crystal 32K osc, RCC_CSR).

3.3.4 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from Flash memory
- Boot from System Memory
- Boot from embedded RAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART1 or USART2. See STM32™ microcontroller system memory boot mode AN2606 for details.

3.7 Memories

The STM32L151x6/8/B and STM32L152x6/8/B devices have the following features:

- Up to 16 Kbytes of embedded RAM accessed (read/write) at CPU clock speed with 0 wait states. With the enhanced bus matrix, operating the RAM does not lead to any performance penalty during accesses to the system bus (AHB and APB buses).
- The non-volatile memory is divided into three arrays:
  - 32, 64 or 128 Kbytes of embedded Flash program memory
  - 4 Kbytes of data EEPROM
  - Options bytes

  The options bytes are used to write-protect the memory (with 4 Kbytes granularity) and/or readout-protect the whole memory with the following options:
  - Level 0: no readout protection
  - Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
  - Level 2: chip readout protection, debug features (Cortex®-M3 JTAG and serial wire) and boot in RAM selection disabled (JTAG fuse)

  The whole non-volatile memory embeds the error correction code (ECC) feature.

3.8 DMA (direct memory access)

The flexible 7-channel, general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, general-purpose timers and ADC.

3.9 LCD (liquid crystal display)

The LCD drives up to 8 common terminals and 44 segment terminals to drive up to 320 pixels.

- Internal step-up converter to guarantee functionality and contrast control irrespective of V_{DD}. This converter can be deactivated, in which case the V_{LCD} pin is used to provide the voltage to the LCD
- Supports static, 1/2, 1/3, 1/4 and 1/8 duty
- Supports static, 1/2, 1/3 and 1/4 bias
- Phase inversion to reduce power consumption and EMI
- Up to 8 pixels can be programmed to blink
- Unneeded segments and common pins can be used as general I/O pins
- LCD RAM can be updated at any time owing to a double-buffer
- The LCD controller can operate in Stop mode

3.10 ADC (analog-to-digital converter)

A 12-bit analog-to-digital converters is embedded into STM32L151x6/8/B and STM32L152x6/8/B devices with up to 24 external channels, performing conversions in single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) can be internally connected to the ADC start trigger and injection trigger, to allow the application to synchronize A/D conversions and timers. An injection mode allows high priority conversions to be done by interrupting a scan mode which runs in as a background task.

The ADC includes a specific low power mode. The converter is able to operate at maximum speed even if the CPU is operating at a very low frequency and has an auto-shutdown function. The ADC’s runtime and analog front-end current consumption are thus minimized whatever the MCU operating mode.

3.10.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode, see *Table 58: Temperature sensor calibration values*.

3.10.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and Comparators. V_{REFINT} is internally connected to the ADC_IN17 input channel. It enables accurate monitoring of the V_{DD} value (when no external voltage, VREF+, is available for ADC). The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode see *Table 16: Embedded internal reference voltage*.

3.11 DAC (digital-to-analog converter)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in non-inverting configuration.

6.1.6 Power supply scheme

Figure 12. Power supply scheme

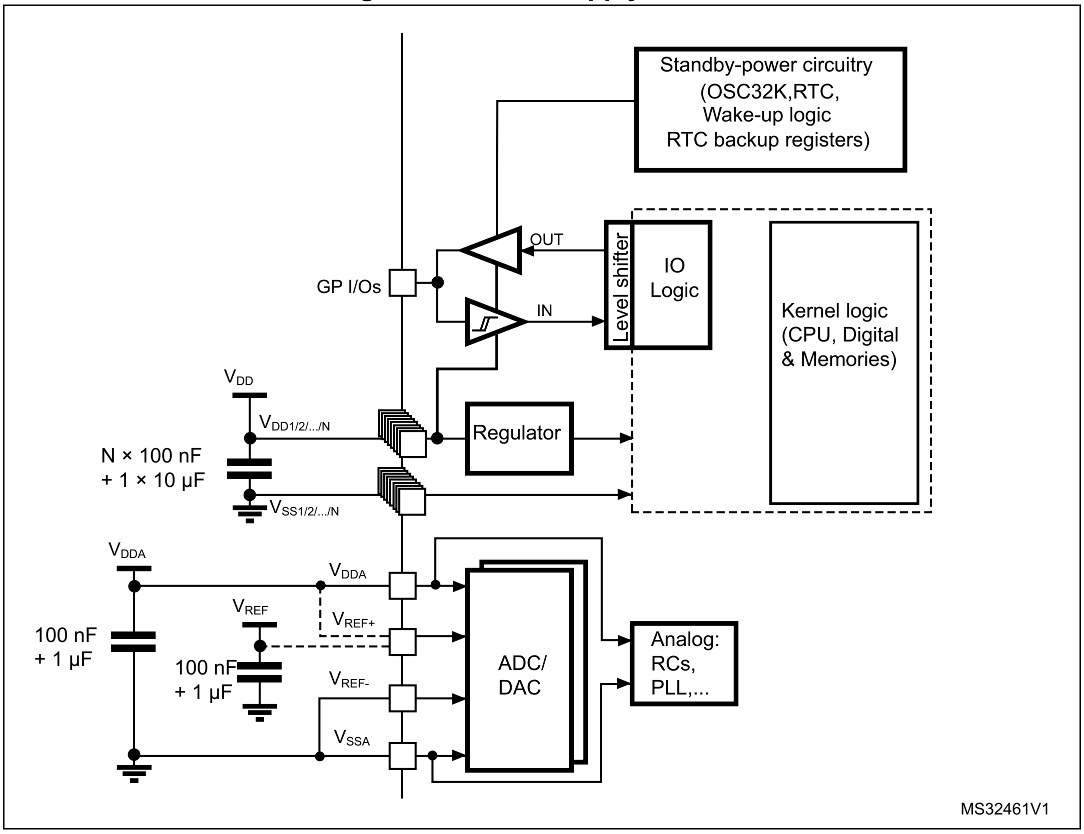


Table 12. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

6.3 Operating conditions

6.3.1 General operating conditions

Table 13. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	32	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	32	
f_{PCLK2}	Internal APB2 clock frequency	-	0	32	
V_{DD}	Standard operating voltage	BOR detector disabled	1.65	3.6	V
		BOR detector enabled, at power on	1.8	3.6	
		BOR detector disabled, after power on	1.65	3.6	
V_{DDA}(1)	Analog operating voltage (ADC and DAC not used)	Must be the same voltage as V_{DD}(2)	1.65	3.6	V
	Analog operating voltage (ADC or DAC used)		1.8	3.6	
V_{IN}	Input voltage on FT pins(3)	$2.0\ V \leq V_{DD} \leq 3.6\ V$	–0.3	5.5	V
		$1.65\ V \leq V_{DD} \leq 2.0\ V$	–0.3	5.25	
	Input voltage on BOOT0 pin		0	5.5	
	Input voltage on any other pin		–0.3	V_{DD}+0.3	
P_D	Power dissipation at T_A = 85 °C(4)	BGA100 package	-	339	mW
T_A	Temperature range	Maximum power dissipation	–40	85	°C
		Low power dissipation(5)	–40	105	
T_J	Junction temperature range	$-40\ °C \leq T_A \leq 105°C$	–40	105	°C

1. When the ADC is used, refer to *Table 54: ADC characteristics*.
2. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and operation.
3. To sustain a voltage higher than V_{DD}+0.3 V, the internal pull-up/pull-down resistors must be disabled.
4. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_J max (see *Table 12: Thermal characteristics on page 53*).
5. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_J max (see *Table 12: Thermal characteristics on page 53*).

Low-speed external user clock generated from an external source

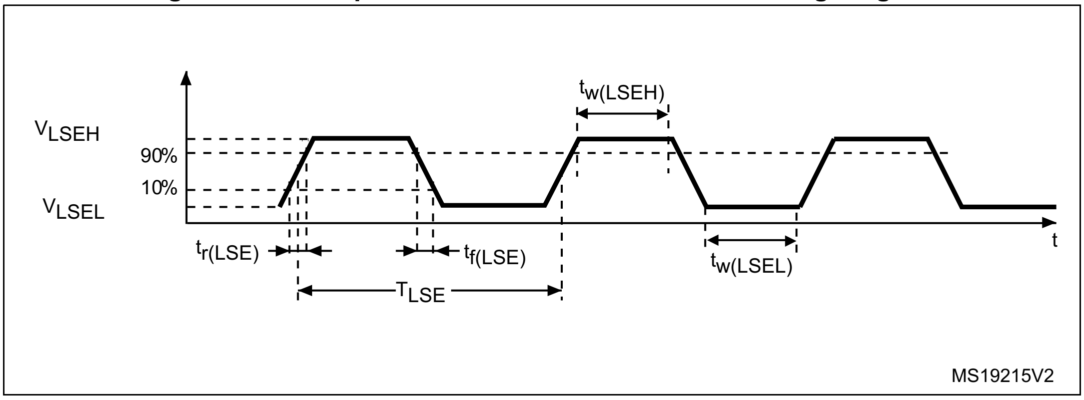
The characteristics given in the following table result from tests performed using a low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in Table 13.

Table 27. Low-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	1	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time		465	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time		-	-	10	
$C_{IN(LSE)}$	OSC32_IN input capacitance	-	-	0.6	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	45	-	55	%
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design.

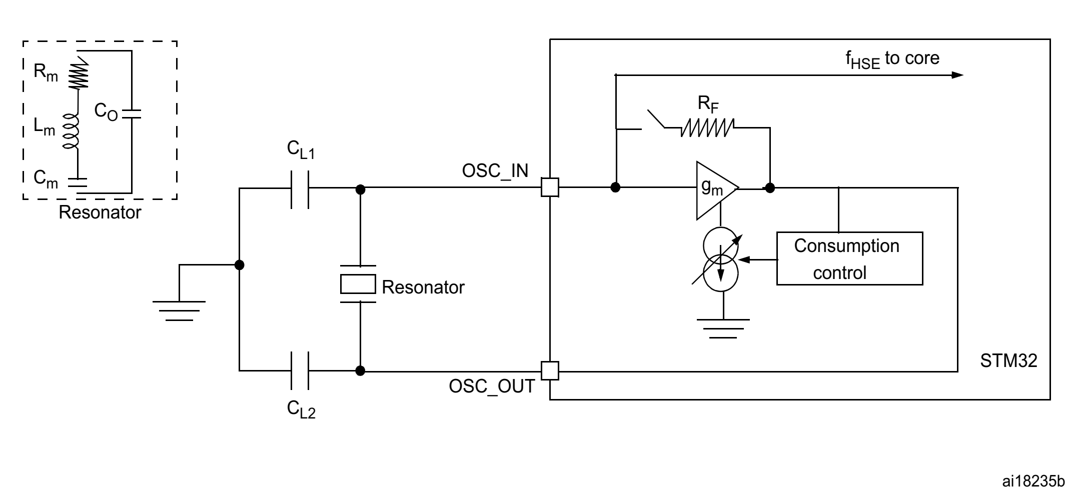
Figure 16. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 1 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in Table 28. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Figure 17. HSE oscillator circuit diagram



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 29*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 29. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE}	Low speed external oscillator frequency	-	-	32.768	-	kHz
R_F	Feedback resistor	-	-	1.2	-	MΩ
C(2)	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(3)	R_S = 30 kΩ	-	8	-	pF
I_{LSE}	LSE driving current	V_{DD} = 3.3 V, V_{IN} = V_{SS}	-	-	1.1	µA
$I_{DD\ (LSE)}$	LSE oscillator current consumption	V_{DD} = 1.8 V	-	450	-	nA
		V_{DD} = 3.0 V	-	600	-	
		V_{DD} = 3.6V	-	750	-	
g_m	Oscillator transconductance	-	3	-	-	µA/V
$t_{SU(LSE)}$(4)	Startup time	V_{DD} is stabilized	-	1	-	s

1. Guaranteed by characterization results.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
3. The oscillator selection can be optimized in terms of supply current using an high quality resonator with small R_S value for example MSIV-TIN32.768kHz. Refer to crystal manufacturer for more details.

6.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 37*. They are based on the EMS levels and classes defined in application note AN1709.

Table 37. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25 °C, f_{HCLK} = 32 MHz conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25 °C, f_{HCLK} = 32 MHz conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the oscillator pins for 1 second.

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with the non-standard V_{OL}/V_{OH} specifications given in *Table 43*.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating $I_{VDD\Sigma}$ (see *Table 11*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating $I_{VSS\Sigma}$ (see *Table 11*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 43* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 13*. All I/Os are CMOS and TTL compliant.

Table 43. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL} (1)(2)	Output low level voltage for an I/O pin	I_{IO} = 8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH} (3)(2)	Output high level voltage for an I/O pin		2.4	-	
V_{OL} (1)(4)	Output low level voltage for an I/O pin	I_{IO} = 4 mA 1.65 V < V_{DD} < 2.7 V	-	0.45	
V_{OH} (3)(4)	Output high level voltage for an I/O pin		V_{DD}-0.45	-	
V_{OL} (1)(4)	Output low level voltage for an I/O pin	I_{IO} = 20 mA 2.7 V < V_{DD} < 3.6 V	-	1.3	
V_{OH} (3)(4)	Output high level voltage for an I/O pin		V_{DD}-1.3	-	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 11* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. Tested in production.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 11* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
4. Guaranteed by characterization results.

6.3.20 Comparator

Table 60. Comparator 1 characteristics

Symbol	Parameter	Conditions	Min[1]	Typ	Max[1]	Unit
V_{DDA}	Analog supply voltage	-	1.65		3.6	V
R_{400K}	R_{400K} value	-	-	400	-	kΩ
R_{10K}	R_{10K} value	-	-	10	-	kΩ
V_{IN}	Comparator 1 input voltage range	-	0.6	-	V_{DDA}	V
t_{START}	Comparator startup time	-	-	7	10	µs
td	Propagation delay[2]	-	-	3	10	µs
Voffset	Comparator offset	-	-	±3	±10	mV
$d_{Voffset}/dt$	Comparator offset variation in worst voltage stress conditions	$V_{DDA} = 3.6$ V $V_{IN+} = 0$ V $V_{IN-} = V_{REFINT}$ $T_A = 25\ °C$	0	1.5	10	mV/1000 h
I_{COMP1}	Current consumption[3]	-	-	160	260	nA

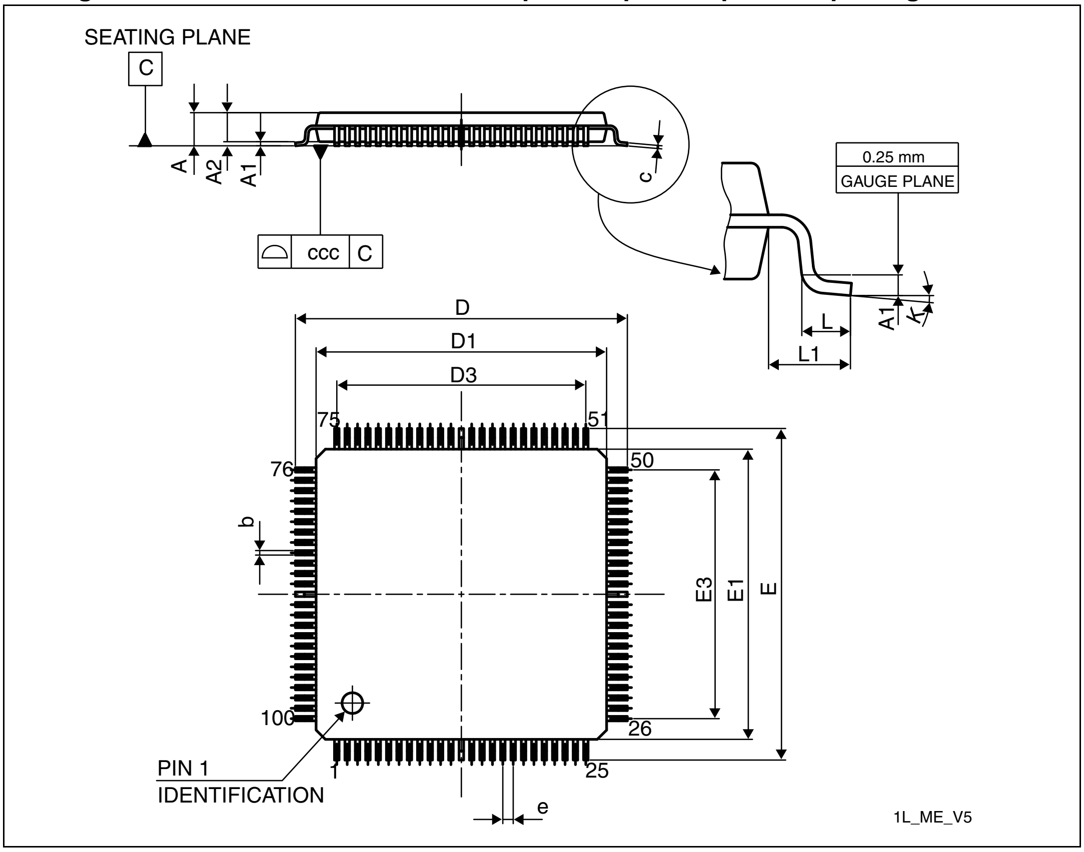
1. Guaranteed by characterization results.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage not included.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.1 LQFP100 14 x 14 mm, 100-pin low-profile quad flat package information

Figure 32. LQFP100 14 x 14 mm, 100-pin low-profile quad flat package outline



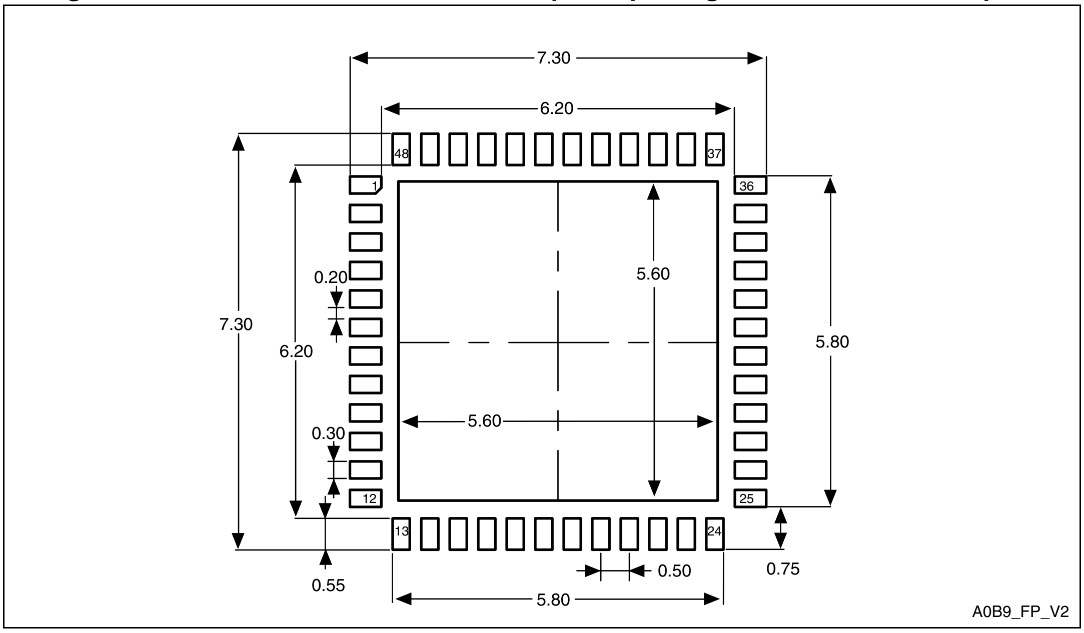
1. Drawing is not to scale.

Table 66. UFQFPN48 7 x 7 mm, 0.5 mm pitch, package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 42. UFQFPN48 7 x 7 mm, 0.5 mm pitch, package recommended footprint



1. Dimensions are in millimeters.

Table 69. TFBGA64 5 x 5 mm, 0.5 mm pitch, package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
eee	-	-	0.15	-	-	0.0059
fff	-	-	0.05	-	-	0.002

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 48. TFBGA64, 5 x 5 mm, 0.5 mm pitch, recommended footprint

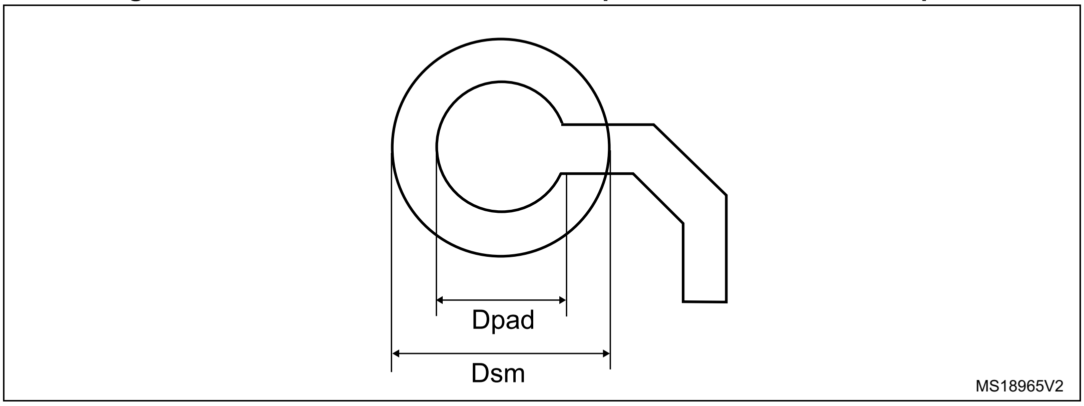


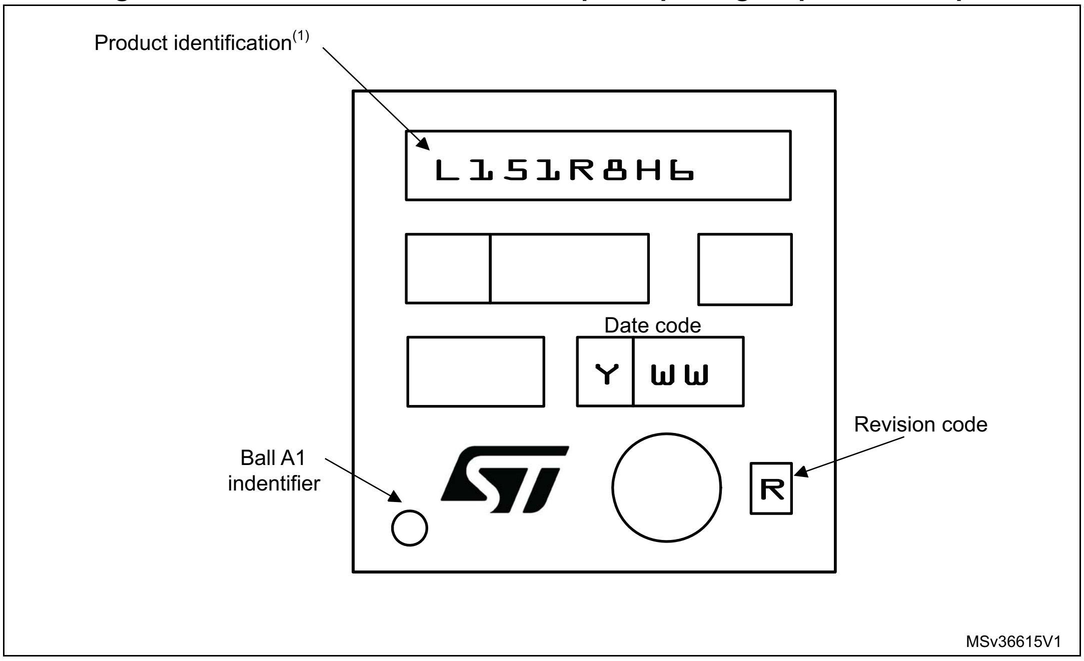
Table 70. TFBGA64 5 x 5 mm, 0.5 mm pitch, recommended PCB design rules

Dimension	Recommended values
Pitch	0.5
Dpad	0.27 mm
Dsm	0.35 mm typ. (depends on the soldermask registration tolerance)
Solder paste	0.27 mm aperture diameter.

TFBGA64 device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Figure 49. TFBGA64 5 x 5 mm, 0.5 mm pitch, package top view example



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 73. Document revision history (continued)

Date	Revision	Changes
17-June-2011	5	Modified 1st page (low power features) Added STM32L15xC6 and STM32L15xR6 devices (32 Kbytes of Flash memory). Modified *Section 3.6: GPIOs (general-purpose inputs/outputs) on page 22* Modified *Section 6.3: Operating conditions on page 53* Modified *Table 55: ADC accuracy on page 95*, *Table 57: DAC characteristics on page 99* and *Table 60: Comparator 1 characteristics on page 102*
25-Jan-2012	6	*Features*: updated internal multispeed low power RC. *Table 2: Ultralow power STM32L15xx6/8/B device features and peripheral counts*: LCD 4x44 and 8x40 available for both 64- and 128-Kbyte devices; two comparators available for all devices. *Table 3: Functionalities depending on the operating power supply range*: added footnote *1*. *Figure 8: STM32L15xCx UFQFPN48 pinout*: replaced VFQPN48 by UFQFPN48 as name of package. *Table 8: STM32L15xx6/8/B pin definitions*: replaced PH0/PH1 by PC14/PC15. *Table 9: Alternate function input/output*: removed EVENT OUT from PH2 port, AFIO15 column. *Table 19: Current consumption in Sleep mode*: updated MSI conditions and f_{HCLK}. *Table 20: Current consumption in Low power run mode*: updated some temperature conditions; added footnote *2*. *Table 21: Current consumption in Low power sleep mode*: updated some temperature conditions and one of the MSI clock conditions. *Table 22: Typical and maximum current consumptions in Stop mode*: updated I_{DD} (WU from Stop) parameter. *Table 23: Typical and maximum current consumptions in Standby mode*: updated I_{DD} (WU from Standby) parameter. *Table 25: Low-power mode wakeup timings*: updated f_{HCLK} value for $t_{WUSLEEP\_LP}$; updated typical value of parameter “Wakeup from Stop mode, regulator in Run mode”. *Table 24: Peripheral current consumption*: replaced GPIOF by GPIOH. *Table 33: PLL characteristics*: updated “PLL output clock” *Table 35: Flash memory and data EEPROM characteristics*: updated all information for I_{DD}. *Figure 19: I/O AC characteristics definition*: replaced the falling edge “$t_{r(IO)out}$” by “$t_{f(IO)out}$”. *Table 47: I2C characteristics*: amended footnote *2*. *Table 54: ADC characteristics*: updated f_S max value for direct channels, 6-bit sampling rate. *Table 55: ADC accuracy*: Updated the first, third and fourth f_{ADC} test condition. *Table 59: Temperature sensor characteristics*: updated typ, min, and max values of the T_{S_temp} parameter.

Table 73. Document revision history (continued)

Date	Revision	Changes
12-Nov-2013	9 (continued)	Updated *Table 54: ADC characteristics* and *Figure 27: Typical connection diagram using the ADC*. *Table 58: Temperature sensor calibration values* was previously in *Section 3.10.1: Temperature sensor*. Updated *Table 59: Temperature sensor characteristics*. In *Table 61: Comparator 2 characteristics*, parameter dThreshold/dt, replaced any occurrence of “VREF+” by “V_{REFINT}”Updated *Table 63: LQPF100 14 x 14 mm, 100-pin low-profile quad flat package mechanical data*, *Table 64: LQFP64 10 x 10 mm 64-pin low-profile quad flat package mechanical data*, *Table 65: LQFP48 7 x 7 mm, 48-pin low-profile quad flat package mechanical data* and *Table 66: UFQFPN48 7 x 7 mm, 0.5 mm pitch, ultra thin fine-pitch quad flat no-lead package mechanical data*. Updated *Figure 33: LQFP100 recommended footprint*. Updated *Figure 46: TFBGA64 - 5.0x5.0x1.2 mm, 0.5 mm pitch, thin fine-pitch ball grid array package outline* title. Remove minimum and typical values of A dimension in *Table 67: UFBGA100 7 x 7 x 0.6 mm 0.5 mm pitch, ultra thin fine-pitch ball grid array package mechanical data* Deleted second footnote in *Figure 42: UFQFPN48 recommended footprint*. Updated *Section 8: Ordering information* title and added first sentence. Changed BOR disabled option identifier in *Table 72: Ordering information scheme*.
22-Jul-2014	10	Updated *Figure 14*, *Figure 15*. Updated *Table 5*. Updated *Figure 6.3.4*. Updated note *5* inside *Table 54*. Updated Ro value inside *Table 54*.