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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Cap Sense, DMA, I²S, POR, PWM, WDT
Number of I/O	37
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UFQFPN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l151cbu6d

Contents

2.2 Ultra-low-power device continuum

The ultra-low-power STM32L151x6/8/B and STM32L152x6/8/B devices are fully pin-to-pin and software compatible. Besides the full compatibility within the family, the devices are part of STMicroelectronics microcontrollers ultra-low-power strategy which also includes STM8L101xx and STM8L15xx devices. The STM8L and STM32L families allow a continuum of performance, peripherals, system architecture and features.

They are all based on STMicroelectronics ultra-low leakage process.

Note: The ultra-low-power STM32L and general-purpose STM32Fxxxx families are pin-to-pin compatible. The STM8L15xxx devices are pin-to-pin compatible with the STM8L101xx devices. Please refer to the STM32F and STM8L documentation for more information on these devices.

2.2.1 Performance

All families incorporate highly energy-efficient cores with both Harvard architecture and pipelined execution: advanced STM8 core for STM8L families and ARM® Cortex®-M3 core for STM32L family. In addition specific care for the design architecture has been taken to optimize the mA/DMIPS and mA/MHz ratios.

This allows the ultra-low-power performance to range from 5 up to 33.3 DMIPs.

2.2.2 Shared peripherals

STM8L15xxx and STM32L1xxxx share identical peripherals which ensure a very easy migration from one family to another:

- Analog peripherals: ADC, DAC and comparators
- Digital peripherals: RTC and some communication interfaces

2.2.3 Common system strategy

To offer flexibility and optimize performance, the STM8L15xx and STM32L1xxxx families use a common architecture:

- Same power supply range from 1.65 V to 3.6 V, (1.65 V at power down only for STM8L15xx devices)
- Architecture optimized to reach ultra-low consumption both in low power modes and Run mode
- Fast startup strategy from low power modes
- Flexible system clock
- Ultrasafe reset: same reset strategy including power-on reset, power-down reset, brownout reset and programmable voltage detector.

2.2.4 Features

ST ultra-low-power continuum also lies in feature compatibility:

- More than 10 packages with pin count from 20 to 144 pins and size down to 3 x 3 mm
- Memory density ranging from 4 to 384 Kbytes

Table 5. Working mode-dependent functionalities (from Run/active down to standby) (continued)

Ips	Run/Active	Sleep	Low-power Run	Low-power Sleep	Stop		Standby	
						Wakeup capability		Wakeup capability
DAC	Y	Y	Y	Y	Y	-	-	-
Temperature sensor	Y	Y	Y	Y	Y	-	-	-
Comparators	Y	Y	Y	Y	Y	Y	-	-
16-bit and 32-bit Timers	Y	Y	Y	Y	-	-	-	-
IWDG	Y	Y	Y	Y	Y	Y	Y	Y
WWDG	Y	Y	Y	Y	-	-	-	-
Touch sensing	Y	-	-	-	-	-	-	-
Systick Timer	Y	Y	Y	Y	-	-	-	-
GPIOs	Y	Y	Y	Y	Y	Y	-	3 Pins
Wakeup time to Run mode	0 µs	0.36 µs	3 µs	32 µs	< 8 µs		50 µs	
Consumption V_{DD}=1.8V to 3.6V (Typ)	Down to 214 µA/MHz (from Flash)	Down to 50 µA/MHz (from Flash)	Down to 9 µA	Down to 4.4 µA	0.5 µA (No RTC) V_{DD}=1.8V		0.3 µA (No RTC) V_{DD}=1.8V	
					1.4 µA (with RTC) V_{DD}=1.8V		1 µA (with RTC) V_{DD}=1.8V	
					0.5 µA (No RTC) V_{DD}=3.0V		0.3 µA (No RTC) V_{DD}=3.0V	
					1.6 µA (with RTC) V_{DD}=3.0V		1.3 µA (with RTC) V_{DD}=3.0V	

1. The startup on communication line wakes the CPU which was made possible by an EXTI, this induces a delay before entering run mode.

3.2 ARM® Cortex®-M3 core with MPU

The ARM® Cortex®-M3 processor is the industry leading processor for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM® Cortex®-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The memory protection unit (MPU) improves system reliability by defining the memory attributes (such as read/write access permissions) for different memory regions. It provides up to eight different regions and an optional predefined background region.

Owing to its embedded ARM core, the STM32L151x6/8/B and STM32L152x6/8/B devices are compatible with all ARM tools and software.

Table 8. STM32L151x6/8/B and STM32L152x6/8/B pin definitions (continued)

Pins					Pin name	Pin type(1)	I/O structure	Main function(2) (after reset)	Pins functions	
LQFP100	LQFP64	TFBGA64	UFBGA100	LQFP48 or UFQFPN48					Alternate functions	Additional functions
35	26	F5	M5	18	PB0	I/O	TC	PB0	TIM3_CH3/LCD_SEG5	ADC_IN8/ COMP1_INP/ VREF_OUT
36	27	G5	M6	19	PB1	I/O	FT	PB1	TIM3_CH4/LCD_SEG6	ADC_IN9/ COMP1_INP/ VREF_OUT
37	28	G6	L6	20	PB2	I/O	FT	PB2/BOOT1	BOOT1	-
38	-	-	M7	-	PE7	I/O	TC	PE7	-	ADC_IN22/ COMP1_INP
39	-	-	L7	-	PE8	I/O	TC	PE8	-	ADC_IN23/ COMP1_INP
40	-	-	M8	-	PE9	I/O	TC	PE9	TIM2_CH1_ETR	ADC_IN24/ COMP1_INP
41	-	-	L8	-	PE10	I/O	TC	PE10	TIM2_CH2	ADC_IN25/ COMP1_INP
42	-	-	M9	-	PE11	I/O	FT	PE11	TIM2_CH3	-
43	-	-	L9	-	PE12	I/O	FT	PE12	TIM2_CH4/SPI1_NSS	-
44	-	-	M10	-	PE13	I/O	FT	PE13	SPI1_SCK	-
45	-	-	M11	-	PE14	I/O	FT	PE14	SPI1_MISO	-
46	-	-	M12	-	PE15	I/O	FT	PE15	SPI1_MOSI	-
47	29	G7	L10	21	PB10	I/O	FT	PB10	I2C2_SCL/USART3_TX/ TIM2_CH3/LCD_SEG10	-
48	30	H7	L11	22	PB11	I/O	FT	PB11	I2C2_SDA/USART3_RX/ TIM2_CH4/LCD_SEG11	-
49	31	D6	F12	23	V_{SS_1}	S	-	V_{SS_1}	-	-
50	32	E6	G12	24	V_{DD_1}	S	-	V_{DD_1}	-	-
51	33	H8	L12	25	PB12	I/O	FT	PB12	SPI2_NSS/I2C2_SMBA/ USART3_CK/ LCD_SEG12/TIM10_CH1	ADC_IN18/ COMP1_INP
52	34	G8	K12	26	PB13	I/O	FT	PB13	SPI2_SCK/USART3_CTS/ LCD_SEG13/ TIM9_CH1	ADC_IN19/ COMP1_INP

Table 8. STM32L151x6/8/B and STM32L152x6/8/B pin definitions (continued)

Pins					Pin name	Pin type[1]	I/O structure	Main function[2] (after reset)	Pins functions	
LQFP100	LQFP64	TFBGA64	UFBGA100	LQFP48 or UFQFPN48					Alternate functions	Additional functions
53	35	F8	K11	27	PB14	I/O	FT	PB14	SPI2_MISO/ USART3_RTS/ LCD_SEG14//TIM9_CH2	ADC_IN20/ COMP1_INP
54	36	F7	K10	28	PB15	I/O	FT	PB15	SPI2_MOSI/LCD_SEG15/ TIM11_CH1	ADC_IN21/ COMP1_INP/ RTC_REFIN
55	-	-	K9	-	PD8	I/O	FT	PD8	USART3_TX/ LCD_SEG28	-
56	-	-	K8	-	PD9	I/O	FT	PD9	USART3_RX/ LCD_SEG29	-
57	-	-	J12	-	PD10	I/O	FT	PD10	USART3_CK/ LCD_SEG30	-
58	-	-	J11	-	PD11	I/O	FT	PD11	USART3_CTS/ LCD_SEG31	-
59	-	-	J10	-	PD12	I/O	FT	PD12	TIM4_CH1/ USART3_RTS/ LCD_SEG32	-
60	-	-	H12	-	PD13	I/O	FT	PD13	TIM4_CH2/LCD_SEG33	-
61	-	-	H11	-	PD14	I/O	FT	PD14	TIM4_CH3/LCD_SEG34	-
62	-	-	H10	-	PD15	I/O	FT	PD15	TIM4_CH4/LCD_SEG35	-
63	37	F6	E12	-	PC6	I/O	FT	PC6	TIM3_CH1/LCD_SEG24	-
64	38	E7	E11	-	PC7	I/O	FT	PC7	TIM3_CH2/LCD_SEG25	-
65	39	E8	E10	-	PC8	I/O	FT	PC8	TIM3_CH3/LCD_SEG26	-
66	40	D8	D12	-	PC9	I/O	FT	PC9	TIM3_CH4/LCD_SEG27	-
67	41	D7	D11	29	PA8	I/O	FT	PA8	USART1_CK/MCO/ LCD_COM0	-
68	42	C7	D10	30	PA9	I/O	FT	PA9	USART1_TX/LCD_COM1	-
69	43	C6	C12	31	PA10	I/O	FT	PA10	USART1_RX/LCD_COM2	-
70	44	C8	B12	32	PA11	I/O	FT	PA11	USART1_CTS/ SPI1_MISO	USB_DM

Table 9. Alternate function input/output (continued)

Port name	Digital alternate function number														
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFOI6	AFIO7	AFIO8	AFIO9	AFIO11	AFIO12	AFIO13	AFIO14	AFIO15
	Alternate function														
	SYSTEM	TIM2	TIM3/4	TIM9/10/11	I2C1/2	SPI1/2	N/A	USART1/2/3	N/A	N/A	LCD	N/A	N/A	RI	SYSTEM
PB5	-	-	TIM3_CH2	-	I2C1_ SMBA	SPI1_MOSI	-	-	-	-	[SEG9]	-	-	-	EVENTOUT
PB6	-	-	TIM4_CH1	-	I2C1_SCL	-	-	USART1_TX	-	-	-	-	-	-	EVENTOUT
PB7	-	-	TIM4_CH2	-	I2C1_SDA	-	-	USART1_RX	-	-	-	-	-	-	EVENTOUT
PB8	-	-	TIM4_CH3	TIM10_CH1*	I2C1_SCL	-	-	-	-	-	SEG16	-	-	-	EVENTOUT
PB9	-	-	TIM4_CH4	TIM11_CH1*	I2C1_SDA	-	-	-	-	-	[COM3]	-	-	-	EVENTOUT
PB10	-	TIM2_CH3	-	-	I2C2_SCL	-	-	USART3_TX	-	-	SEG10	-	-	-	EVENTOUT
PB11	-	TIM2_CH4	-	-	I2C2_SDA	-	-	USART3_RX	-	-	SEG11	-	-	-	EVENTOUT
PB12	-	-	-	TIM10_CH1	I2C2_ SMBA	SPI2_NSS	-	USART3_CK	-	-	SEG12	-	-	-	EVENTOUT
PB13	-	-	-	TIM9_CH1	-	SPI2_SCK	-	USART3_CTS	-	-	SEG13	-	-	-	EVENTOUT
PB14	-	-	-	TIM9_CH2	-	SPI2_MISO	-	USART3_RTS	-	-	SEG14	-	-	-	EVENTOUT
PB15	-	-	-	TIM11_CH1	-	SPI2_MOSI	-	-	-	-	SEG15	-	-	-	EVENTOUT
PC0	-	-	-	-	-	-	-	-	-	-	SEG18	-	-	TIMx_IC1	EVENTOUT
PC1	-	-	-	-	-	-	-	-	-	-	SEG19	-	-	TIMx_IC2	EVENTOUT
PC2	-	-	-	-	-	-	-	-	-	-	SEG20	-	-	TIMx_IC3	EVENTOUT
PC3	-	-	-	-	-	-	-	-	-	-	SEG21	-	-	TIMx_IC4	EVENTOUT
PC4	-	-	-	-	-	-	-	-	-	-	SEG22	-	-	TIMx_IC1	EVENTOUT
PC5	-	-	-	-	-	-	-	-	-	-	SEG23	-	-	TIMx_IC2	EVENTOUT
PC6	-	-	TIM3_CH1	-	-	-	-	-	-	-	SEG24	-	-	TIMx_IC3	EVENTOUT
PC7	-	-	TIM3_CH2	-	-	-	-	-	-	-	SEG25	-	-	TIMx_IC4	EVENTOUT
PC8	-	-	TIM3_CH3	-	-	-	-	-	-	-	SEG26	-	-	TIMx_IC1	EVENTOUT
PC9	-	-	TIM3_CH4	-	-	-	-	-	-	-	SEG27	-	-	TIMx_IC2	EVENTOUT
PC10	-	-	-	-	-	-	-	USART3_TX	-	-	COM4 / SEG28 / SEG40	-	-	TIMx_IC3	EVENTOUT

6.1.6 Power supply scheme

Figure 12. Power supply scheme

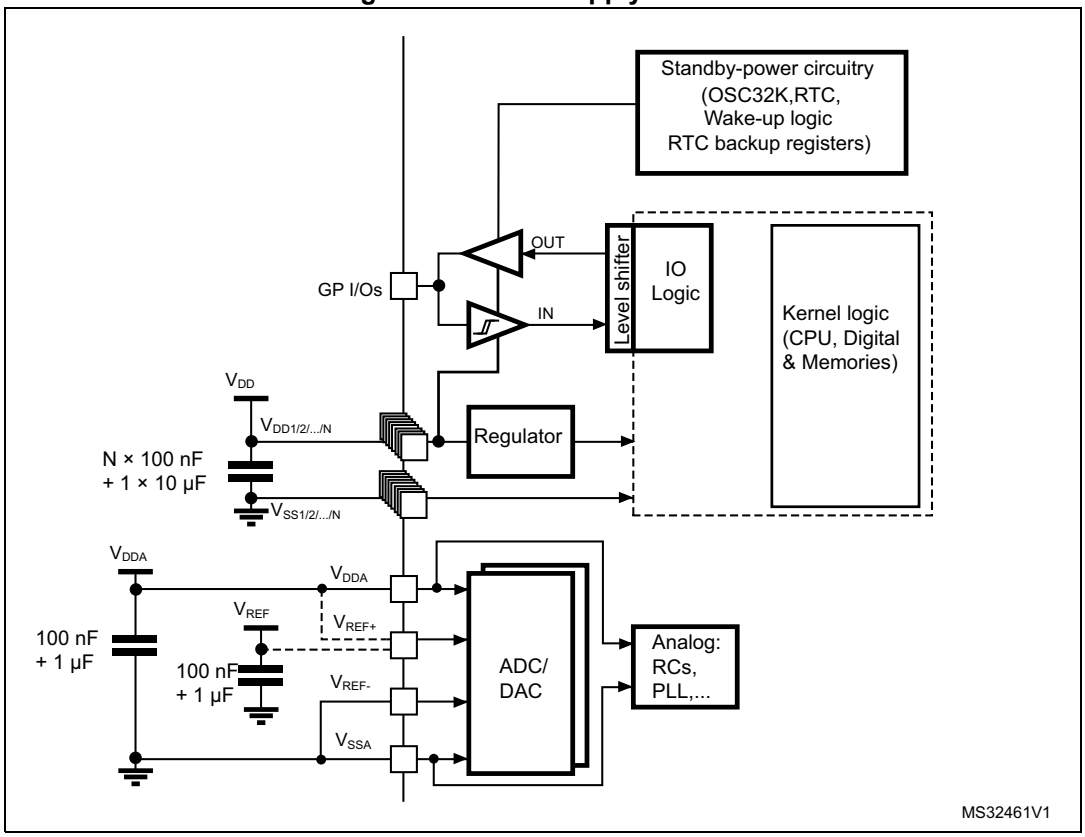


Table 17. Current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max(1)			Unit
						55 °C	85 °C	105 °C	
I_{DD} (Run from Flash)	Supply current in Run mode, code executed from Flash	$f_{HSE} = f_{HCLK}$ up to 16 MHz, included $f_{HSE} = f_{HCLK}/2$ above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	1 MHz	270	400	400	400	µA
				2 MHz	470	600	600	600	
				4 MHz	890	1025	1025	1025	
			Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	4 MHz	1	1.3	1.3	1.3	mA
				8 MHz	2	2.5	2.5	2.5	
				16 MHz	3.9	5	5	5	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	8 MHz	2.16	3	3	3	
				16 MHz	4.8	5.5	5.5	5.5	
				32 MHz	9.6	11	11	11	
		HSI clock source (16 MHz)	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	16 MHz	4	5	5	5	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	32 MHz	9.4	11	11	11	
		MSI clock, 65 kHz	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	65 kHz	0.05	0.085	0.09	0.1	
		MSI clock, 524 kHz		524 kHz	0.15	0.185	0.19	0.2	
		MSI clock, 4.2 MHz		4.2 MHz	0.9	1	1	1	

1. Guaranteed by characterization results, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 19. Current consumption in Sleep mode

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max(1)			Unit
						55 °C	85 °C	105 °C	
I_{DD} (Sleep)	Supply current in Sleep mode, code executed from RAM, Flash switched OFF	f_{HSE} = f_{HCLK} up to 16 MHz included, f_{HSE} = f_{HCLK}/2 above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	1 MHz	80	140	140	140	µA
				2 MHz	150	210	210	210	
				4 MHz	280	330	330	330(3)	
			Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	4 MHz	280	400	400	400	
				8 MHz	450	550	550	550	
				16 MHz	900	1050	1050	1050	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	8 MHz	550	650	650	650	
				16 MHz	1050	1200	1200	1200	
				32 MHz	2300	2500	2500	2500	
		HSI clock source (16 MHz)	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	16 MHz	1000	1100	1100	1100	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	32 MHz	2300	2500	2500	2500	
		MSI clock, 65 kHz	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	65 kHz	30	50	50	60	
		MSI clock, 524 kHz		524 kHz	50	70	70	80	
		MSI clock, 4.2 MHz		4.2 MHz	200	240	240	250	
	Supply current in Sleep mode, code executed from Flash	f_{HSE} = f_{HCLK} up to 16 MHz included, f_{HSE} = f_{HCLK}/2 above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	1 MHz	80	140	140	140	µA
				2 MHz	150	210	210	210	
				4 MHz	290	350	350	350	
			Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	4 MHz	300	400	400	400	
				8 MHz	500	600	600	600	
				16 MHz	1000	1100	1100	1100	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	8 MHz	550	650	650	650	
				16 MHz	1050	1200	1200	1200	
				32 MHz	2300	2500	2500	2500	
		HSI clock source (16 MHz)	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	16 MHz	1000	1100	1100	1100	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	32 MHz	2300	2500	2500	2500	

Table 24. Peripheral current consumption(1) (continued)

Peripheral		Typical consumption, V_{DD} = 3.0 V, T_A = 25 °C				Unit
		Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	Low power sleep and run	
AHB	GPIOA	5	4.5	3.5	4	µA/MHz (f_{HCLK})
	GPIOB	5	4.5	3.5	4.5	
	GPIOC	5	4.5	3.5	4.5	
	GPIOD	5	4.5	3.5	4.5	
	GPIOE	5	4.5	3.5	4.5	
	GPIOH	4	4	3	3.5	
	CRC	1	0.5	0.5	0.5	
	FLASH	13	11.5	9	18.5	
	DMA1	12	10	8	10.5	
All enabled		166	138	106	130	
$I_{DD\ (RTC)}$		0.47				µA
$I_{DD\ (LCD)}$		3.1				
$I_{DD\ (ADC)}$(3)		1450				
$I_{DD\ (DAC)}$(4)		340				
$I_{DD\ (COMP1)}$		0.16				
$I_{DD\ (COMP2)}$	Slow mode	2				
	Fast mode	5				
$I_{DD\ (PVD\ /\ BOR)}$(5)		2.6				
$I_{DD\ (IWDG)}$		0.25				

1. Data based on differential I_{DD} measurement between all peripherals OFF an one peripheral with clock enabled, in the following conditions: f_{HCLK} = 32 MHz (Range 1), f_{HCLK} = 16 MHz (Range 2), f_{HCLK} = 4 MHz (Range 3), f_{HCLK} = 64kHz (Low power run/sleep), $f_{APB1} = f_{HCLK}$, $f_{APB2} = f_{HCLK}$, default prescaler value for each peripheral. The CPU is in Sleep mode in both cases. No I/O pins toggling.
2. HSI oscillator is OFF for this measure.
3. Data based on a differential I_{DD} measurement between ADC in reset configuration and continuous ADC conversion (HSI consumption not included).
4. Data based on a differential I_{DD} measurement between DAC in reset configuration and continuous DAC conversion of V_{DD}/2. DAC is in buffered mode, output is left floating.
5. Including supply current of internal reference voltage.

6.3.6 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO. The external clock signal has to respect the I/O characteristics in *Section 6.3.13*. However, the recommended clock input waveform is shown in *Figure 15: High-speed external clock source AC timing diagram*.

Table 26. High-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	CSS is on or PLL is used	1	8	32	MHz
		CSS is off, PLL not used	0			
V_{HSEH}	OSC_IN input pin high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time		12	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time		-	-	20	
$C_{in(HSE)}$	OSC_IN input capacitance	-	-	2.6	-	pF
$DuCy_{(HSE)}$	Duty cycle	-	45	-	55	%
I_L	OSC_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design.

Figure 15. High-speed external clock source AC timing diagram

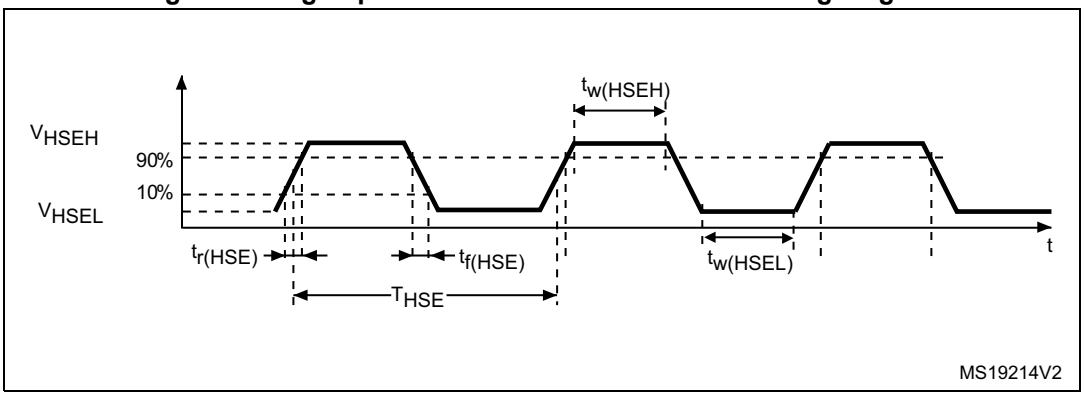


Table 28. HSE oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	1		24	MHz
R_F	Feedback resistor	-		200	-	kΩ
C	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(3)	R_S = 30 Ω	-	20	-	pF
I_{HSE}	HSE driving current	V_{DD}= 3.3 V, V_{IN} = V_{SS} with 30 pF load	-	-	3	mA
$I_{DD(HSE)}$	HSE oscillator power consumption	C = 20 pF f_{OSC} = 16 MHz	-	-	2.5 (startup) 0.7 (stabilized)	mA
		C = 10 pF f_{OSC} = 16 MHz	-	-	2.5 (startup) 0.46 (stabilized)	
g_m	Oscillator transconductance	Startup	3.5	-	-	mA /V
$t_{SU(HSE)}$ (4)	Startup time	V_{DD} is stabilized	-	1	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by characterization results.
3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 17*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}. Refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website *www.st.com*.

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with the non-standard V_{OL}/V_{OH} specifications given in *Table 43*.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating $I_{VDD\Sigma}$ (see *Table 11*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating $I_{VSS\Sigma}$ (see *Table 11*).

Output voltage levels

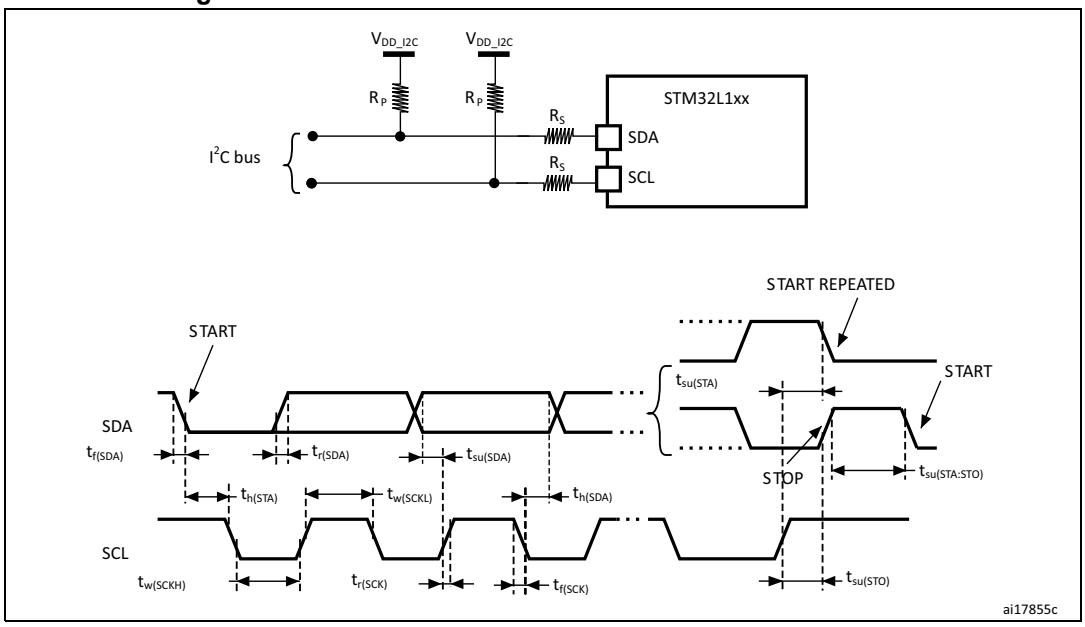
Unless otherwise specified, the parameters given in *Table 43* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 13*. All I/Os are CMOS and TTL compliant.

Table 43. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL} (1)(2)	Output low level voltage for an I/O pin	I_{IO} = 8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH} (3)(2)	Output high level voltage for an I/O pin		2.4	-	
V_{OL} (1)(4)	Output low level voltage for an I/O pin	I_{IO} = 4 mA 1.65 V < V_{DD} < 2.7 V	-	0.45	
V_{OH} (3)(4)	Output high level voltage for an I/O pin		V_{DD}-0.45	-	
V_{OL} (1)(4)	Output low level voltage for an I/O pin	I_{IO} = 20 mA 2.7 V < V_{DD} < 3.6 V	-	1.3	
V_{OH} (3)(4)	Output high level voltage for an I/O pin		V_{DD}-1.3	-	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 11* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. Tested in production.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 11* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
4. Guaranteed by characterization results.

Figure 21. I²C bus AC waveforms and measurement circuit



1. R_S = series protection resistors
2. R_P = pull-up resistors
3. V_{DD_I2C} = I2C bus supply
4. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 48. SCL frequency (f_{PCLK1}= 32 MHz, V_{DD} = V_{DD_I2C} = 3.3 V)(1)(2)

f_{SCL} (kHz)	I2C_CCR value
	R_P = 4.7 kΩ
400	0x801B
300	0x8024
200	0x8035
100	0x00A0
50	0x0140
20	0x0320

1. R_P = External pull-up resistance, f_{SCL} = I²C speed.
2. For speeds around 200 kHz, the tolerance on the achieved speed is ±5%. For other speed ranges, the tolerance on the achieved speed is ±2%. These variations depend on the accuracy of the external components used to design the application.

SPI characteristics

Unless otherwise specified, the parameters given in the following table are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 13*.

Refer to *Section 6.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 49. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Max(2)	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	16	MHz
		Slave mode	-	16	
		Slave transmitter	-	12(3)	
$t_{r(SCK)}$(2) $t_{f(SCK)}$(2)	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	6	ns
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	30	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode	$4t_{HCLK}$	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	$2t_{HCLK}$	-	
$t_{w(SCKH)}$(2) $t_{w(SCKL)}$(2)	SCK high and low time	Master mode	$t_{SCK}/2-5$	$t_{SCK}/2+3$	
$t_{su(MI)}$(2)	Data input setup time	Master mode	5	-	
$t_{su(SI)}$(2)		Slave mode	6	-	
$t_{h(MI)}$(2)	Data input hold time	Master mode	5	-	
$t_{h(SI)}$(2)		Slave mode	5	-	
$t_{a(SO)}$(4)	Data output access time	Slave mode	0	$3t_{HCLK}$	
$t_{v(SO)}$(2)	Data output valid time	Slave mode	-	33	
$t_{v(MO)}$(2)	Data output valid time	Master mode	-	6.5	
$t_{h(SO)}$(2)	Data output hold time	Slave mode	17	-	
$t_{h(MO)}$(2)		Master mode	0.5	-	

1. The characteristics above are given for voltage Range 1.
2. Guaranteed by characterization results.
3. The maximum SPI clock frequency in slave transmitter mode is given for an SPI slave input clock duty cycle (DuCy(SCK)) ranging between 40 to 60%.
4. Min time is for the minimum time to drive the output and max time is for the maximum time to validate the data.

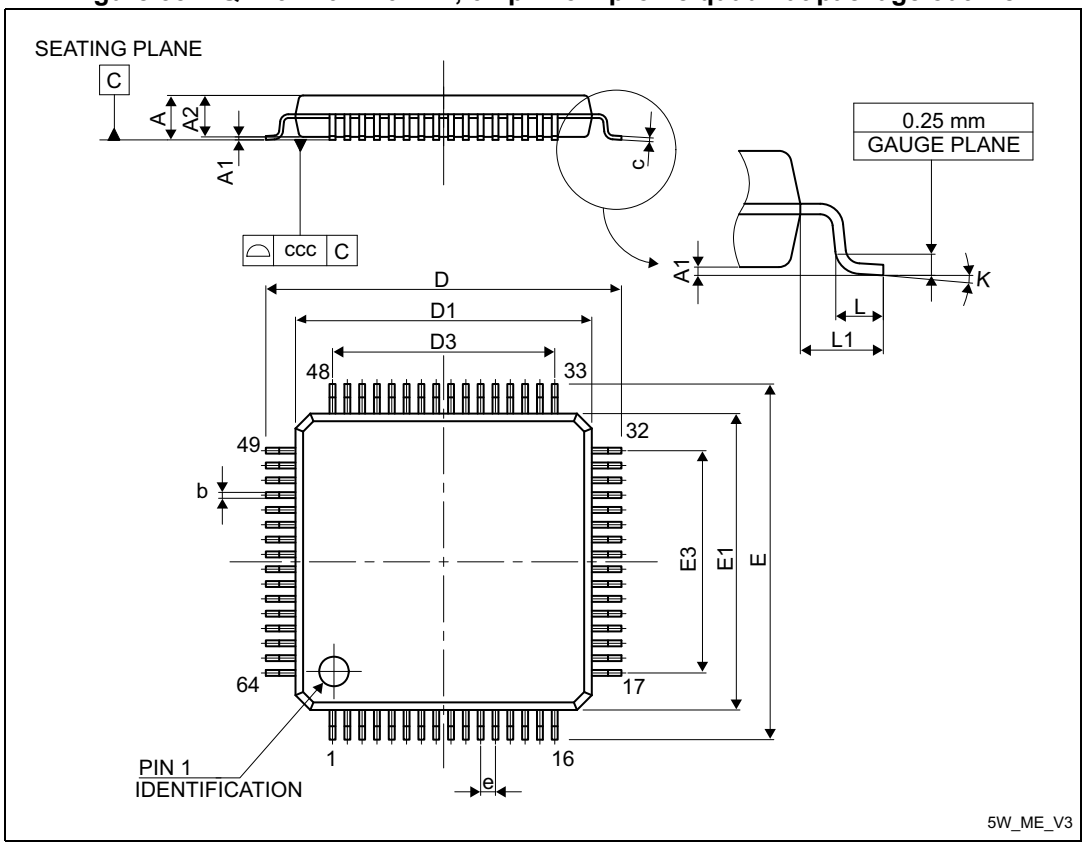
Table 63. LQPF100 14 x 14 mm, 100-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

7.2 LQFP64 10 x 10 mm, 64-pin low-profile quad flat package information

Figure 35. LQFP64 10 x 10 mm, 64-pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 64. LQFP64 10 x 10 mm, 64-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Typ	Min	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-

Table 67. UFBGA100 7 x 7 mm, 0.5 mm pitch, package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
eee	-	-	0.15	-	-	0.0059
fff	-	-	0.05	-	-	0.002

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 45. UFBGA100 7 x 7 mm, 0.5 mm pitch, package recommended footprint

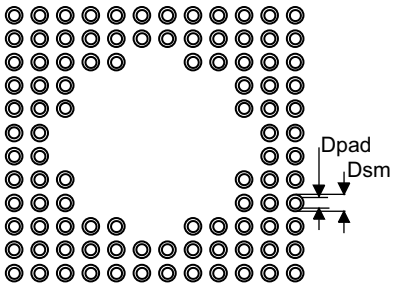


Table 68. UFBGA100 7 x 7 mm, 0.5 mm pitch, recommended PCB design rules

Dimension	Recommended values
Pitch	0.5
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm

Table 73. Document revision history (continued)

Date	Revision	Changes
12-Nov-2013	9 (continued)	Updated *Table 54: ADC characteristics* and *Figure 27: Typical connection diagram using the ADC*. *Table 58: Temperature sensor calibration values* was previously in *Section 3.10.1: Temperature sensor*. Updated *Table 59: Temperature sensor characteristics*. In *Table 61: Comparator 2 characteristics*, parameter dThreshold/dt, replaced any occurrence of “VREF+” by “V_{REFINT}”Updated *Table 63: LQPF100 14 x 14 mm, 100-pin low-profile quad flat package mechanical data*, *Table 64: LQFP64 10 x 10 mm 64-pin low-profile quad flat package mechanical data*, *Table 65: LQFP48 7 x 7 mm, 48-pin low-profile quad flat package mechanical data* and *Table 66: UFQFPN48 7 x 7 mm, 0.5 mm pitch, ultra thin fine-pitch quad flat no-lead package mechanical data*. Updated *Figure 33: LQFP100 recommended footprint*. Updated *Figure 46: TFBGA64 - 5.0x5.0x1.2 mm, 0.5 mm pitch, thin fine-pitch ball grid array package outline* title. Remove minimum and typical values of A dimension in *Table 67: UFBGA100 7 x 7 x 0.6 mm 0.5 mm pitch, ultra thin fine-pitch ball grid array package mechanical data* Deleted second footnote in *Figure 42: UFQFPN48 recommended footprint*. Updated *Section 8: Ordering information* title and added first sentence. Changed BOR disabled option identifier in *Table 72: Ordering information scheme*.
22-Jul-2014	10	Updated *Figure 14*, *Figure 15*. Updated *Table 5*. Updated *Figure 6.3.4*. Updated note *5* inside *Table 54*. Updated Ro value inside *Table 54*.