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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, Cap Sense, DMA, I²S, POR, PWM, WDT
Number of I/O	51
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 20x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l151r6t6

Contents

3.7 Memories

The STM32L151x6/8/B and STM32L152x6/8/B devices have the following features:

- Up to 16 Kbytes of embedded RAM accessed (read/write) at CPU clock speed with 0 wait states. With the enhanced bus matrix, operating the RAM does not lead to any performance penalty during accesses to the system bus (AHB and APB buses).
- The non-volatile memory is divided into three arrays:
  - 32, 64 or 128 Kbytes of embedded Flash program memory
  - 4 Kbytes of data EEPROM
  - Options bytes

  The options bytes are used to write-protect the memory (with 4 Kbytes granularity) and/or readout-protect the whole memory with the following options:
  - Level 0: no readout protection
  - Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
  - Level 2: chip readout protection, debug features (Cortex®-M3 JTAG and serial wire) and boot in RAM selection disabled (JTAG fuse)

  The whole non-volatile memory embeds the error correction code (ECC) feature.

3.8 DMA (direct memory access)

The flexible 7-channel, general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, general-purpose timers and ADC.

3.9 LCD (liquid crystal display)

The LCD drives up to 8 common terminals and 44 segment terminals to drive up to 320 pixels.

- Internal step-up converter to guarantee functionality and contrast control irrespective of V_{DD}. This converter can be deactivated, in which case the V_{LCD} pin is used to provide the voltage to the LCD
- Supports static, 1/2, 1/3, 1/4 and 1/8 duty
- Supports static, 1/2, 1/3 and 1/4 bias
- Phase inversion to reduce power consumption and EMI
- Up to 8 pixels can be programmed to blink
- Unneeded segments and common pins can be used as general I/O pins
- LCD RAM can be updated at any time owing to a double-buffer
- The LCD controller can operate in Stop mode

3.15.5 Window watchdog (WWDG)

The window watchdog is based on a 7-bit down-counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.16 Communication interfaces

3.16.1 I²C bus

Up to two I²C bus interfaces can operate in multimaster and slave modes. They can support standard and fast modes.

They support dual slave addressing (7-bit only) and both 7- and 10-bit addressing in master mode. A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SM Bus 2.0/PM Bus.

3.16.2 Universal synchronous/asynchronous receiver transmitter (USART)

All USART interfaces are able to communicate at speeds of up to 4 Mbit/s. They provide hardware management of the CTS and RTS signals and are ISO 7816 compliant. They support IrDA SIR ENDEC and have LIN Master/Slave capability.

All USART interfaces can be served by the DMA controller.

3.16.3 Serial peripheral interface (SPI)

Up to two SPIs are able to communicate at up to 16 Mbits/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

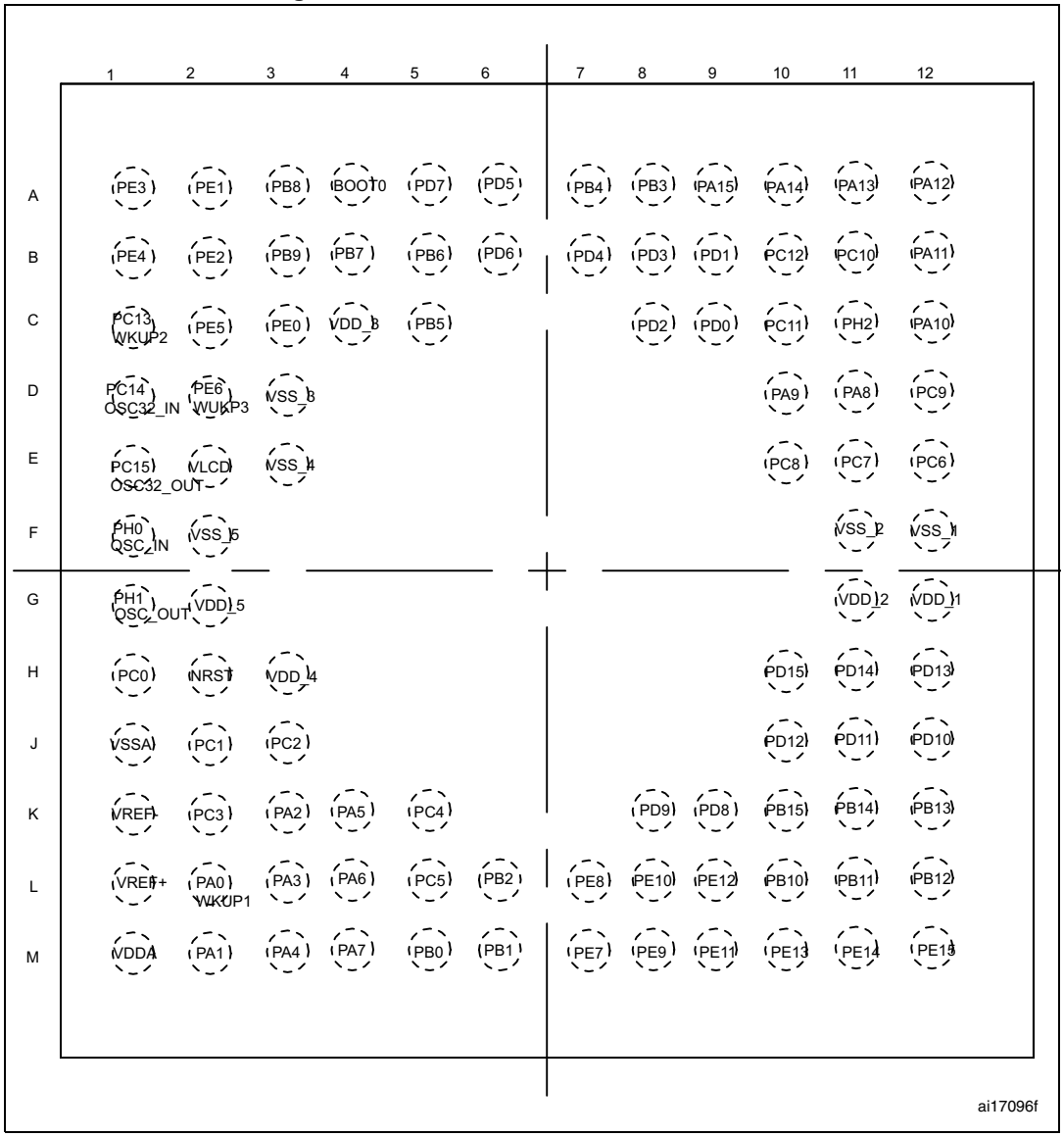
Both SPIs can be served by the DMA controller.

3.16.4 Universal serial bus (USB)

The STM32L151x6/8/B and STM32L152x6/8/B devices embed a USB device peripheral compatible with the USB full speed 12 Mbit/s. The USB interface implements a full speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and supports suspend/resume. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

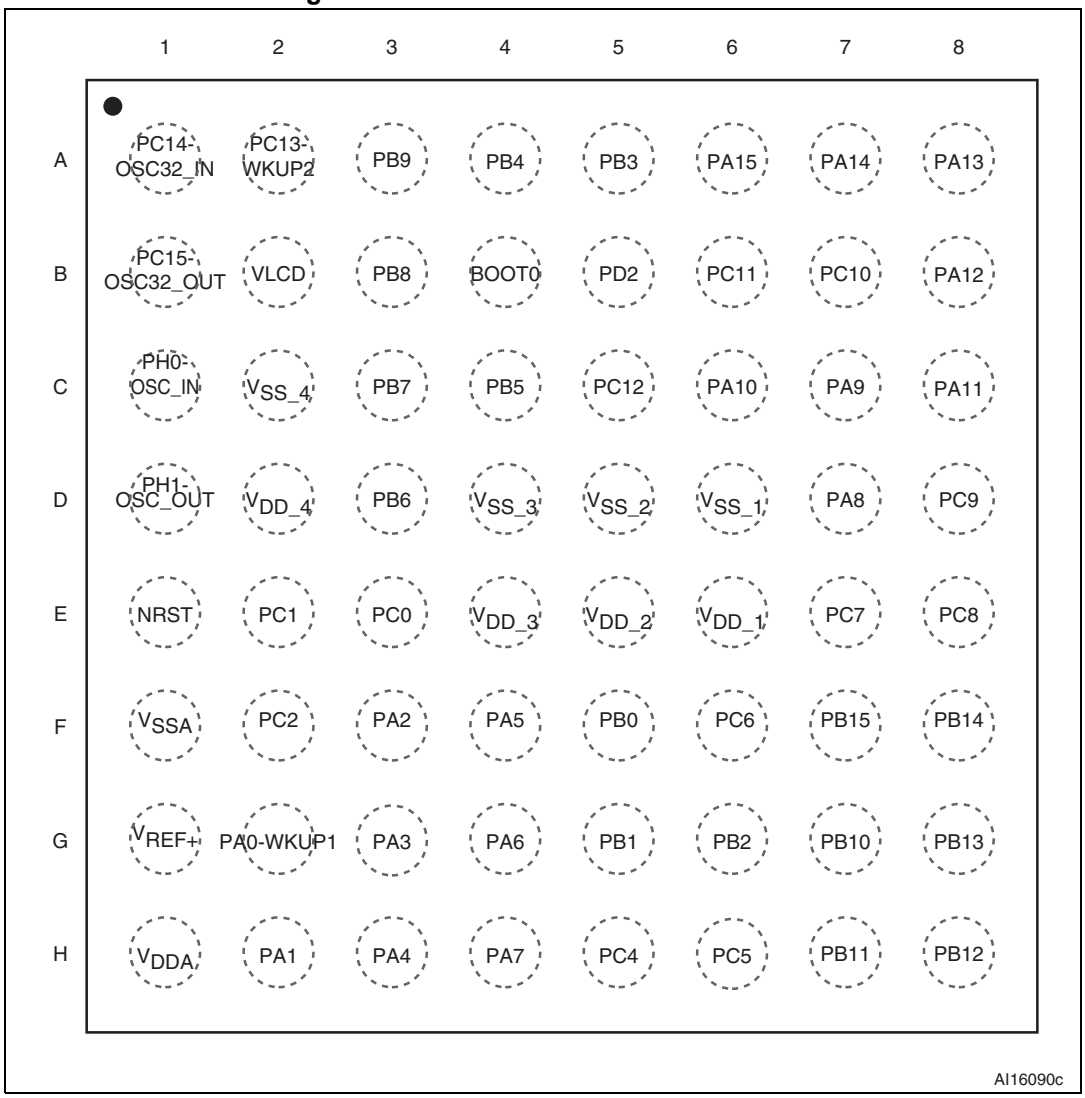
4 Pin descriptions

Figure 3. STM32L15xVx UFBGA100 ballout



1. This figure shows the package top view.

Figure 5. STM32L15xRx TFBGA64 ballout



1. This figure shows the package top view.

Table 8. STM32L151x6/8/B and STM32L152x6/8/B pin definitions

Pins					Pin name	Pin type[1]	I/O structure	Main function[2] (after reset)	Pins functions	
LQFP100	LQFP64	TFBGA64	UFBGA100	LQFP48 or UFQFPN48					Alternate functions	Additional functions
1	-	-	B2	-	PE2	I/O	FT	PE2	TRACECLK/LCD_SEG38/ TIM3_ETR	-
2	-	-	A1	-	PE3	I/O	FT	PE3	TRACED0/LCD_SEG39/ TIM3_CH1	-
3	-	-	B1	-	PE4	I/O	FT	PE4	TRACED1/TIM3_CH2	-
4	-	-	C2	-	PE5	I/O	FT	PE5	TRACED2/TIM9_CH1	-
5	-	-	D2	-	PE6-WKUP3	I/O	FT	PE6	TRACED3/TIM9_CH2	WKUP3
6	1	B2	E2	1	V_{LCD}[3]	S		V_{LCD}	-	-
7	2	A2	C1	2	PC13-WKUP2	I/O	FT	PC13	-	RTC_TAMP1/ RTC_TS/ RTC_OUT/ WKUP2
8	3	A1	D1	3	PC14-OSC32_IN[4]	I/O	TC	PC14	-	OSC32_IN
9	4	B1	E1	4	PC15-OSC32_OUT[4]	I/O	TC	PC15	-	OSC32_OUT
10	-	-	F2	-	V_{SS_5}	S	-	V_{SS_5}	-	-
11	-	-	G2	-	V_{DD_5}	S	-	V_{DD_5}	-	-
12	5	C1	F1	5	PH0-OSC_IN[5]	I/O	TC	PH0	-	OSC_IN
13	6	D1	G1	6	PH1-OSC_OUT	I/O	TC	PH1	-	OSC_OUT
14	7	E1	H2	7	NRST	I/O	RST	NRST	-	-
15	8	E3	H1	-	PC0	I/O	FT	PC0	LCD_SEG18	ADC_IN10/ /COMP1_INP
16	9	E2	J2	-	PC1	I/O	FT	PC1	LCD_SEG19	ADC_IN11/ COMP1_INP
17	10	F2	J3	-	PC2	I/O	FT	PC2	LCD_SEG20	ADC_IN12/ COMP1_INP
18	11	-[6]	K2	-	PC3	I/O	TC	PC3	LCD_SEG21	ADC_IN13/ COMP1_INP

Table 8. STM32L151x6/8/B and STM32L152x6/8/B pin definitions (continued)

Pins					Pin name	Pin type[1]	I/O structure	Main function[2] (after reset)	Pins functions	
LQFP100	LQFP64	TFBGA64	UFBGA100	LQFP48 or UFQFPN48					Alternate functions	Additional functions
90	56	A4	A7	40	PB4	I/O	FT	NJTRST	TIM3_CH1/PB4/ SPI1_MISO/LCD_SEG8/ NJTRST	COMP2_INP
91	57	C4	C5	41	PB5	I/O	FT	PB5	I2C1_SMBA/TIM3_CH2/ SPI1_MOSI/LCD_SEG9	COMP2_INP
92	58	D3	B5	42	PB6	I/O	FT	PB6	I2C1_SCL/TIM4_CH1/ USART1_TX	
93	59	C3	B4	43	PB7	I/O	FT	PB7	I2C1_SDA/TIM4_CH2/ USART1_RX	PVD_IN
94	60	B4	A4	44	BOOT0	I	B	BOOT0	-	-
95	61	B3	A3	45	PB8	I/O	FT	PB8	TIM4_CH3/I2C1_SCL/ LCD_SEG16/TIM10_CH1	-
96	62	A3	B3	46	PB9	I/O	FT	PB9	TIM4_CH4/I2C1_SDA/ LCD_COM3/TIM11_CH1	-
97	-	-	C3	-	PE0	I/O	FT	PE0	TIM4_ETR/LCD_SEG36/ TIM10_CH1	-
98	-	-	A2	-	PE1	I/O	FT	PE1	LCD_SEG37/TIM11_CH1	-
99	63	D4	D3	47	V_{SS_3}	S	-	V_{SS_3}	-	-
100	64	E4	C4	48	V_{DD_3}	S	-	V_{DD_3}	-	-

1. I = input, O = output, S = supply.
2. Function availability depends on the chosen device. For devices having reduced peripheral counts, it is always the lower number of peripheral that is included. For example, if a device has only one SPI and two USARTs, they will be called SPI1 and USART1 & USART2, respectively. Refer to *Table 2 on page 11*.
3. Applicable to STM32L152xx devices only. In STM32L151xx devices, this pin should be connected to V_{DD}.
4. The PC14 and PC15 I/Os are only configured as OSC32_IN/OSC32_OUT when the LSE oscillator is on (by setting the LSEON bit in the RCC_CSR register). The LSE oscillator pins OSC32_IN/OSC32_OUT can be used as general-purpose PC14/PC15 I/Os, respectively, when the LSE oscillator is off (after reset, the LSE oscillator is off). The LSE has priority over the GPIO function. For more details, refer to Using the OSC32_IN/OSC32_OUT pins as GPIO PC14/PC15 port pins section in the STM32L1xxxx reference manual (RM0038).
5. The PH0 and PH1 I/Os are only configured as OSC_IN/OSC_OUT when the HSE oscillator is on (by setting the HSEON bit in the RCC_CR register). The HSE oscillator pins OSC_IN/OSC_OUT can be used as general-purpose PH0/PH1 I/Os, respectively, when the HSE oscillator is off (after reset, the HSE oscillator is off). The HSE has priority over the GPIO function.
6. Unlike in the LQFP64 package, there is no PC3 in the TFBGA64 package. The V_{REF+} functionality is provided instead.

Table 18. Current consumption in Run mode, code with data processing running from RAM

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max(1)			Unit
						55 °C	85 °C	105 °C	
I_{DD} (Run from RAM)	Supply current in Run mode, code executed from RAM, Flash switched off	$f_{HSE} = f_{HCLK}$ up to 16 MHz, included $f_{HSE} = f_{HCLK}/2$ above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	1 MHz	200	300	300	300	µA
				2 MHz	380	500	500	500	
				4 MHz	720	860	860	860(3)	
			Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	4 MHz	0.9	1	1	1	mA
				8 MHz	1.65	2	2	2	
				16 MHz	3.2	3.7	3.7	3.7	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	8 MHz	2	2.5	2.5	2.5	
				16 MHz	4	4.5	4.5	4.5	
				32 MHz	7.7	8.5	8.5	8.5	
		HSI clock source (16 MHz)	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	16 MHz	3.3	3.8	3.8	3.8	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	32 MHz	7.8	9.2	9.2	9.2	
		MSI clock, 65 kHz	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	65 kHz	40	60	60	80	µA
		MSI clock, 524 kHz		524 kHz	110	140	140	160	
		MSI clock, 4.2 MHz		4.2 MHz	700	800	800	820	

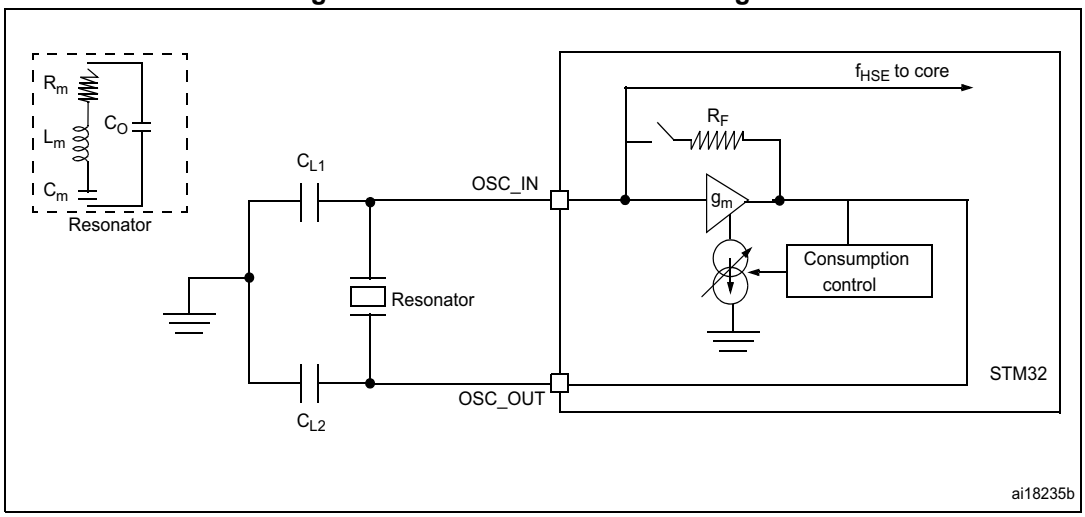
1. Guaranteed by characterization results, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).
3. Tested in production.

Table 19. Current consumption in Sleep mode (continued)

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max(1)			Unit
						55 °C	85 °C	105 °C	
I_{DD} (Sleep)	Supply current in Sleep mode, code executed from Flash	MSI clock, 65 kHz	Range 3, V_{CORE}=1.2V VOS[1:0] = 11	65 kHz	40	70	70	80	µA
		MSI clock, 524 kHz		524 kHz	60	90	90	100	
		MSI clock, 4.2 MHz		4.2 MHz	210	250	250	260	

1. Guaranteed by characterization results, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register)
3. Tested in production

Figure 17. HSE oscillator circuit diagram



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 29*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 29. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE}	Low speed external oscillator frequency	-	-	32.768	-	kHz
R_F	Feedback resistor	-	-	1.2	-	MΩ
$C^{(2)}$	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(3)	R_S = 30 kΩ	-	8	-	pF
I_{LSE}	LSE driving current	V_{DD} = 3.3 V, V_{IN} = V_{SS}	-	-	1.1	µA
$I_{DD\ (LSE)}$	LSE oscillator current consumption	V_{DD} = 1.8 V	-	450	-	nA
		V_{DD} = 3.0 V	-	600	-	
		V_{DD} = 3.6V	-	750	-	
g_m	Oscillator transconductance	-	3	-	-	µA/V
$t_{SU(LSE)}$(4)	Startup time	V_{DD} is stabilized	-	1	-	s

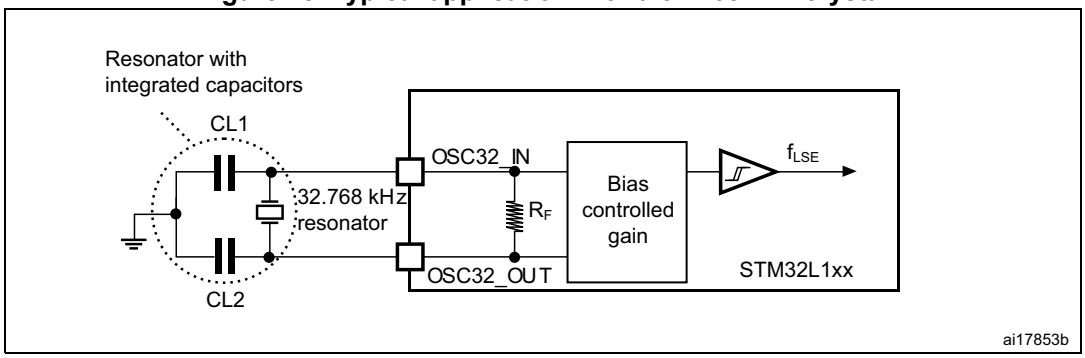
1. Guaranteed by characterization results.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
3. The oscillator selection can be optimized in terms of supply current using an high quality resonator with small R_S value for example MSIV-TIN32.768kHz. Refer to crystal manufacturer for more details.

4. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Note: For CL1 and CL2, it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator (see Figure 18). CL1 and CL2, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of CL1 and CL2.
Load capacitance CL has the following formula: CL = CL1 x CL2 / (CL1 + CL2) + Cstray where Cstray is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

Caution: To avoid exceeding the maximum value of CL1 and CL2 (15 pF) it is strongly recommended to use a resonator with a load capacitance CL ≤ 7 pF. Never use a resonator with a load capacitance of 12.5 pF.
Example: if a resonator is chosen with a load capacitance of CL = 6 pF and Cstray = 2 pF, then CL1 = CL2 = 8 pF.

Figure 18. Typical application with a 32.768 kHz crystal



Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 19* and *Table 44*, respectively.

Unless otherwise specified, the parameters given in *Table 44* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 13*.

Table 44. I/O AC characteristics(1)

OSPEEDRx [1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Max(2)	Unit
00	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	400	kHz
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	400	
	$t_{f(IO)out}$ $t_{r(IO)out}$	Output rise and fall time	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	625	ns
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	625	
01	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	2	MHz
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	1	
	$t_{f(IO)out}$ $t_{r(IO)out}$	Output rise and fall time	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	125	ns
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	250	
10	$F_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	10	MHz
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	2	
	$t_{f(IO)out}$ $t_{r(IO)out}$	Output rise and fall time	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	25	ns
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	125	
11	$F_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	50	MHz
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	8	
	$t_{f(IO)out}$ $t_{r(IO)out}$	Output rise and fall time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	5	ns
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	30	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	8	-	

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the STM32L151x6/8/B and STM32L152x6/8/B reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design.
3. The maximum frequency is defined in *Figure 19*.

6.3.17 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 54* are guaranteed by design.

Table 53. ADC clock frequency

Symbol	Parameter	Conditions			Min	Max	Unit
f_{ADC}	ADC clock frequency	Voltage Range 1 & 2	2.4 V ≤V_{DDA} ≤3.6 V	V_{REF+} = V_{DDA}	0.480	16	MHz
				V_{REF+} < V_{DDA} V_{REF+} > 2.4 V		8	
				V_{REF+} < V_{DDA} V_{REF+} ≤2.4 V		4	
			1.8 V ≤V_{DDA} ≤2.4 V	V_{REF+} = V_{DDA}		8	
				V_{REF+} < V_{DDA}		4	
		Voltage Range 3				4	

Table 54. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	1.8	-	3.6	V
V_{REF+}	Positive reference voltage	2.4 V ≤V_{DDA} ≤3.6 V V_{REF+} must be below or equal to V_{DDA}	1.8(1)	-	V_{DDA}	V
V_{REF-}	Negative reference voltage	-	-	V_{SSA}	-	V
I_{VDDA}	Current on the V_{DDA} input pin	-	-	1000	1450	µA
I_{VREF}(2)	Current on the V_{REF} input pin	Peak	-	400	700	µA
		Average	-		450	µA
V_{AIN}	Conversion voltage range(3)	-	0(4)	-	V_{REF+}	V
f_S	12-bit sampling rate	Direct channels	0.03	-	1	Msps
		Multiplexed channels	0.03	-	0.76	
	10-bit sampling rate	Direct channels	0.03	-	1.07	Msps
		Multiplexed channels	0.03	-	0.8	
	8-bit sampling rate	Direct channels	0.03	-	1.23	Msps
		Multiplexed channels	0.03	-	0.89	
	6-bit sampling rate	Direct channels	0.03	-	1.45	Msps
		Multiplexed channels	0.03	-	1	

Table 54. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_S	Sampling time(5)	Direct channels 2.4 V ≤V_{DDA} ≤3.6 V	0.25	-	-	µs
		Multiplexed channels 2.4 V ≤V_{DDA} ≤3.6 V	0.56	-	-	
		Direct channels 1.8 V ≤V_{DDA} ≤2.4 V	0.56	-	-	
		Multiplexed channels 1.8 V ≤V_{DDA} ≤2.4 V	1	-	-	
		-	4	-	384	$1/f_{ADC}$
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 16 MHz	1	-	24.75	µs
		-	4 to 384 (sampling phase) +12 (successive approximation)			$1/f_{ADC}$
C_{ADC}	Internal sample and hold capacitor	Direct channels	-	16	-	pF
		Multiplexed channels	-		-	
f_{TRIG}	External trigger frequency Regular sequencer	12-bit conversions	-	-	Tconv+1	$1/f_{ADC}$
		6/8/10-bit conversions	-	-	Tconv	$1/f_{ADC}$
f_{TRIG}	External trigger frequency Injected sequencer	12-bit conversions	-	-	Tconv+2	$1/f_{ADC}$
		6/8/10-bit conversions	-	-	Tconv+1	$1/f_{ADC}$
R_{AIN}	Signal source impedance(5)	-	-	-	50	kΩ
t_{lat}	Injection trigger conversion latency	f_{ADC} = 16 MHz	219	-	281	ns
		-	3.5	-	4.5	$1/f_{ADC}$
t_{latr}	Regular trigger conversion latency	f_{ADC} = 16 MHz	156	-	219	ns
		-	2.5	-	3.5	$1/f_{ADC}$
t_{STAB}	Power-up time	-	-	-	3.5	µs

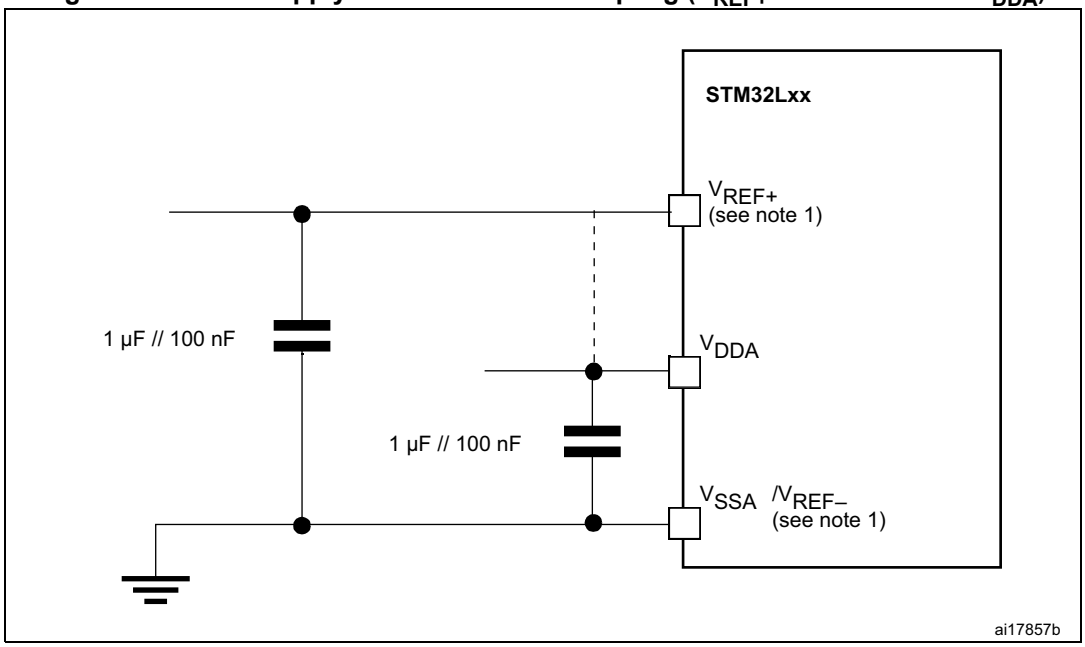
1. The V_{REF+} input can be grounded iif neither the ADC nor the DAC are used (this allows to shut down an external voltage reference).
2. The current consumption through V_{REF} is composed of two parameters:

   - one constant (max 300 µA)

   - one variable (max 400 µA), only during sampling time + 2 first conversion pulses.

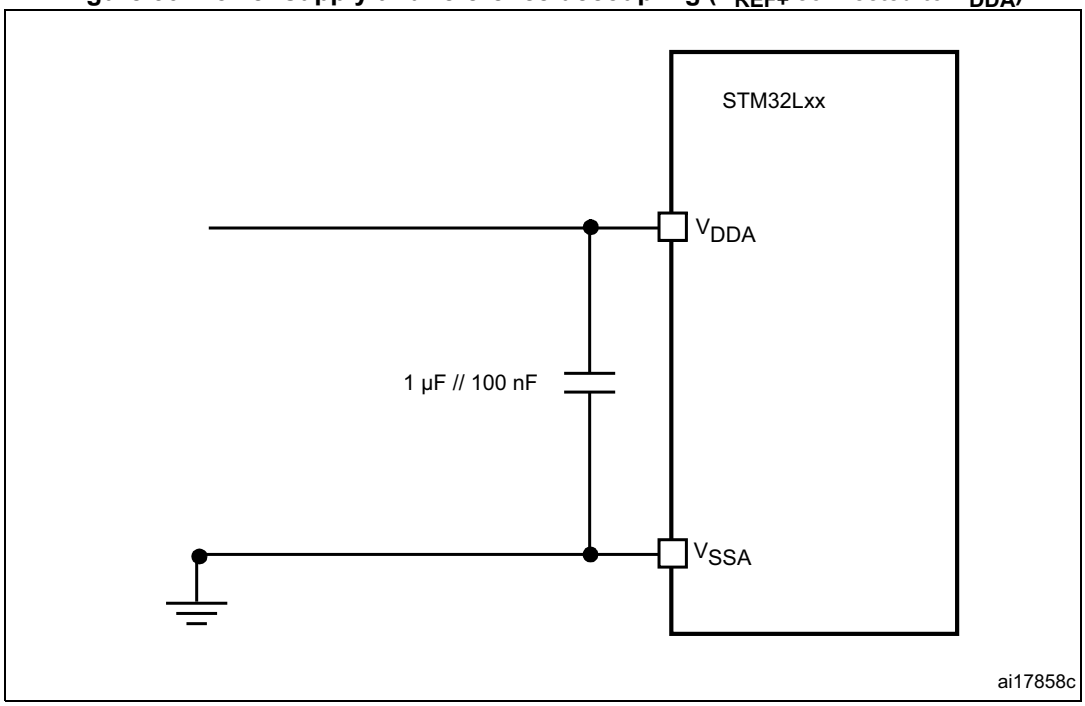
   So, peak consumption is 300+400 = 700 µA and average consumption is 300 + [(4 sampling + 2) /16] x 400 = 450 µA at 1Msps
3. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA}, depending on the package. Refer to *Section 4: Pin descriptions* for further details.
4. V_{SSA} must be tied to ground.
5. See *Table 56: Maximum source impedance RAIN max* for R_{AIN} limitation.

Figure 29. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.

Figure 30. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.

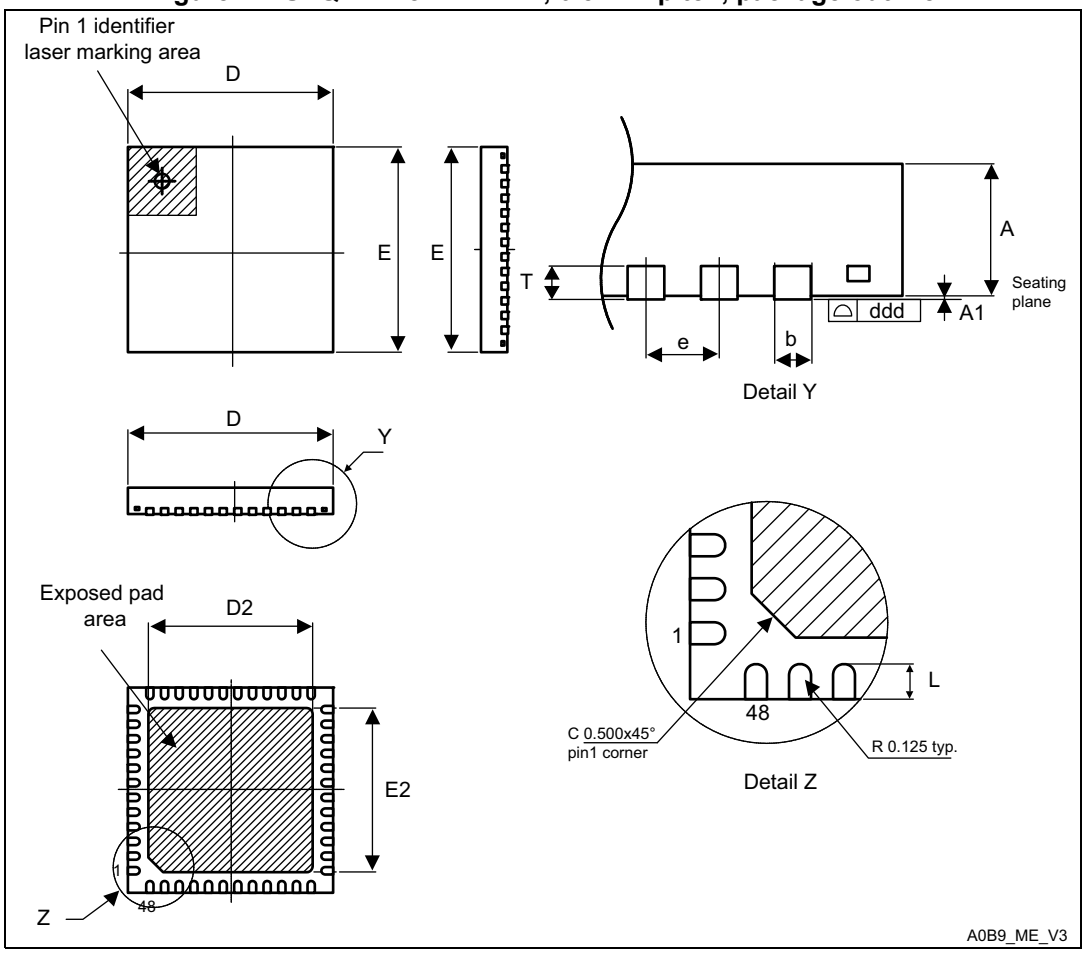
Table 57. DAC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
dOffset/dT(1)	Offset error temperature coefficient (code 0x800)	V_{DDA} = 3.3V, T_A = 0 to 50 °C DAC output buffer OFF	-20	-10	0	µV/°C
		V_{DDA} = 3.3V, T_A = 0 to 50 °C DAC output buffer ON	0	20	50	
Gain(1)	Gain error(6)	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON	-	+0.1 / -0.2%	+0.2 / -0.5%	%
		No R_{LOAD}, $C_L \leq 50$ pF DAC output buffer OFF	-	+0 / -0.2%	+0 / -0.4%	
dGain/dT(1)	Gain error temperature coefficient	V_{DDA} = 3.3V, T_A = 0 to 50 °C DAC output buffer OFF	-10	-2	0	µV/°C
		V_{DDA} = 3.3V, T_A = 0 to 50 °C DAC output buffer ON	-40	-8	0	
TUE(1)	Total unadjusted error	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON	-	12	30	LSB
		No R_{LOAD}, $C_L \leq 50$ pF DAC output buffer OFF	-	8	12	
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes till DAC_OUT reaches final value ±1LSB	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ	-	7	12	µs
Update rate	Max frequency for a correct DAC_OUT change (95% of final value) with 1 LSB variation in the input code	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ	-	-	1	Msps
t_{WAKEUP}	Wakeup time from off state (setting the ENx bit in the DAC Control register)(7)	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ	-	9	15	µs
PSRR+	V_{DDA} supply rejection ratio (static DC measurement)	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ	-	-60	-35	dB

1. Guaranteed by characterization results.
2. Difference between two consecutive codes - 1 LSB.
3. Difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095.
4. Difference between the value measured at Code (0x800) and the ideal value = V/2.
5. Difference between the value measured at Code (0x001) and the ideal value.
6. Difference between ideal slope of the transfer function and measured slope computed from code 0x000 and 0xFFF when buffer is OFF, and from code giving 0.2 V and (V_{DDA} – 0.2) V when buffer is ON.
7. In buffered mode, the output can overshoot above the final value for low input code (starting from min value).

7.4 UFQFPN48 7 x 7 mm, 0.5 mm pitch, package information

Figure 41. UFQFPN48 7 x 7 mm, 0.5 mm pitch, package outline



1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

Table 73. Document revision history (continued)

Date	Revision	Changes
17-June-2011	5	Modified 1st page (low power features) Added STM32L15xC6 and STM32L15xR6 devices (32 Kbytes of Flash memory). Modified *Section 3.6: GPIOs (general-purpose inputs/outputs) on page 22* Modified *Section 6.3: Operating conditions on page 53* Modified *Table 55: ADC accuracy on page 95*, *Table 57: DAC characteristics on page 99* and *Table 60: Comparator 1 characteristics on page 102*
25-Jan-2012	6	*Features*: updated internal multispeed low power RC. *Table 2: Ultralow power STM32L15xx6/8/B device features and peripheral counts*: LCD 4x44 and 8x40 available for both 64- and 128-Kbyte devices; two comparators available for all devices. *Table 3: Functionalities depending on the operating power supply range*: added footnote *1*. *Figure 8: STM32L15xCx UFQFPN48 pinout*: replaced VFQPN48 by UFQFPN48 as name of package. *Table 8: STM32L15xx6/8/B pin definitions*: replaced PH0/PH1 by PC14/PC15. *Table 9: Alternate function input/output*: removed EVENT OUT from PH2 port, AFIO15 column. *Table 19: Current consumption in Sleep mode*: updated MSI conditions and f_{HCLK}. *Table 20: Current consumption in Low power run mode*: updated some temperature conditions; added footnote *2.* *Table 21: Current consumption in Low power sleep mode*: updated some temperature conditions and one of the MSI clock conditions. *Table 22: Typical and maximum current consumptions in Stop mode*: updated I_{DD} (WU from Stop) parameter. *Table 23: Typical and maximum current consumptions in Standby mode*: updated I_{DD} (WU from Standby) parameter. *Table 25: Low-power mode wakeup timings*: updated f_{HCLK} value for $t_{WUSLEEP\_LP}$; updated typical value of parameter “Wakeup from Stop mode, regulator in Run mode”. *Table 24: Peripheral current consumption*: replaced GPIOF by GPIOH. *Table 33: PLL characteristics*: updated “PLL output clock” *Table 35: Flash memory and data EEPROM characteristics*: updated all information for I_{DD}. *Figure 19: I/O AC characteristics definition*: replaced the falling edge “$t_{r(IO)out}$” by “$t_{f(IO)out}$”. *Table 47: I2C characteristics*: amended footnote *2.* *Table 54: ADC characteristics*: updated f_S max value for direct channels, 6-bit sampling rate. *Table 55: ADC accuracy*: Updated the first, third and fourth f_{ADC} test condition. *Table 59: Temperature sensor characteristics*: updated typ, min, and max values of the T_{S_temp} parameter.

Table 73. Document revision history (continued)

Date	Revision	Changes
30-Jan-2015	11	Updated DMIPS features in cover page and *Section 2: Description*. Updated *Table 8: STM32L151x6/8/B and STM32L152x6/8/B pin definitions* and *Table 9: Alternate function input/output* putting additional functions. Updated package top view marking in *Section 7.1: Package mechanical data*. Updated *Figure 9: Memory map*. Updated *Table 56: Maximum source impedance RAIN max* adding note 2. Updated *Table 72: Ordering information scheme*.
28-Apr-2016	12	Updated *Section 7: Package information* structure: Paragraph titles and paragraph heading level. Updated *Section 7: Package information* for all package device markings, adding text for device orientation versus pin 1/ ball A1 identifier. Updated *Figure 34: LQFP100 14 x 14 mm, 100-pin package top view example* removing gate mark. Updated *Table 64: LQFP64 10 x 10 mm, 64-pin low-profile quad flat package mechanical data*. Updated *Section 7.5: UFBGA100 7 x 7 mm, 0.5 mm pitch, ultra thin fine-pitch ball grid array package information* adding *Table 68: UFBGA100 7 x 7 mm, 0.5 mm pitch, recommended PCB design rules* and *Figure 45: UFBGA100 7 x 7 mm, 0.5 mm pitch, package recommended footprint*. Updated *Section 7.6: TFBGA64 5 x 5 mm, 0.5 mm pitch, thin fine-pitch ball grid array package information* adding *Table 70: TFBGA64 5 x 5 mm, 0.5 mm pitch, recommended PCB design rules* and changing *Figure 48: TFBGA64, 5 x 5 mm, 0.5 mm pitch, recommended footprint*. Updated *Table 16: Embedded internal reference voltage* temperature coefficient at 100ppm/°C. Updated note 3 below *Table 16*. Updated *Table 61: Comparator 2 characteristics* new maximum threshold voltage temperature coefficient at 100ppm/°C. Updated *Table 39: ESD absolute maximum ratings* CDM class. Updated all the notes, removing ‘not tested in production’. Updated *Table 10: Voltage characteristics* adding note about V_{REF-} pin. Updated *Table 5: Working mode-dependent functionalities (from Run/active down to standby)* LSI and LSE functionalities putting “Y” in Standby mode. Removed note 1 below *Figure 2: Clock tree*. Updated *Table 57: DAC characteristics* resistive load.