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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Cap Sense, DMA, I²S, POR, PWM, WDT
Number of I/O	51
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 20x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TFBGA
Supplier Device Package	64-TFBGA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l151rbh6d

2.2 Ultra-low-power device continuum

The ultra-low-power STM32L151x6/8/B and STM32L152x6/8/B devices are fully pin-to-pin and software compatible. Besides the full compatibility within the family, the devices are part of STMicroelectronics microcontrollers ultra-low-power strategy which also includes STM8L101xx and STM8L15xx devices. The STM8L and STM32L families allow a continuum of performance, peripherals, system architecture and features.

They are all based on STMicroelectronics ultra-low leakage process.

Note: *The ultra-low-power STM32L and general-purpose STM32Fxxxx families are pin-to-pin compatible. The STM8L15xxx devices are pin-to-pin compatible with the STM8L101xx devices. Please refer to the STM32F and STM8L documentation for more information on these devices.*

2.2.1 Performance

All families incorporate highly energy-efficient cores with both Harvard architecture and pipelined execution: advanced STM8 core for STM8L families and ARM$^®$ Cortex$^®$-M3 core for STM32L family. In addition specific care for the design architecture has been taken to optimize the mA/DMIPS and mA/MHz ratios.

This allows the ultra-low-power performance to range from 5 up to 33.3 DMIPs.

2.2.2 Shared peripherals

STM8L15xxx and STM32L1xxxx share identical peripherals which ensure a very easy migration from one family to another:

* Analog peripherals: ADC, DAC and comparators
* Digital peripherals: RTC and some communication interfaces

2.2.3 Common system strategy

To offer flexibility and optimize performance, the STM8L15xx and STM32L1xxxx families use a common architecture:

* Same power supply range from 1.65 V to 3.6 V, (1.65 V at power down only for STM8L15xx devices)
* Architecture optimized to reach ultra-low consumption both in low power modes and Run mode
* Fast startup strategy from low power modes
* Flexible system clock
* Ultrasafe reset: same reset strategy including power-on reset, power-down reset, brownout reset and programmable voltage detector.

2.2.4 Features

ST ultra-low-power continuum also lies in feature compatibility:

* More than 10 packages with pin count from 20 to 144 pins and size down to 3 x 3 mm
* Memory density ranging from 4 to 384 Kbytes

HSE crystal oscillators are disabled. The voltage regulator is in the low power mode. The device can be woken up from Stop mode by any of the EXTI line, in 8 µs. The EXTI line source can be one of the 16 external lines. It can be the PVD output, the Comparator 1 event or Comparator 2 event (if internal reference voltage is on). It can also be wakened by the USB wakeup.

Stop mode consumption: refer to *Table 22: Typical and maximum current consumptions in Stop mode*.

- **Standby** mode with RTC

  Standby mode is used to achieve the lowest power consumption and real time clock. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSI RC and HSE crystal oscillators are also switched off. The LSE or LSI is still running. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC_CSR).

  The device exits Standby mode in 60 µs when an external reset (NRST pin), an IWDG reset, a rising edge on one of the three WKUP pins, RTC alarm (Alarm A or Alarm B), RTC tamper event, RTC timestamp event or RTC Wakeup event occurs.

- **Standby** mode without RTC

  Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI, RC, HSI and LSI RC, HSE and LSE crystal oscillators are also switched off. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC_CSR).

  The device exits Standby mode in 60 µs when an external reset (NRST pin) or a rising edge on one of the three WKUP pin occurs.

  Standby mode consumption: refer to *Table 23*.

Note: *The RTC, the IWDG, and the corresponding clock sources are not stopped by entering the Stop or Standby mode.*

Table 3. Functionalities depending on the operating power supply range

Operating power supply range	Functionalities depending on the operating power supply range			
	DAC and ADC operation	USB	Dynamic voltage scaling range	I/O operation
V_{DD} = 1.65 to 1.71 V	Not functional	Not functional	Range 2 or Range 3	Degraded speed performance
V_{DD} = 1.71 to 1.8 V[1]	Not functional	Not functional	Range 1, Range 2 or Range 3	Degraded speed performance
V_{DD} = 1.8 to 2.0 V[1]	Conversion time up to 500 Ksps	Not functional	Range 1, Range 2 or Range 3	Degraded speed performance

Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Stop mode, it is possible to automatically switch off the internal reference voltage (V_{REFINT}) in Stop mode. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for any external reset circuit.

Note: *The start-up time at power-on is typically 3.3 ms when BOR is active at power-up, the start-up time at power-on can be decreased down to 1 ms typically for devices with BOR inactive at power-up.*

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.3.3 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

*   MR is used in Run mode (nominal regulation)
*   LPR is used in the Low-power run, Low-power sleep and Stop modes
*   Power down is used in Standby mode. The regulator output is high impedance, the kernel circuitry is powered down, inducing zero consumption but the contents of the registers and RAM are lost are lost except for the standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE crystal 32K osc, RCC_CSR).

3.3.4 Boot modes

At startup, boot pins are used to select one of three boot options:

*   Boot from Flash memory
*   Boot from System Memory
*   Boot from embedded RAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART1 or USART2. See STM32™ microcontroller system memory boot mode AN2606 for details.

3.4 Clock management

The clock controller distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low power modes and ensures clock robustness. It features:

- **Clock prescaler**: to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler

- **Safe clock switching**: clock sources can be changed safely on the fly in run mode through a configuration register.

- **Clock management**: to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.

- **Master clock source**: three different clock sources can be used to drive the master clock:
  - 1-24 MHz high-speed external crystal (HSE), that can supply a PLL
  - 16 MHz high-speed internal RC oscillator (HSI), trimmable by software, that can supply a PLL
  - Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 7 frequencies (65.5 kHz, 131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.1 MHz, 4.2 MHz) with a consumption proportional to speed, down to 750 nA typical. When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be trimmed by software down to a ±0.5% accuracy.

- **Auxiliary clock source**: two ultra-low-power clock sources that can be used to drive the LCD controller and the real-time clock:
  - 32.768 kHz low-speed external crystal (LSE)
  - 37 kHz low-speed internal RC (LSI), also used to drive the independent watchdog. The LSI clock can be measured using the high-speed internal RC oscillator for greater precision.

- **RTC and LCD clock sources:** the LSI, LSE or HSE sources can be chosen to clock the RTC and the LCD, whatever the system clock.

- **USB clock source:** the embedded PLL has a dedicated 48 MHz clock output to supply the USB interface.

- **Startup clock:** after reset, the microcontroller restarts by default with an internal 2.1 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.

- **Clock security system (CSS):** this feature can be enabled by software. If a HSE clock failure occurs, the master clock is automatically switched to HSI and a software interrupt is generated if enabled.

- **Clock-out capability (MCO: microcontroller clock output):** it outputs one of the internal clocks for external use by the application.

Several prescalers allow the configuration of the AHB frequency, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the AHB and the APB domains is 32 MHz. See *Figure 2* for details on the clock tree.

Table 8. STM32L151x6/8/B and STM32L152x6/8/B pin definitions

Pins					Pin name	Pin type[1]	I/O structure	Main function[2] (after reset)	Pins functions	
LQFP100	LQFP64	TFBGA64	UFBGA100	LQFP48 or UFQFPN48					Alternate functions	Additional functions
1	-	-	B2	-	PE2	I/O	FT	PE2	TRACECLK/LCD_SEG38/ TIM3_ETR	-
2	-	-	A1	-	PE3	I/O	FT	PE3	TRACED0/LCD_SEG39/ TIM3_CH1	-
3	-	-	B1	-	PE4	I/O	FT	PE4	TRACED1/TIM3_CH2	-
4	-	-	C2	-	PE5	I/O	FT	PE5	TRACED2/TIM9_CH1	-
5	-	-	D2	-	PE6-WKUP3	I/O	FT	PE6	TRACED3/TIM9_CH2	WKUP3
6	1	B2	E2	1	V_{LCD}[3]	S		V_{LCD}	-	-
7	2	A2	C1	2	PC13-WKUP2	I/O	FT	PC13	-	RTC_TAMP1/ RTC_TS/ RTC_OUT/ WKUP2
8	3	A1	D1	3	PC14-OSC32_IN[4]	I/O	TC	PC14	-	OSC32_IN
9	4	B1	E1	4	PC15-OSC32_OUT[4]	I/O	TC	PC15	-	OSC32_OUT
10	-	-	F2	-	V_{SS_5}	S	-	V_{SS_5}	-	-
11	-	-	G2	-	V_{DD_5}	S	-	V_{DD_5}	-	-
12	5	C1	F1	5	PH0-OSC_IN[5]	I/O	TC	PH0	-	OSC_IN
13	6	D1	G1	6	PH1-OSC_OUT	I/O	TC	PH1	-	OSC_OUT
14	7	E1	H2	7	NRST	I/O	RST	NRST	-	-
15	8	E3	H1	-	PC0	I/O	FT	PC0	LCD_SEG18	ADC_IN10/ /COMP1_INP
16	9	E2	J2	-	PC1	I/O	FT	PC1	LCD_SEG19	ADC_IN11/ COMP1_INP
17	10	F2	J3	-	PC2	I/O	FT	PC2	LCD_SEG20	ADC_IN12/ COMP1_INP
18	11	-[6]	K2	-	PC3	I/O	TC	PC3	LCD_SEG21	ADC_IN13/ COMP1_INP

Table 8. STM32L151x6/8/B and STM32L152x6/8/B pin definitions (continued)

Pins					Pin name	Pin type[1]	I/O structure	Main function[2] (after reset)	Pins functions	
LQFP100	LQFP64	TFBGA64	UFBGA100	LQFP48 or UFQFPN48					Alternate functions	Additional functions
35	26	F5	M5	18	PB0	I/O	TC	PB0	TIM3_CH3/LCD_SEG5	ADC_IN8/ COMP1_INP/ VREF_OUT
36	27	G5	M6	19	PB1	I/O	FT	PB1	TIM3_CH4/LCD_SEG6	ADC_IN9/ COMP1_INP/ VREF_OUT
37	28	G6	L6	20	PB2	I/O	FT	PB2/BOOT1	BOOT1	-
38	-	-	M7	-	PE7	I/O	TC	PE7	-	ADC_IN22/ COMP1_INP
39	-	-	L7	-	PE8	I/O	TC	PE8	-	ADC_IN23/ COMP1_INP
40	-	-	M8	-	PE9	I/O	TC	PE9	TIM2_CH1_ETR	ADC_IN24/ COMP1_INP
41	-	-	L8	-	PE10	I/O	TC	PE10	TIM2_CH2	ADC_IN25/ COMP1_INP
42	-	-	M9	-	PE11	I/O	FT	PE11	TIM2_CH3	-
43	-	-	L9	-	PE12	I/O	FT	PE12	TIM2_CH4/SPI1_NSS	-
44	-	-	M10	-	PE13	I/O	FT	PE13	SPI1_SCK	-
45	-	-	M11	-	PE14	I/O	FT	PE14	SPI1_MISO	-
46	-	-	M12	-	PE15	I/O	FT	PE15	SPI1_MOSI	-
47	29	G7	L10	21	PB10	I/O	FT	PB10	I2C2_SCL/USART3_TX/ TIM2_CH3/LCD_SEG10	-
48	30	H7	L11	22	PB11	I/O	FT	PB11	I2C2_SDA/USART3_RX/ TIM2_CH4/LCD_SEG11	-
49	31	D6	F12	23	V_{SS_1}	S	-	V_{SS_1}	-	-
50	32	E6	G12	24	V_{DD_1}	S	-	V_{DD_1}	-	-
51	33	H8	L12	25	PB12	I/O	FT	PB12	SPI2_NSS/I2C2_SMBA/ USART3_CK/ LCD_SEG12/TIM10_CH1	ADC_IN18/ COMP1_INP
52	34	G8	K12	26	PB13	I/O	FT	PB13	SPI2_SCK/USART3_CTS/ LCD_SEG13/ TIM9_CH1	ADC_IN19/ COMP1_INP

Table 9. Alternate function input/output (continued)

Port name	Digital alternate function number														
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFOI6	AFIO7	AFIO8	AFIO9	AFIO11	AFIO12	AFIO13	AFIO14	AFIO15
	Alternate function														
	SYSTEM	TIM2	TIM3/4	TIM9/10/11	I2C1/2	SPI1/2	N/A	USART1/2/3	N/A	N/A	LCD	N/A	N/A	RI	SYSTEM
PD13	-	-	TIM4_CH2	-	-	-	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PD14	-	-	TIM4_CH3	-	-	-	-	-	-	-	-	-	-	TIMx_IC3	EVENTOUT
PD15	-	-	TIM4_CH4	-	-	-	-	-	-	-	-	-	-	TIMx_IC4	EVENTOUT
PE0	-	-	TIM4_ETR	TIM10_CH1	-	-	-	-	-	-	-	-	-	TIMx_IC1	EVENTOUT
PE1	-	-		TIM11_CH1	-	-	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PE2	TRACECK	-	TIM3_ETR	-	-	-	-	-	-	-	-	-	-	TIMx_IC3	EVENTOUT
PE3	TRACED0	-	TIM3_CH1	-	-	-	-	-	-	-	-	-	-	TIMx_IC4	EVENTOUT
PE4	TRACED1	-	TIM3_CH2	-	-	-	-	-	-	-	-	-	-	TIMx_IC1	EVENTOUT
PE5	TRACED2	-	-	TIM9_CH1*	-	-	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PE6	TRACED3	-	-	TIM9_CH2*	-	-	-	-	-	-	-	-	-	TIMx_IC3	EVENTOUT
PE7	-	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC4	EVENTOUT
PE8	-	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC1	EVENTOUT
PE9	-	TIM2_CH1_ETR	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PE10	-	TIM2_CH2	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC3	EVENTOUT
PE11	-	TIM2_CH3	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC4	EVENTOUT
PE12	-	TIM2_CH4	-	-	-	SPI1_NSS	-	-	-	-	-	-	-	TIMx_IC1	EVENTOUT
PE13	-	-	-	-	-	SPI1_SCK	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PE14	-	-	-	-	-	SPI1_MISO	-	-	-	-	-	-	-	TIMx_IC3	EVENTOUT
PE15	-	-	-	-	-	SPI1_MOSI	-	-	-	-	-	-	-	TIMx_IC4	EVENTOUT
PH0-OSC_IN	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

6   Electrical characteristics

6.1   Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1   Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

Please refer to device ErrataSheet for possible latest changes of electrical characteristics.

6.1.2   Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.6 V (for the 1.65 V ≤ V_{DD} ≤ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

6.1.3   Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4   Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 10*.

6.1.5   Pin input voltage

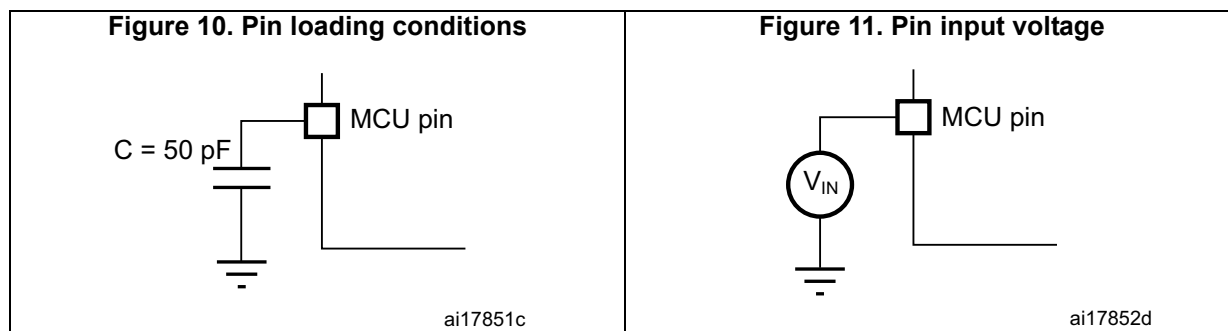The input voltage measurement on a pin of the device is described in *Figure 11*.

Figure 10. Pin loading conditions

Figure 11. Pin input voltage

Table 24. Peripheral current consumption[1]

Peripheral		Typical consumption, V_{DD} = 3.0 V, T_A = 25 °C				Unit
		Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	Low power sleep and run	
APB1	TIM2	13	10.5	8	10.5	µA/MHz (f_{HCLK})
	TIM3	14	12	9	12	
	TIM4	12.5	10.5	8	11	
	TIM6	5.5	4.5	3.5	4.5	
	TIM7	5.5	5	3.5	4.5	
	LCD	5.5	5	3.5	5	
	WWDG	4	3.5	2.5	3.5	
	SPI2	5.5	5	4	5	
	USART2	9	8	5.5	8.5	
	USART3	10.5	9	6	8	
	I2C1	8.5	7	5.5	7.5	
	I2C2	8.5	7	5.5	6.5	
	USB	12.5	10	6.5	10	
	PWR	4.5	4	3	3.5	
	DAC	9	7.5	6	7	
	COMP	4.5	4	3.5	4.5	
APB2	SYSCFG & RI	3	2.5	2	2.5	µA/MHz (f_{HCLK})
	TIM9	9	7.5	6	7	
	TIM10	6.5	5.5	4.5	5.5	
	TIM11	7	6	4.5	5.5	
	ADC[2]	11.5	9.5	8	9	
	SPI1	5	4.5	3	4	
	USART1	9	7.5	6	7.5	

6.3.5 Wakeup time from Low power mode

The wakeup times given in the following table are measured with the MSI RC oscillator. The clock source used to wake up the device depends on the current operating mode:

- Sleep mode: the clock source is the clock that was set before entering Sleep mode
- Stop mode: the clock source is the MSI oscillator in the range configured before entering Stop mode
- Standby mode: the clock source is the MSI oscillator running at 2.1 MHz

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 13*.

Table 25. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ	Max[1]	Unit
$t_{WUSLEEP}$	Wakeup from Sleep mode	f_{HCLK} = 32 MHz	0.36	-	μs
$t_{WUSLEEP\_LP}$	Wakeup from Low power sleep mode f_{HCLK} = 262 kHz	f_{HCLK} = 262 kHz Flash enabled	32	-	
		f_{HCLK} = 262 kHz Flash switched OFF	34	-	
t_{WUSTOP}	Wakeup from Stop mode, regulator in Run mode	f_{HCLK} = f_{MSI} = 4.2 MHz	8.2	-	
	Wakeup from Stop mode, regulator in low power mode	f_{HCLK} = f_{MSI} = 4.2 MHz Voltage Range 1 and 2	8.2	9.3	
		f_{HCLK} = f_{MSI} = 4.2 MHz Voltage Range 3	7.8	11.2	
		f_{HCLK} = f_{MSI} = 2.1 MHz	10	12	
		f_{HCLK} = f_{MSI} = 1.05 MHz	15.5	20	
		f_{HCLK} = f_{MSI} = 524 kHz	29	35	
		f_{HCLK} = f_{MSI} = 262 kHz	53	63	
		f_{HCLK} = f_{MSI} = 131 kHz	105	118	
		f_{HCLK} = MSI = 65 kHz	210	237	
$t_{WUSTDBY}$	Wakeup from Standby mode FWU bit = 1	f_{HCLK} = MSI = 2.1 MHz	50	103	
	Wakeup from Standby mode FWU bit = 0	f_{HCLK} = MSI = 2.1 MHz	2.5	3.2	ms

1. Guaranteed by characterization results, unless otherwise specified

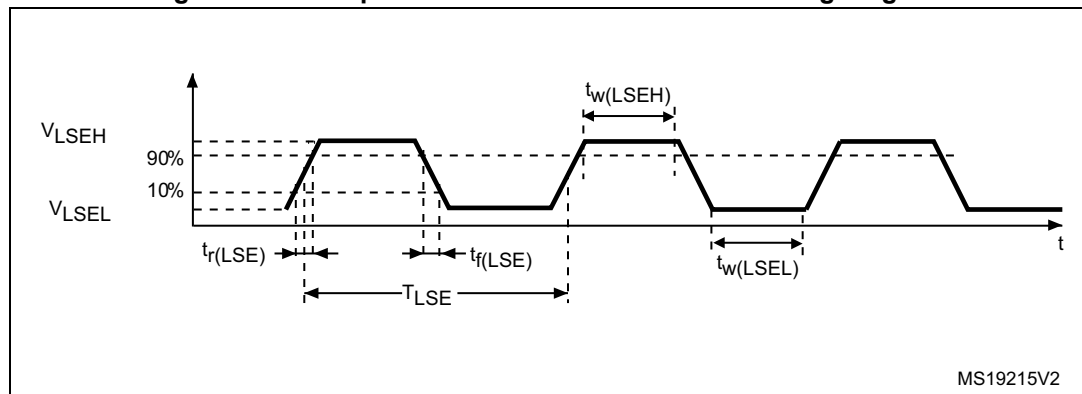### Low-speed external user clock generated from an external source

The characteristics given in the following table result from tests performed using a low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 13*.

Table 27. Low-speed external user clock characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency		1	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage	-	V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time		465	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time		-	-	10	
$C_{IN(LSE)}$	OSC32_IN input capacitance	-	-	0.6	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	45	-	55	%
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design.

Figure 16. Low-speed external clock source AC timing diagram

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 1 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 28*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

6.3.7   Internal clock source characteristics

The parameters given in the following table are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 13*.

High-speed internal (HSI) RC oscillator

Table 30. HSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	V_{DD} = 3.0 V	-	16	-	MHz
$TRIM^{(1)(2)}$	HSI user-trimmed resolution	Trimming code is not a multiple of 16	-	± 0.4	0.7	%
		Trimming code is a multiple of 16	-	-	± 1.5	%
$ACC_{HSI}^{(2)}$	Accuracy of the factory-calibrated HSI oscillator	V_{DDA} = 3.0 V, T_A = 25 °C	-1[3]	-	1[3]	%
		V_{DDA} = 3.0 V, T_A = 0 to 55 °C	-1.5	-	1.5	%
		V_{DDA} = 3.0 V, T_A = -10 to 70 °C	-2	-	2	%
		V_{DDA} = 3.0 V, T_A = -10 to 85 °C	-2.5	-	2	%
		V_{DDA} = 3.0 V, T_A = -10 to 105 °C	-4	-	2	%
		V_{DDA} = 1.65 V to 3.6 V T_A = -40 to 105 °C	-4	-	3	%
$t_{SU(HSI)}^{(2)}$	HSI oscillator startup time	-	-	3.7	6	µs
$I_{DD(HSI)}^{(2)}$	HSI oscillator power consumption	-	-	100	140	µA

1. The trimming step differs depending on the trimming code. It is usually negative on the codes which are multiples of 16 (0x00, 0x10, 0x20, 0x30...0xE0).

2. Guaranteed by characterization results.

3. Tested in production.

Low-speed internal (LSI) RC oscillator

Table 31. LSI oscillator characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$f_{LSI}^{(1)}$	LSI frequency	26	38	56	kHz
$D_{LSI}^{(2)}$	LSI oscillator frequency drift $0°C \leq T_A \leq 85°C$	-10	-	4	%
$t_{su(LSI)}^{(3)}$	LSI oscillator startup time	-	-	200	µs
$I_{DD(LSI)}^{(3)}$	LSI oscillator power consumption	-	400	510	nA

1. Tested in production.

2. This is a deviation for an individual part, once the initial frequency has been measured.

3. Guaranteed by design.

6.3.9 Memory characteristics

The characteristics are given at T_A = -40 to 105 °C unless otherwise specified.

RAM memory

Table 34. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VRM	Data retention mode[1]	STOP mode (or RESET)	1.65	-	-	V

1. Minimum supply voltage without losing data stored in RAM (in Stop mode or under Reset) or in hardware registers (only in Stop mode).

Flash memory and data EEPROM

Table 35. Flash memory and data EEPROM characteristics

Symbol	Parameter	Conditions	Min	Typ	Max[1]	Unit
V_{DD}	Operating voltage Read / Write / Erase	-	1.65	-	3.6	V
t_{prog}	Programming / erasing time for byte / word / double word / half-page	Erasing	-	3.28	3.94	ms
		Programming	-	3.28	3.94	
I_{DD}	Average current during whole program/erase operation	T_A = 25 °C, V_{DD} = 3.6 V	-	300	-	µA
	Maximum current (peak) during program/erase operation		-	1.5	2.5	mA

1. Guaranteed by design.

Table 36. Flash memory, data EEPROM endurance and data retention

Symbol	Parameter	Conditions	Value Min[1]	Typ	Max	Unit
NCYC[2]	Cycling (erase / write) Program memory	T_A = -40°C to 105 °C	10	-	-	kcycles
	Cycling (erase / write) EEPROM data memory		300	-	-	
t_{RET}[2]	Data retention (program memory) after 10 kcycles at T_A = 85 °C	TRET = +85 °C	30	-	-	years
	Data retention (EEPROM data memory) after 300 kcycles at T_A = 85 °C		30	-	-	
	Data retention (program memory) after 10 kcycles at T_A = 105 °C	TRET = +105 °C	10	-	-	
	Data retention (EEPROM data memory) after 300 kcycles at T_A = 105 °C		10	-	-	

1. Guaranteed by characterization results.

2. Characterization is done according to JEDEC JESD22-A117.

Table 61. Comparator 2 characteristics

| Symbol	Parameter	Conditions	Min	Typ	Max[1]	Unit
V_{DDA}	Analog supply voltage	-	1.	-	3.6	V
V_{IN}	Comparator 2 input voltage range	-	0	-	V_{DDA}	V
t_{START}	Comparator startup time	Fast mode	-	15	20	μs
		Slow mode	-	20	25	
$t_{d\ slow}$	Propagation delay[2] in slow mode	1. V $\leq V_{DDA} \leq$ 2.7 V	-	1.8	3.5	
		2.7 V $\leq V_{DDA} \leq$ 3.6 V	-	2.5	6	
$t_{d\ fast}$	Propagation delay[2] in fast mode	1. V $\leq V_{DDA} \leq$ 2.7 V	-	0.8	2	
		2.7 V $\leq V_{DDA} \leq$ 3.6 V	-	1.2	4	
V_{offset}	Comparator offset error	-	-	±4	±20	mV
dThreshold/ dt	Threshold voltage temperature coefficient	V_{DDA} = 3.3V T_A = 0 to 50 °C V- = V_{REFINT}, 3/4 V_{REFINT}, 1/2 V_{REFINT}, 1/4 V_{REFINT}	-	15	100	ppm /°C
I_{COMP2}	Current consumption[3]	Fast mode	-	3.5	5	μA
		Slow mode	-	0.5	2	

1. Guaranteed by characterization results.

2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.

3. Comparator consumption only. Internal reference voltage (necessary for comparator operation) is not included.

7.2 LQFP64 10 x 10 mm, 64-pin low-profile quad flat package information

Figure 35. LQFP64 10 x 10 mm, 64-pin low-profile quad flat package outline
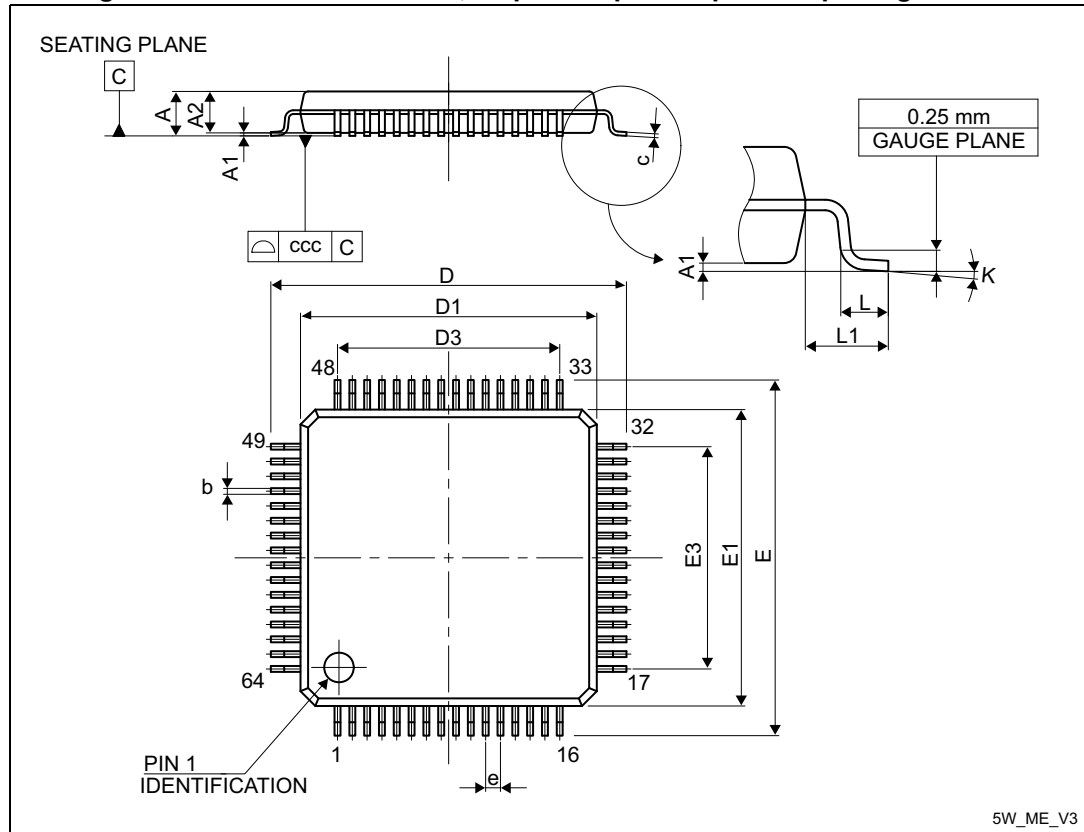
1. Drawing is not to scale.

Table 64. LQFP64 10 x 10 mm, 64-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	**Typ**	**Max**	**Typ**	**Min**	**Max**
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-

Table 65. LQFP48 7 x 7 mm, 48-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 39. LQFP48 7 x 7 mm, 48-pin low-profile quad flat recommended footprint
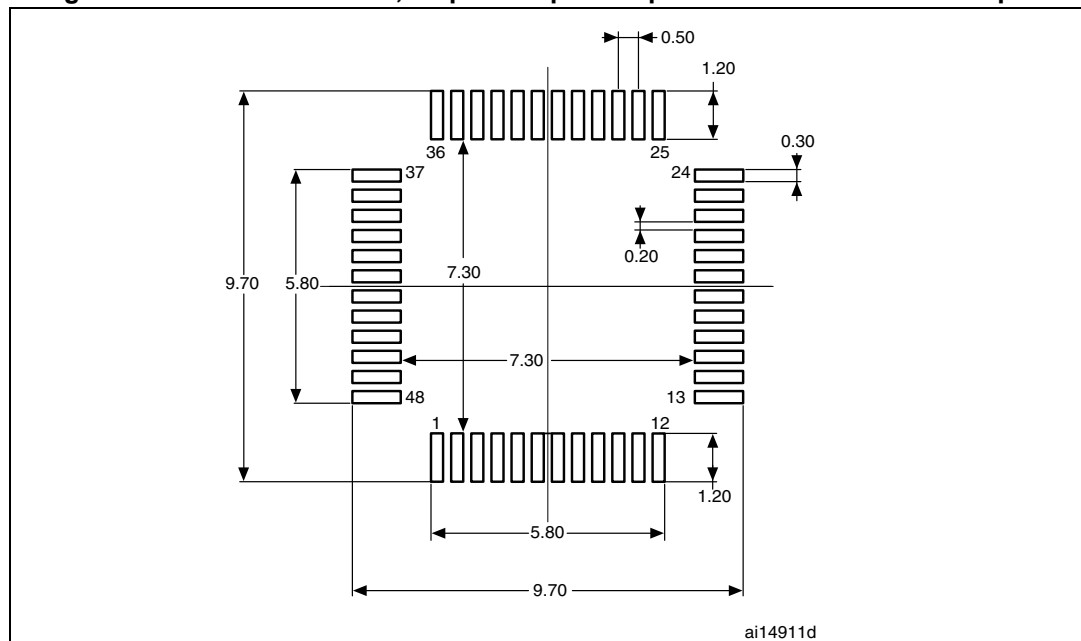
1. Dimensions are in millimeters.

9   Revision history

Table 73. Document revision history

Date	Revision	Changes
02-Jul-2010	1	Initial release.
01-Oct-2010	2	Removed 5 V tolerance (FT) from PA3, PB0 and PC3 in *Table 8: STM32L15xx6/8/B pin definitions* Updated *Table 14: Embedded reset and power control block characteristics* Updated *Table 16: Embedded internal reference voltage* Added *Table 53: ADC clock frequency* Updated *Table 54: ADC characteristics*
16-Dec-2010	3	Modified consumptions on page 1 and in *Section 3.1: Low power modes* LED_SEG8 removed on PB6. Updated *Section 6: Electrical characteristics* VFQFPN48 replaced by UFQFPN48
25-Feb-2011	4	*Section 3.3.2: Power supply supervisor*: updated note. *Table 8: STM32L15xx6/8/B pin definitions:* modified main function (after reset) and alternate function for OSC_IN and OSC_OUT pins; modified footnote 5; added footnote to OSC32_IN and OSC32_OUT pins; C1 and D1 removed on PD0 and PD1 pins (TFBGA64 column). *Section 3.11: DAC (digital-to-analog converter)*: updated bullet list. *Table 10: Voltage characteristics on page 52*: updated footnote 3 regarding $I_{INJ(PIN)}$. *Table 11: Current characteristics on page 52*: updated footnote 4 regarding positive and negative injection. *Table 14: Embedded reset and power control block characteristics on page 54*: updated typ and max values for $T_{RSTTEMPO}$ (V_{DD} rising, BOR enabled). *Table 17: Current consumption in Run mode, code with data processing running from Flash on page 58*: removed values for HSI clock source (16 MHz), Range 3. *Table 18: Current consumption in Run mode, code with data processing running from RAM on page 59*: removed values for HSI clock source (16 MHz), Range 3. *Table 19: Current consumption in Sleep mode on page 60* removed values for HSI clock source (16 MHz), Range 3 for both RAM and Flash; changed units. *Table 20: Current consumption in Low power run mode on page 62*: updated parameter and max value of I_{DD} Max (LP Run). *Table 21: Current consumption in Low power sleep mode on page 63*: updated symbol, parameter, and max value of I_{DD} Max (LP Sleep). *Table 22: Typical and maximum current consumptions in Stop mode on page 64* updated values for $I_{DD\ (Stop\ with\ RTC)}$ - RTC clocked by LSE external clock (32.768 kHz), regulator in LP mode, HSI and HSE OFF (no independent watchdog).

Table 73. Document revision history (continued)

Date	Revision	Changes
26-Oct-2012	7	Updated cover page. Updated *Section 3.10: ADC (analog-to-digital converter)* Updated *Table 3: Functionalities depending on the operating power supply range*, added *Table 4: CPU frequency range depending on dynamic voltage scaling* and *Table 5: Working mode-dependent functionalities (from Run/active down to standby)*. Updated *Table 27: Low-speed external user clock characteristics*Added footnote *2.* in *Table 14: Embedded reset and power control block characteristics* Updated *Table 22: Typical and maximum current consumptions in Stop mode* and *Table 23: Typical and maximum current consumptions in Standby mode* Updated footnote *4.* in *Table 22: Typical and maximum current consumptions in Stop mode* Updated *Table 44: I/O AC characteristics* Updated *Table 47: I2C characteristics* Updated *Table 49: SPI characteristics* Updated *Section 6.3.9: Memory characteristics* Updated "non-robust" *Table 54: ADC characteristics* Removed the note "position of 4.7 µf capacitor" in *Section 6.1.6: Power supply scheme* Updated *Table 66: UFQFPN48 7 x 7 mm, 0.5 mm pitch, ultra thin fine-pitch quad flat no-lead package mechanical data* Updated *Table 65: LQFP48 7 x 7 mm, 48-pin low-profile quad flat package mechanical data* Added the resistance of TFBGA in *Table 71: Thermal characteristics* Added *Figure 50: Thermal resistance*
07-Feb-2013	8	Removed AHB1/AHB2 in *Figure 1: Ultralow power STM32L15xx6/8/B block diagram* Added IWDG and WWDG rows in *Table 5: Working mode-dependent functionalities (from Run/active down to standby)*. Updated I_{DD} (Supply current during wakeup time from Standby mode) in *Table 23: Typical and maximum current consumptions in Standby mode* The comment "HSE = 16 MHz(2) (PLL ON for fHCLK above 16 MHz)" replaced by "fHSE = fHCLK up to 16 MHz included, fHSE = fHCLK/2 above 16 MHz (PLL ON)(2)" in *Table 19: Current consumption in Sleep mode* Updated Stop mode current to 1.2 µA in *Ultra-low-power platform* Updated entire *Section 7: Package information* Removed alternate function "I2C2_SMBA" for GPIO pin "PH2" in *Table 8: STM32L15xx6/8/B pin definitions* Updated *Table 27: Low-speed external user clock characteristics* and definition of symbol "R_{AIN}" in *Table 54: ADC characteristics* Removed first sentence in *I2C interface characteristics*

Table 73. Document revision history (continued)

Date	Revision	Changes
30-Jan-2015	11	Updated DMIPS features in cover page and *Section 2: Description*. Updated *Table 8: STM32L151x6/8/B and STM32L152x6/8/B pin definitions* and *Table 9: Alternate function input/output* putting additional functions. Updated package top view marking in *Section 7.1: Package mechanical data*. Updated *Figure 9: Memory map*. Updated *Table 56: Maximum source impedance RAIN max* adding note 2. Updated *Table 72: Ordering information scheme*.
28-Apr-2016	12	Updated *Section 7: Package information* structure: Paragraph titles and paragraph heading level. Updated *Section 7: Package information* for all package device markings, adding text for device orientation versus pin 1/ ball A1 identifier. Updated *Figure 34: LQFP100 14 x 14 mm, 100-pin package top view example* removing gate mark. Updated *Table 64: LQFP64 10 x 10 mm, 64-pin low-profile quad flat package mechanical data*. Updated *Section 7.5: UFBGA100 7 x 7 mm, 0.5 mm pitch, ultra thin fine-pitch ball grid array package information* adding *Table 68: UFBGA100 7 x 7 mm, 0.5 mm pitch, recommended PCB design rules* and *Figure 45: UFBGA100 7 x 7 mm, 0.5 mm pitch, package recommended footprint*. Updated *Section 7.6: TFBGA64 5 x 5 mm, 0.5 mm pitch, thin fine-pitch ball grid array package information* adding *Table 70: TFBGA64 5 x 5 mm, 0.5 mm pitch, recommended PCB design rules* and changing *Figure 48: TFBGA64, 5 x 5 mm, 0.5 mm pitch, recommended footprint*. Updated *Table 16: Embedded internal reference voltage* temperature coefficient at 100ppm/°C. Updated note 3 below *Table 16*. Updated *Table 61: Comparator 2 characteristics* new maximum threshold voltage temperature coefficient at 100ppm/°C. Updated *Table 39: ESD absolute maximum ratings* CDM class. Updated all the notes, removing 'not tested in production'. Updated *Table 10: Voltage characteristics* adding note about V_{REF-} pin. Updated *Table 5: Working mode-dependent functionalities (from Run/active down to standby)* LSI and LSE functionalities putting "Y" in Standby mode. Removed note 1 below *Figure 2: Clock tree*. Updated *Table 57: DAC characteristics* resistive load.