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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 32MHz |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART, USB |
| Peripherals | Cap Sense, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 51 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 4K x 8 |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.65V ~ 3.6V |
| Data Converters | A/D 20x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l151rbt6d |

# List of tables

## 2.2 Ultra-low-power device continuum

The ultra-low-power STM32L151x6/8/B and STM32L152x6/8/B devices are fully pin-to-pin and software compatible. Besides the full compatibility within the family, the devices are part of STMicroelectronics microcontrollers ultra-low-power strategy which also includes STM8L101xx and STM8L15xx devices. The STM8L and STM32L families allow a continuum of performance, peripherals, system architecture and features.

They are all based on STMicroelectronics ultra-low leakage process.

*Note: The ultra-low-power STM32L and general-purpose STM32Fxxxx families are pin-to-pin compatible. The STM8L15xxx devices are pin-to-pin compatible with the STM8L101xx devices. Please refer to the STM32F and STM8L documentation for more information on these devices.*

### 2.2.1 Performance

All families incorporate highly energy-efficient cores with both Harvard architecture and pipelined execution: advanced STM8 core for STM8L families and ARM® Cortex®-M3 core for STM32L family. In addition specific care for the design architecture has been taken to optimize the mA/DMIPS and mA/MHz ratios.

This allows the ultra-low-power performance to range from 5 up to 33.3 DMIPs.

### 2.2.2 Shared peripherals

STM8L15xxx and STM32L1xxxx share identical peripherals which ensure a very easy migration from one family to another:

- Analog peripherals: ADC, DAC and comparators
- Digital peripherals: RTC and some communication interfaces

### 2.2.3 Common system strategy

To offer flexibility and optimize performance, the STM8L15xx and STM32L1xxxx families use a common architecture:

- Same power supply range from 1.65 V to 3.6 V, (1.65 V at power down only for STM8L15xx devices)
- Architecture optimized to reach ultra-low consumption both in low power modes and Run mode
- Fast startup strategy from low power modes
- Flexible system clock
- Ultrasafe reset: same reset strategy including power-on reset, power-down reset, brownout reset and programmable voltage detector.

### 2.2.4 Features

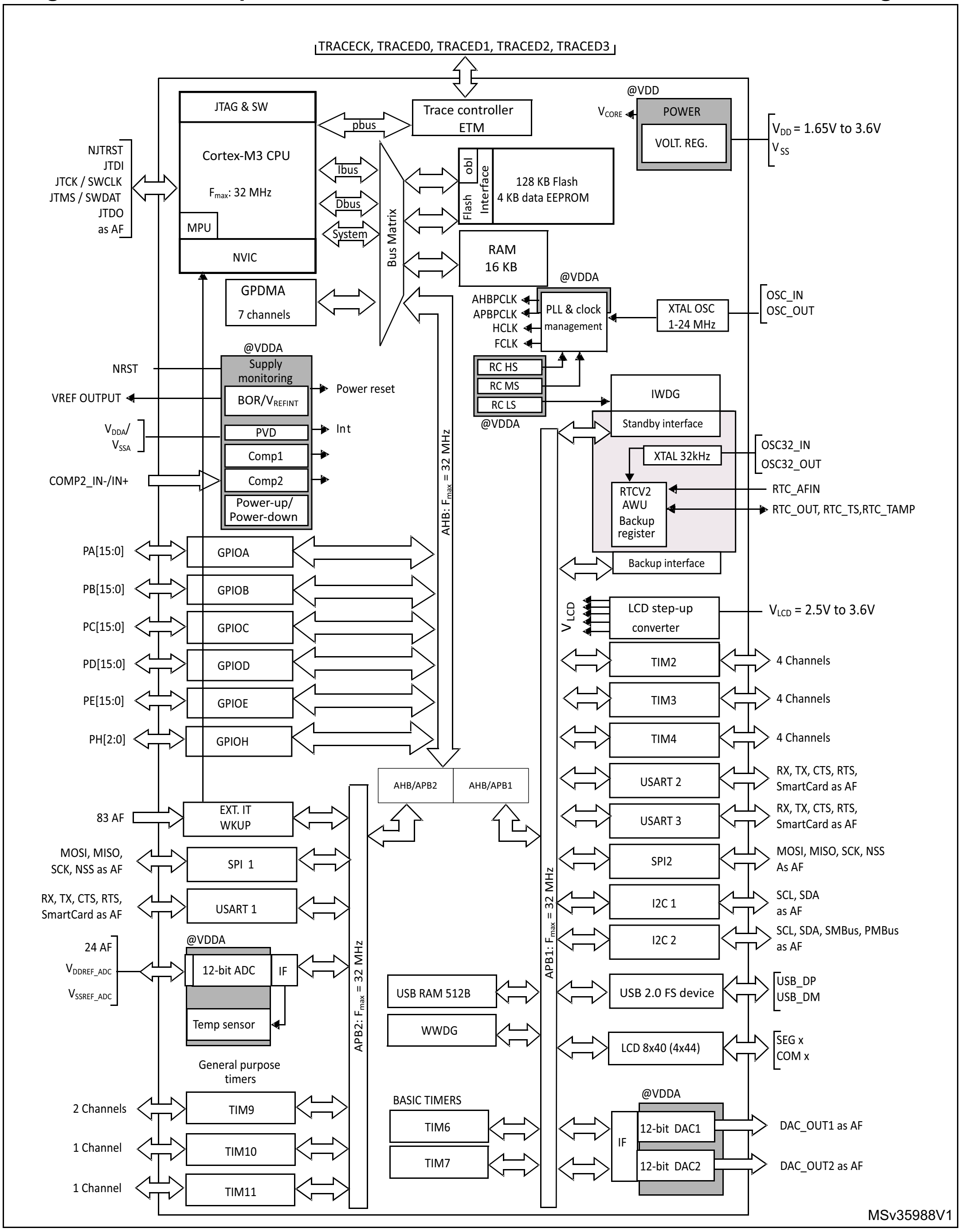
ST ultra-low-power continuum also lies in feature compatibility:

- More than 10 packages with pin count from 20 to 144 pins and size down to 3 x 3 mm
- Memory density ranging from 4 to 384 Kbytes

# 3 Functional overview

*Figure 1* shows the block diagram.

**Figure 1. Ultra-low-power STM32L151x6/8/B and STM32L152x6/8/B block diagram**




1. AF = alternate function on I/O port pin.

HSE crystal oscillators are disabled. The voltage regulator is in the low power mode. The device can be woken up from Stop mode by any of the EXTI line, in 8 µs. The EXTI line source can be one of the 16 external lines. It can be the PVD output, the Comparator 1 event or Comparator 2 event (if internal reference voltage is on). It can also be wakened by the USB wakeup.

Stop mode consumption: refer to *Table 22: Typical and maximum current consumptions in Stop mode*.

- **Standby** mode with RTC

  Standby mode is used to achieve the lowest power consumption and real time clock. The internal voltage regulator is switched off so that the entire $V_{CORE}$ domain is powered off. The PLL, MSI RC, HSI RC and HSE crystal oscillators are also switched off. The LSE or LSI is still running. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC_CSR).

  The device exits Standby mode in 60 µs when an external reset (NRST pin), an IWDG reset, a rising edge on one of the three WKUP pins, RTC alarm (Alarm A or Alarm B), RTC tamper event, RTC timestamp event or RTC Wakeup event occurs.

- **Standby** mode without RTC

  Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire $V_{CORE}$ domain is powered off. The PLL, MSI, RC, HSI and LSI RC, HSE and LSE crystal oscillators are also switched off. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC_CSR).

  The device exits Standby mode in 60 µs when an external reset (NRST pin) or a rising edge on one of the three WKUP pin occurs.

  Standby mode consumption: refer to *Table 23*.

*Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering the Stop or Standby mode.*

**Table 3. Functionalities depending on the operating power supply range**

| Operating power supply range | Functionalities depending on the operating power supply range | | | |
|---|---|---|---|---|
| | DAC and ADC operation | USB | Dynamic voltage scaling range | I/O operation |
| $V_{DD}$ = 1.65 to 1.71 V | Not functional | Not functional | Range 2 or Range 3 | Degraded speed performance |
| $V_{DD}$ = 1.71 to 1.8 V(1) | Not functional | Not functional | Range 1, Range 2 or Range 3 | Degraded speed performance |
| $V_{DD}$ = 1.8 to 2.0 V(1) | Conversion time up to 500 Ksps | Not functional | Range 1, Range 2 or Range 3 | Degraded speed performance |

Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Stop mode, it is possible to automatically switch off the internal reference voltage ($V_{REFINT}$) in Stop mode. The device remains in reset mode when $V_{DD}$ is below a specified threshold, $V_{POR/PDR}$ or $V_{BOR}$, without the need for any external reset circuit.

*Note: The start-up time at power-on is typically 3.3 ms when BOR is active at power-up, the start-up time at power-on can be decreased down to 1 ms typically for devices with BOR inactive at power-up.*

The device features an embedded programmable voltage detector (PVD) that monitors the $V_{DD}/V_{DDA}$ power supply and compares it to the $V_{PVD}$ threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when $V_{DD}/V_{DDA}$ drops below the $V_{PVD}$ threshold and/or when $V_{DD}/V_{DDA}$ is higher than the $V_{PVD}$ threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

### 3.3.3 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in Run mode (nominal regulation)
- LPR is used in the Low-power run, Low-power sleep and Stop modes
- Power down is used in Standby mode. The regulator output is high impedance, the kernel circuitry is powered down, inducing zero consumption but the contents of the registers and RAM are lost are lost except for the standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE crystal 32K osc, RCC_CSR).

### 3.3.4 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from Flash memory
- Boot from System Memory
- Boot from embedded RAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART1 or USART2. See STM32™ microcontroller system memory boot mode AN2606 for details.

## 3.7 Memories

The STM32L151x6/8/B and STM32L152x6/8/B devices have the following features:

- Up to 16 Kbytes of embedded RAM accessed (read/write) at CPU clock speed with 0 wait states. With the enhanced bus matrix, operating the RAM does not lead to any performance penalty during accesses to the system bus (AHB and APB buses).
- The non-volatile memory is divided into three arrays:
  - 32, 64 or 128 Kbytes of embedded Flash program memory
  - 4 Kbytes of data EEPROM
  - Options bytes

  The options bytes are used to write-protect the memory (with 4 Kbytes granularity) and/or readout-protect the whole memory with the following options:
  - Level 0: no readout protection
  - Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
  - Level 2: chip readout protection, debug features (Cortex®-M3 JTAG and serial wire) and boot in RAM selection disabled (JTAG fuse)

  The whole non-volatile memory embeds the error correction code (ECC) feature.

## 3.8 DMA (direct memory access)

The flexible 7-channel, general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

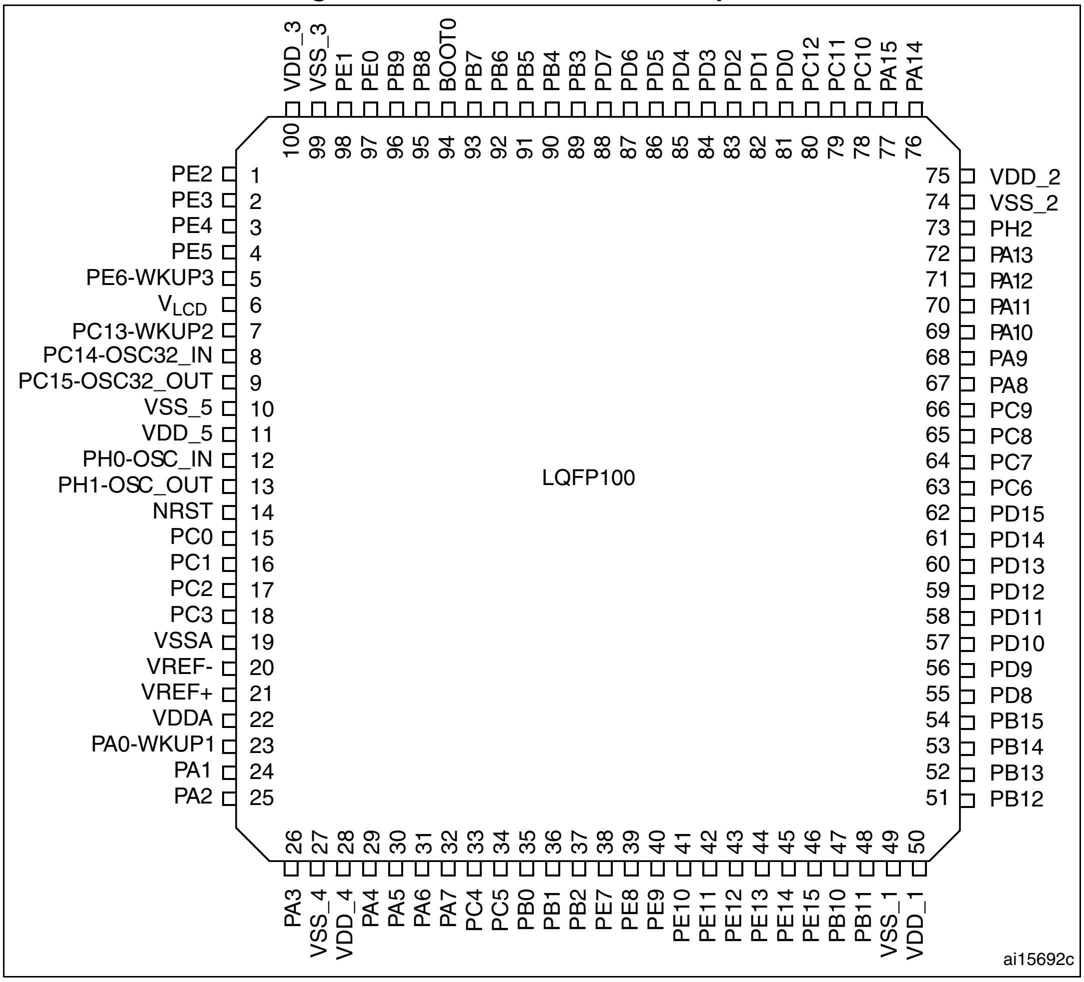
The DMA can be used with the main peripherals: SPI, I$^2$C, USART, general-purpose timers and ADC.

## 3.9 LCD (liquid crystal display)

The LCD drives up to 8 common terminals and 44 segment terminals to drive up to 320 pixels.

- Internal step-up converter to guarantee functionality and contrast control irrespective of $V_{DD}$. This converter can be deactivated, in which case the $V_{LCD}$ pin is used to provide the voltage to the LCD
- Supports static, 1/2, 1/3, 1/4 and 1/8 duty
- Supports static, 1/2, 1/3 and 1/4 bias
- Phase inversion to reduce power consumption and EMI
- Up to 8 pixels can be programmed to blink
- Unneeded segments and common pins can be used as general I/O pins
- LCD RAM can be updated at any time owing to a double-buffer
- The LCD controller can operate in Stop mode

**Figure 4. STM32L15xVx LQFP100 pinout**




1. This figure shows the package top view.

**Figure 5. STM32L15xRx TFBGA64 ballout**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| A | PC14-OSC32_IN | PC13-WKUP2 | PB9 | PB4 | PB3 | PA15 | PA14 | PA13 |
| B | PC15-OSC32_OUT | VLCD | PB8 | BOOT0 | PD2 | PC11 | PC10 | PA12 |
| C | PH0-OSC_IN | $V_{SS\_4}$ | PB7 | PB5 | PC12 | PA10 | PA9 | PA11 |
| D | PH1-OSC_OUT | $V_{DD\_4}$ | PB6 | $V_{SS\_3}$ | $V_{SS\_2}$ | $V_{SS\_1}$ | PA8 | PC9 |
| E | NRST | PC1 | PC0 | $V_{DD\_3}$ | $V_{DD\_2}$ | $V_{DD\_1}$ | PC7 | PC8 |
| F | $V_{SSA}$ | PC2 | PA2 | PA5 | PB0 | PC6 | PB15 | PB14 |
| G | $V_{REF+}$ | PA0-WKUP1 | PA3 | PA6 | PB1 | PB2 | PB10 | PB13 |
| H | $V_{DDA}$ | PA1 | PA4 | PA7 | PC4 | PC5 | PB11 | PB12 |

AI16090c

1. This figure shows the package top view.

**Table 7. Legend/abbreviations used in the pinout table**

| Name | | Abbreviation | Definition |
|---|---|---|---|
| Pin name | | Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name | |
| Pin type | | S | Supply pin |
| | | I | Input only pin |
| | | I/O | Input / output pin |
| I/O structure | | FT | 5 V tolerant I/O |
| | | TC | Standard 3.3 V I/O |
| | | B | Dedicated BOOT0 pin |
| | | RST | Bidirectional reset pin with embedded weak pull-up resistor |
| Notes | | Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset | |
| Pin functions | Alternate functions | Functions selected through GPIOx_AFR registers | |
| | Additional functions | Functions directly selected/enabled through peripheral registers | |

**Table 9. Alternate function input/output (continued)**

| Port name | Digital alternate function number | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | AFIO0 | AFIO1 | AFIO2 | AFIO3 | AFIO4 | AFIO5 | AFOI6 | AFIO7 | AFIO8 | AFIO9 | AFIO11 | AFIO12 | AFIO13 | AFIO14 | AFIO15 |
| | Alternate function | | | | | | | | | | | | | | |
| | SYSTEM | TIM2 | TIM3/4 | TIM9/10/11 | I2C1/2 | SPI1/2 | N/A | USART1/2/3 | N/A | N/A | LCD | N/A | N/A | RI | SYSTEM |
| PD13 | - | - | TIM4_CH2 | - | - | - | - | - | - | - | - | - | - | TIMx_IC2 | EVENTOUT |
| PD14 | - | - | TIM4_CH3 | - | - | - | - | - | - | - | - | - | - | TIMx_IC3 | EVENTOUT |
| PD15 | - | - | TIM4_CH4 | - | - | - | - | - | - | - | - | - | - | TIMx_IC4 | EVENTOUT |
| PE0 | - | - | TIM4_ETR | TIM10_CH1 | - | - | - | - | - | - | - | - | - | TIMx_IC1 | EVENTOUT |
| PE1 | - | - | | TIM11_CH1 | - | - | - | - | - | - | - | - | - | TIMx_IC2 | EVENTOUT |
| PE2 | TRACECK | - | TIM3_ETR | - | - | - | - | - | - | - | - | - | - | TIMx_IC3 | EVENTOUT |
| PE3 | TRACED0 | - | TIM3_CH1 | - | - | - | - | - | - | - | - | - | - | TIMx_IC4 | EVENTOUT |
| PE4 | TRACED1 | - | TIM3_CH2 | - | - | - | - | - | - | - | - | - | - | TIMx_IC1 | EVENTOUT |
| PE5 | TRACED2 | - | - | TIM9_CH1* | - | - | - | - | - | - | - | - | - | TIMx_IC2 | EVENTOUT |
| PE6 | TRACED3 | - | - | TIM9_CH2* | - | - | - | - | - | - | - | - | - | TIMx_IC3 | EVENTOUT |
| PE7 | - | - | - | - | - | - | - | - | - | - | - | - | - | TIMx_IC4 | EVENTOUT |
| PE8 | - | - | - | - | - | - | - | - | - | - | - | - | - | TIMx_IC1 | EVENTOUT |
| PE9 | - | TIM2_CH1_ETR | - | - | - | - | - | - | - | - | - | - | - | TIMx_IC2 | EVENTOUT |
| PE10 | - | TIM2_CH2 | - | - | - | - | - | - | - | - | - | - | - | TIMx_IC3 | EVENTOUT |
| PE11 | - | TIM2_CH3 | - | - | - | - | - | - | - | - | - | - | - | TIMx_IC4 | EVENTOUT |
| PE12 | - | TIM2_CH4 | - | - | - | SPI1_NSS | - | - | - | - | - | - | - | TIMx_IC1 | EVENTOUT |
| PE13 | - | - | - | - | - | SPI1_SCK | - | - | - | - | - | - | - | TIMx_IC2 | EVENTOUT |
| PE14 | - | - | - | - | - | SPI1_MISO | - | - | - | - | - | - | - | TIMx_IC3 | EVENTOUT |
| PE15 | - | - | - | - | - | SPI1_MOSI | - | - | - | - | - | - | - | TIMx_IC4 | EVENTOUT |
| PH0-OSC_IN | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |

# 5 Memory mapping

The memory map is shown in *Figure 9*.

Figure 9. Memory map

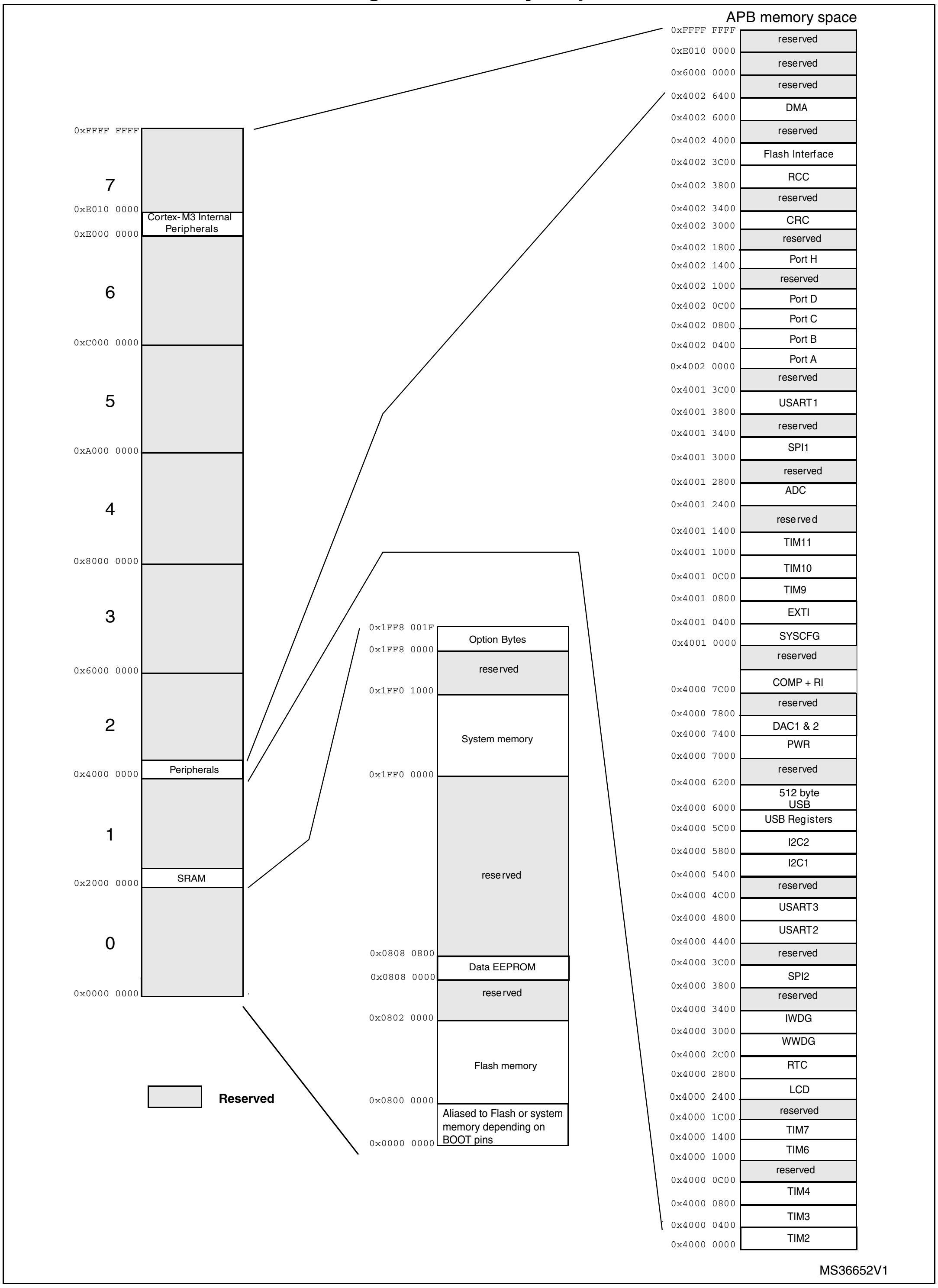


**Table 14. Embedded reset and power control block characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{PVD0}$ | Programmable voltage detector threshold 0 | Falling edge | 1.8 | 1.85 | 1.88 | V |
| | | Rising edge | 1.88 | 1.94 | 1.99 | |
| $V_{PVD1}$ | PVD threshold 1 | Falling edge | 1.98 | 2.04 | 2.09 | |
| | | Rising edge | 2.08 | 2.14 | 2.18 | |
| $V_{PVD2}$ | PVD threshold 2 | Falling edge | 2.20 | 2.24 | 2.28 | |
| | | Rising edge | 2.28 | 2.34 | 2.38 | |
| $V_{PVD3}$ | PVD threshold 3 | Falling edge | 2.39 | 2.44 | 2.48 | |
| | | Rising edge | 2.47 | 2.54 | 2.58 | |
| $V_{PVD4}$ | PVD threshold 4 | Falling edge | 2.57 | 2.64 | 2.69 | |
| | | Rising edge | 2.68 | 2.74 | 2.79 | |
| $V_{PVD5}$ | PVD threshold 5 | Falling edge | 2.77 | 2.83 | 2.88 | |
| | | Rising edge | 2.87 | 2.94 | 2.99 | |
| $V_{PVD6}$ | PVD threshold 6 | Falling edge | 2.97 | 3.05 | 3.09 | |
| | | Rising edge | 3.08 | 3.15 | 3.20 | |
| $V_{hyst}$ | Hysteresis voltage | BOR0 threshold | - | 40 | - | mV |
| | | All BOR and PVD thresholds excepting BOR0 | - | 100 | - | |

1. Guaranteed by characterization results.
2. Valid for device version without BOR at power up. Please see option "T" in Ordering information scheme for more details.

Table 23. Typical and maximum current consumptions in Standby mode

| Symbol | Parameter | Conditions | | Typ[1] | Max [1][2] | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ (Standby with RTC) | Supply current in Standby mode with RTC enabled | RTC clocked by LSI (no independent watchdog) | $T_A$ = -40 °C to 25 °C $V_{DD}$ = 1.8 V | 0.9 | - | µA |
| | | | $T_A$ = -40 °C to 25 °C | 1.1 | 1.8 | |
| | | | $T_A$ = 55 °C | 1.42 | 2.5 | |
| | | | $T_A$= 85 °C | 1.87 | 3 | |
| | | | $T_A$ = 105 °C | 2.78 | 5 | |
| | | RTC clocked by LSE (no independent watchdog)[3] | $T_A$ = -40 °C to 25 °C $V_{DD}$ = 1.8 V | 1 | - | |
| | | | $T_A$ = -40 °C to 25 °C | 1.33 | 2.9 | |
| | | | $T_A$ = 55 °C | 1.59 | 3.4 | |
| | | | $T_A$= 85 °C | 2.01 | 4.3 | |
| | | | $T_A$ = 105 °C | 3.27 | 6.3 | |
| $I_{DD}$ (Standby) | Supply current in Standby mode with RTC disabled | Independent watchdog and LSI enabled | $T_A$ = -40 °C to 25 °C | 1.1 | 1.6 | |
| | | Independent watchdog and LSI OFF | $T_A$ = -40 °C to 25 °C | 0.3 | 0.55 | |
| | | | $T_A$ = 55 °C | 0.5 | 0.8 | |
| | | | $T_A$ = 85 °C | 1 | 1.7 | |
| | | | $T_A$ = 105 °C | 2.5 | 4[4] | |
| $I_{DD}$ (WU from Standby) | RMS supply current during wakeup time when exiting from Standby mode | - | $V_{DD}$ = 3.0 V $T_A$ = -40 °C to 25 °C | 1 | - | |

1. The typical values are given for $V_{DD}$ = 3.0 V and max values are given for $V_{DD}$ = 3.6 V, unless otherwise specified.
2. Guaranteed by characterization results, unless otherwise specified.
3. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8pF loading capacitors.
4. Tested in production.

### On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in the following table. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at $V_{DD}$ or $V_{SS}$ (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on

### 6.3.9 Memory characteristics

The characteristics are given at $T_A$ = -40 to 105 °C unless otherwise specified.

#### RAM memory

**Table 34. RAM and hardware registers**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| VRM | Data retention mode(1) | STOP mode (or RESET) | 1.65 | - | - | V |

1. Minimum supply voltage without losing data stored in RAM (in Stop mode or under Reset) or in hardware registers (only in Stop mode).

#### Flash memory and data EEPROM

**Table 35. Flash memory and data EEPROM characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Operating voltage<br>Read / Write / Erase | - | 1.65 | - | 3.6 | V |
| $t_{prog}$ | Programming / erasing time for byte / word / double word / half-page | Erasing | - | 3.28 | 3.94 | ms |
| | | Programming | - | 3.28 | 3.94 | |
| $I_{DD}$ | Average current during whole program/erase operation | $T_A$ = 25 °C, $V_{DD}$ = 3.6 V | - | 300 | - | µA |
| | Maximum current (peak) during program/erase operation | | - | 1.5 | 2.5 | mA |

1. Guaranteed by design.

**Table 36. Flash memory, data EEPROM endurance and data retention**

| Symbol | Parameter | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min(1) | Typ | Max | |
| NCYC(2) | Cycling (erase / write)<br>Program memory | $T_A$ = -40°C to 105 °C | 10 | - | - | kcycles |
| | Cycling (erase / write)<br>EEPROM data memory | | 300 | - | - | |
| $t_{RET}$(2) | Data retention (program memory) after 10 kcycles at $T_A$ = 85 °C | TRET = +85 °C | 30 | - | - | years |
| | Data retention (EEPROM data memory) after 300 kcycles at $T_A$ = 85 °C | | 30 | - | - | |
| | Data retention (program memory) after 10 kcycles at $T_A$ = 105 °C | TRET = +105 °C | 10 | - | - | |
| | Data retention (EEPROM data memory) after 300 kcycles at $T_A$ = 105 °C | | 10 | - | - | |

1. Guaranteed by characterization results.
2. Characterization is done according to JEDEC JESD22-A117.

## Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 19* and *Table 44*, respectively.

Unless otherwise specified, the parameters given in *Table 44* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 13*.

**Table 44. I/O AC characteristics(1)**

| OSPEEDRx [1:0] bit value(1) | Symbol | Parameter | Conditions | Min | Max(2) | Unit |
|---|---|---|---|---|---|---|
| 00 | $f_{max(IO)out}$ | Maximum frequency(3) | $C_L$ = 50 pF, $V_{DD}$ = 2.7 V to 3.6 V | - | 400 | kHz |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 1.65 V to 2.7 V | - | 400 | |
| | $t_{f(IO)out}$<br>$t_{r(IO)out}$ | Output rise and fall time | $C_L$ = 50 pF, $V_{DD}$ = 2.7 V to 3.6 V | - | 625 | ns |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 1.65 V to 2.7 V | - | 625 | |
| 01 | $f_{max(IO)out}$ | Maximum frequency(3) | $C_L$ = 50 pF, $V_{DD}$ = 2.7 V to 3.6 V | - | 2 | MHz |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 1.65 V to 2.7 V | - | 1 | |
| | $t_{f(IO)out}$<br>$t_{r(IO)out}$ | Output rise and fall time | $C_L$ = 50 pF, $V_{DD}$ = 2.7 V to 3.6 V | - | 125 | ns |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 1.65 V to 2.7 V | - | 250 | |
| 10 | $F_{max(IO)out}$ | Maximum frequency(3) | $C_L$ = 50 pF, $V_{DD}$ = 2.7 V to 3.6 V | - | 10 | MHz |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 1.65 V to 2.7 V | - | 2 | |
| | $t_{f(IO)out}$<br>$t_{r(IO)out}$ | Output rise and fall time | $C_L$ = 50 pF, $V_{DD}$ = 2.7 V to 3.6 V | - | 25 | ns |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 1.65 V to 2.7 V | - | 125 | |
| 11 | $F_{max(IO)out}$ | Maximum frequency(3) | $C_L$ = 50 pF, $V_{DD}$ = 2.7 V to 3.6 V | - | 50 | MHz |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 1.65 V to 2.7 V | - | 8 | |
| | $t_{f(IO)out}$<br>$t_{r(IO)out}$ | Output rise and fall time | $C_L$ = 30 pF, $V_{DD}$ = 2.7 V to 3.6 V | - | 5 | ns |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 1.65 V to 2.7 V | - | 30 | |
| - | $t_{EXTIpw}$ | Pulse width of external signals detected by the EXTI controller | - | 8 | - | |

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the STM32L151x6/8/B and STM32L152x6/8/B reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design.
3. The maximum frequency is defined in *Figure 19*.

## SPI characteristics

Unless otherwise specified, the parameters given in the following table are derived from tests performed under ambient temperature, $f_{PCLKx}$ frequency and $V_{DD}$ supply voltage conditions summarized in Table 13.

Refer to Section 6.3.12: I/O current injection characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

**Table 49. SPI characteristics(1)**

| Symbol | Parameter | Conditions | Min | Max(2) | Unit |
|---|---|---|---|---|---|
| $f_{SCK}$ $1/t_{c(SCK)}$ | SPI clock frequency | Master mode | - | 16 | MHz |
| | | Slave mode | - | 16 | |
| | | Slave transmitter | - | 12(3) | |
| $t_{r(SCK)}$(2) $t_{f(SCK)}$(2) | SPI clock rise and fall time | Capacitive load: C = 30 pF | - | 6 | ns |
| DuCy(SCK) | SPI slave input clock duty cycle | Slave mode | 30 | 70 | % |
| $t_{su(NSS)}$ | NSS setup time | Slave mode | $4t_{HCLK}$ | - | ns |
| $t_{h(NSS)}$ | NSS hold time | Slave mode | $2t_{HCLK}$ | - | |
| $t_{w(SCKH)}$(2) $t_{w(SCKL)}$(2) | SCK high and low time | Master mode | $t_{SCK}/2-5$ | $t_{SCK}/2+3$ | |
| $t_{su(MI)}$(2) | Data input setup time | Master mode | 5 | - | |
| $t_{su(SI)}$(2) | | Slave mode | 6 | - | |
| $t_{h(MI)}$(2) | Data input hold time | Master mode | 5 | - | |
| $t_{h(SI)}$(2) | | Slave mode | 5 | - | |
| $t_{a(SO)}$(4) | Data output access time | Slave mode | 0 | $3t_{HCLK}$ | |
| $t_{v(SO)}$(2) | Data output valid time | Slave mode | - | 33 | |
| $t_{v(MO)}$(2) | Data output valid time | Master mode | - | 6.5 | |
| $t_{h(SO)}$(2) | Data output hold time | Slave mode | 17 | - | |
| $t_{h(MO)}$(2) | | Master mode | 0.5 | - | |

1. The characteristics above are given for voltage Range 1.
2. Guaranteed by characterization results.
3. The maximum SPI clock frequency in slave transmitter mode is given for an SPI slave input clock duty cycle (DuCy(SCK)) ranging between 40 to 60%.
4. Min time is for the minimum time to drive the output and max time is for the maximum time to validate the data.

Table 51. USB DC electrical characteristics

| Symbol | Parameter | Conditions | Min.(1) | Max.(1) | Unit |
|---|---|---|---|---|---|
| **Input levels** | | | | | |
| $V_{DD}$ | USB operating voltage(2) | - | 3.0 | 3.6 | V |
| $V_{DI}$(3) | Differential input sensitivity | I(USB_DP, USB_DM) | 0.2 | - | |
| $V_{CM}$(3) | Differential common mode range | Includes $V_{DI}$ range | 0.8 | 2.5 | V |
| $V_{SE}$(3) | Single ended receiver threshold | - | 1.3 | 2.0 | |
| **Output levels** | | | | | |
| $V_{OL}$(4) | Static output level low | $R_L$ of 1.5 kΩ to 3.6 V(5) | - | 0.3 | V |
| $V_{OH}$(4) | Static output level high | $R_L$ of 15 kΩ to $V_{SS}$(5) | 2.8 | 3.6 | |

1. All the voltages are measured from the local ground potential.
2. To be compliant with the USB 2.0 full speed electrical specification, the USB_DP (D+) pin should be pulled up with a 1.5 kΩ resistor to a 3.0-to-3.6 V voltage range.
3. Guaranteed by characterization results.
4. Tested in production.
5. $R_L$ is the load connected on the USB drivers.

Figure 25. USB timings: definition of data signal rise and fall time

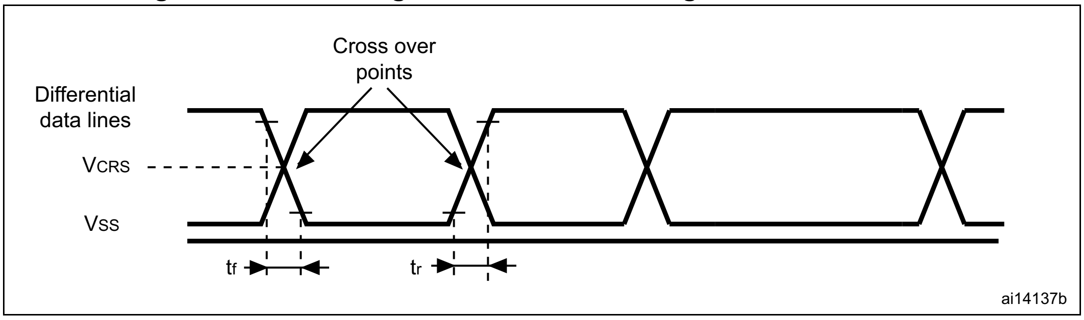


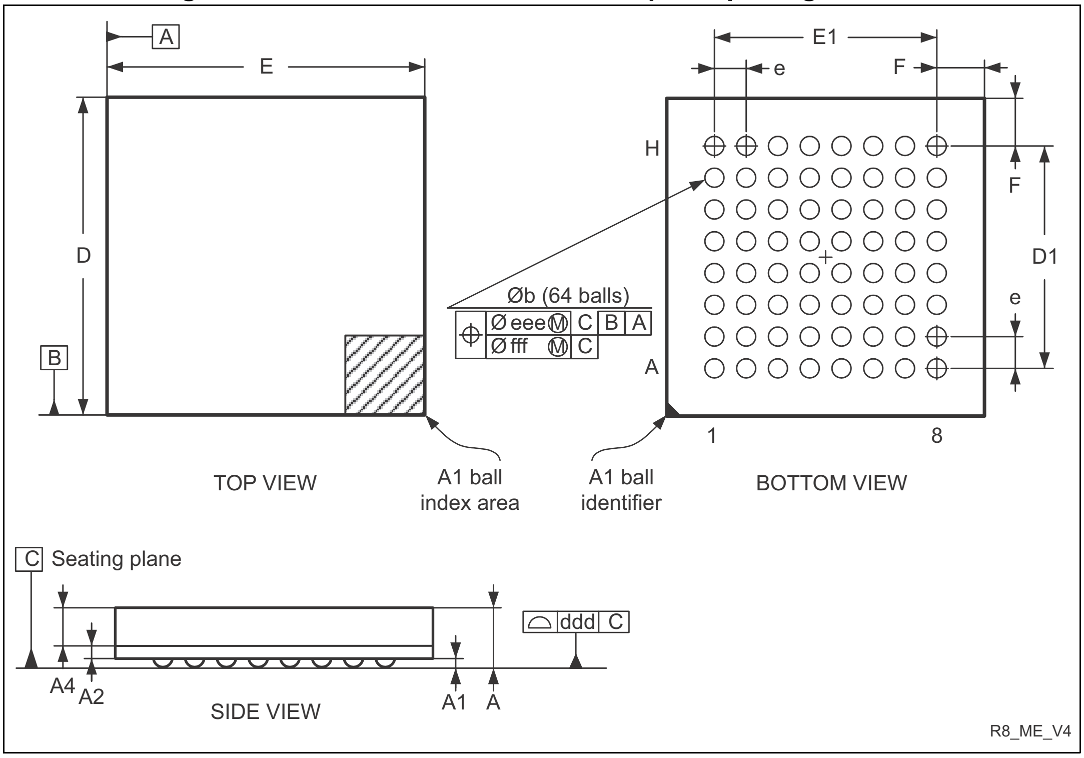

Table 52. USB: full speed electrical characteristics

| Driver characteristics(1) | | | | | |
|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Unit** |
| $t_r$ | Rise time(2) | $C_L$ = 50 pF | 4 | 20 | ns |
| $t_f$ | Fall Time(2) | $C_L$ = 50 pF | 4 | 20 | ns |
| $t_{rfm}$ | Rise/ fall time matching | $t_r/t_f$ | 90 | 110 | % |
| $V_{CRS}$ | Output signal crossover voltage | | 1.3 | 2.0 | V |

1. Guaranteed by design.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

## 7.6 TFBGA64 5 x 5 mm, 0.5 mm pitch, thin fine-pitch ball grid array package information

**Figure 47. TFBGA64 5 x 5 mm, 0.5 mm pitch, package outline**




1. Drawing is not to scale.

**Table 69. TFBGA64 5 x 5 mm, 0.5 mm pitch, package mechanical data**

| Symbol | millimeters | | | inches(1) | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.200 | - | - | 0.0472 |
| A1 | 0.150 | - | - | 0.0059 | - | - |
| A2 | - | 0.200 | - | - | 0.0079 | - |
| A4 | - | - | 0.600 | - | - | 0.0236 |
| b | 0.250 | 0.300 | 0.350 | 0.0098 | 0.0118 | 0.0138 |
| D | 4.850 | 5.000 | 5.150 | 0.1909 | 0.1969 | 0.2028 |
| D1 | - | 3.500 | - | - | 0.1378 | - |
| E | 4.850 | 5.000 | 5.150 | 0.1909 | 0.1969 | 0.2028 |
| E1 | - | 3.500 | - | - | 0.1378 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| F | - | 0.750 | - | - | 0.0295 | - |
| ddd | - | - | 0.080 | - | - | 0.0031 |

# 9 Revision history

**Table 73. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 02-Jul-2010 | 1 | Initial release. |
| 01-Oct-2010 | 2 | Removed 5 V tolerance (FT) from PA3, PB0 and PC3 in *Table 8: STM32L15xx6/8/B pin definitions*<br>Updated *Table 14: Embedded reset and power control block characteristics*<br>Updated *Table 16: Embedded internal reference voltage*<br>Added *Table 53: ADC clock frequency*<br>Updated *Table 54: ADC characteristics* |
| 16-Dec-2010 | 3 | Modified consumptions on page 1 and in *Section 3.1: Low power modes*<br>LED_SEG8 removed on PB6.<br>Updated *Section 6: Electrical characteristics*<br>VFQFPN48 replaced by UFQFPN48 |
| 25-Feb-2011 | 4 | *Section 3.3.2: Power supply supervisor*: updated note.<br>*Table 8: STM32L15xx6/8/B pin definitions:* modified main function (after reset) and alternate function for OSC_IN and OSC_OUT pins; modified footnote 5; added footnote to OSC32_IN and OSC32_OUT pins; C1 and D1 removed on PD0 and PD1 pins (TFBGA64 column).<br>*Section 3.11: DAC (digital-to-analog converter)*: updated bullet list.<br>*Table 10: Voltage characteristics on page 52*: updated footnote 3 regarding $I_{INJ(PIN)}$.<br>*Table 11: Current characteristics on page 52*: updated footnote 4 regarding positive and negative injection.<br>*Table 14: Embedded reset and power control block characteristics on page 54*: updated typ and max values for $T_{RSTTEMPO}$ ($V_{DD}$ rising, BOR enabled).<br>*Table 17: Current consumption in Run mode, code with data processing running from Flash on page 58*: removed values for HSI clock source (16 MHz), Range 3.<br>*Table 18: Current consumption in Run mode, code with data processing running from RAM on page 59*: removed values for HSI clock source (16 MHz), Range 3.<br>*Table 19: Current consumption in Sleep mode on page 60* removed values for HSI clock source (16 MHz), Range 3 for both RAM and Flash; changed units.<br>*Table 20: Current consumption in Low power run mode on page 62*: updated parameter and max value of $I_{DD}$ Max (LP Run).<br>*Table 21: Current consumption in Low power sleep mode on page 63*: updated symbol, parameter, and max value of $I_{DD}$ Max (LP Sleep).<br>*Table 22: Typical and maximum current consumptions in Stop mode on page 64* updated values for $I_{DD\ (Stop\ with\ RTC)}$ - RTC clocked by LSE external clock (32.768 kHz), regulator in LP mode, HSI and HSE OFF (no independent watchdog). |

Table 73. Document revision history (continued)

| Date | Revision | Changes |
|---|---|---|
| 30-Jan-2015 | 11 | Updated DMIPS features in cover page and *Section 2: Description*.<br>Updated *Table 8: STM32L151x6/8/B and STM32L152x6/8/B pin definitions* and *Table 9: Alternate function input/output* putting additional functions.<br>Updated package top view marking in *Section 7.1: Package mechanical data*.<br>Updated *Figure 9: Memory map*.<br>Updated *Table 56: Maximum source impedance RAIN max* adding note 2.<br>Updated *Table 72: Ordering information scheme*. |
| 28-Apr-2016 | 12 | Updated *Section 7: Package information* structure: Paragraph titles and paragraph heading level.<br>Updated *Section 7: Package information* for all package device markings, adding text for device orientation versus pin 1/ ball A1 identifier.<br>Updated *Figure 34: LQFP100 14 x 14 mm, 100-pin package top view example* removing gate mark.<br>Updated *Table 64: LQFP64 10 x 10 mm, 64-pin low-profile quad flat package mechanical data*.<br>Updated *Section 7.5: UFBGA100 7 x 7 mm, 0.5 mm pitch, ultra thin fine-pitch ball grid array package information* adding *Table 68: UFBGA100 7 x 7 mm, 0.5 mm pitch, recommended PCB design rules* and *Figure 45: UFBGA100 7 x 7 mm, 0.5 mm pitch, package recommended footprint*.<br>Updated *Section 7.6: TFBGA64 5 x 5 mm, 0.5 mm pitch, thin fine-pitch ball grid array package information* adding *Table 70: TFBGA64 5 x 5 mm, 0.5 mm pitch, recommended PCB design rules* and changing *Figure 48: TFBGA64, 5 x 5 mm, 0.5 mm pitch, recommended footprint*.<br>Updated *Table 16: Embedded internal reference voltage* temperature coefficient at 100ppm/°C.<br>Updated note 3 below *Table 16*.<br>Updated *Table 61: Comparator 2 characteristics* new maximum threshold voltage temperature coefficient at 100ppm/°C.<br>Updated *Table 39: ESD absolute maximum ratings* CDM class.<br>Updated all the notes, removing ‘not tested in production’.<br>Updated *Table 10: Voltage characteristics* adding note about $V_{REF-}$ pin.<br>Updated *Table 5: Working mode-dependent functionalities (from Run/active down to standby)* LSI and LSE functionalities putting “Y” in Standby mode.<br>Removed note 1 below *Figure 2: Clock tree*.<br>Updated *Table 57: DAC characteristics* resistive load. |