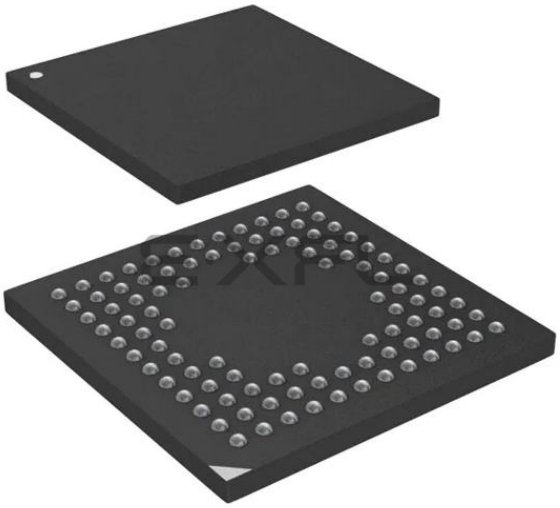

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 32MHz |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, Cap Sense, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 83 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 4K x 8 |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 24x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-UFBGA |
| Supplier Device Package | 100-UFBGA (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l151vbh6 |

Figure 48. TFBGA64, 5 x 5 mm, 0.5 mm pitch, recommended footprint . . . . . 121
Figure 49. TFBGA64 5 x 5 mm, 0.5 mm pitch, package top view example . . . . . 122
Figure 50. Thermal resistance . . . . . 124

HSE crystal oscillators are disabled. The voltage regulator is in the low power mode. The device can be woken up from Stop mode by any of the EXTI line, in 8 µs. The EXTI line source can be one of the 16 external lines. It can be the PVD output, the Comparator 1 event or Comparator 2 event (if internal reference voltage is on). It can also be wakened by the USB wakeup.

Stop mode consumption: refer to *Table 22: Typical and maximum current consumptions in Stop mode*.

- **Standby** mode with RTC

  Standby mode is used to achieve the lowest power consumption and real time clock. The internal voltage regulator is switched off so that the entire $V_{CORE}$ domain is powered off. The PLL, MSI RC, HSI RC and HSE crystal oscillators are also switched off. The LSE or LSI is still running. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC_CSR).

  The device exits Standby mode in 60 µs when an external reset (NRST pin), an IWDG reset, a rising edge on one of the three WKUP pins, RTC alarm (Alarm A or Alarm B), RTC tamper event, RTC timestamp event or RTC Wakeup event occurs.

- **Standby** mode without RTC

  Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire $V_{CORE}$ domain is powered off. The PLL, MSI, RC, HSI and LSI RC, HSE and LSE crystal oscillators are also switched off. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC_CSR).

  The device exits Standby mode in 60 µs when an external reset (NRST pin) or a rising edge on one of the three WKUP pin occurs.

  Standby mode consumption: refer to *Table 23*.

*Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering the Stop or Standby mode.*

**Table 3. Functionalities depending on the operating power supply range**

| Operating power supply range | Functionalities depending on the operating power supply range | | | |
|---|---|---|---|---|
| | DAC and ADC operation | USB | Dynamic voltage scaling range | I/O operation |
| $V_{DD}$ = 1.65 to 1.71 V | Not functional | Not functional | Range 2 or Range 3 | Degraded speed performance |
| $V_{DD}$ = 1.71 to 1.8 V(1) | Not functional | Not functional | Range 1, Range 2 or Range 3 | Degraded speed performance |
| $V_{DD}$ = 1.8 to 2.0 V(1) | Conversion time up to 500 Ksps | Not functional | Range 1, Range 2 or Range 3 | Degraded speed performance |

### 3.15.1 General-purpose timers (TIM2, TIM3, TIM4, TIM9, TIM10 and TIM11)

There are six synchronizable general-purpose timers embedded in the STM32L151x6/8/B and STM32L152x6/8/B devices (see *Table 6* for differences).

#### TIM2, TIM3, TIM4

These timers are based on a 16-bit auto-reload up/down-counter and a 16-bit prescaler. They feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.

The TIM2, TIM3, TIM4 general-purpose timers can work together or with the TIM10, TIM11 and TIM9 general-purpose timers via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs.

TIM2, TIM3, TIM4 all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

#### TIM10, TIM11 and TIM9

These timers are based on a 16-bit auto-reload up-counter and a 16-bit prescaler. They include a 16-bit prescaler. TIM10 and TIM11 feature one independent channel, whereas TIM9 has two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4 full-featured general-purpose timers.

They can also be used as simple time bases and be clocked by the LSE clock source (32.768 kHz) to provide time bases independent from the main CPU clock.

### 3.15.2 Basic timers (TIM6 and TIM7)

These timers are mainly used for DAC trigger generation. They can also be used as generic 16-bit time bases.

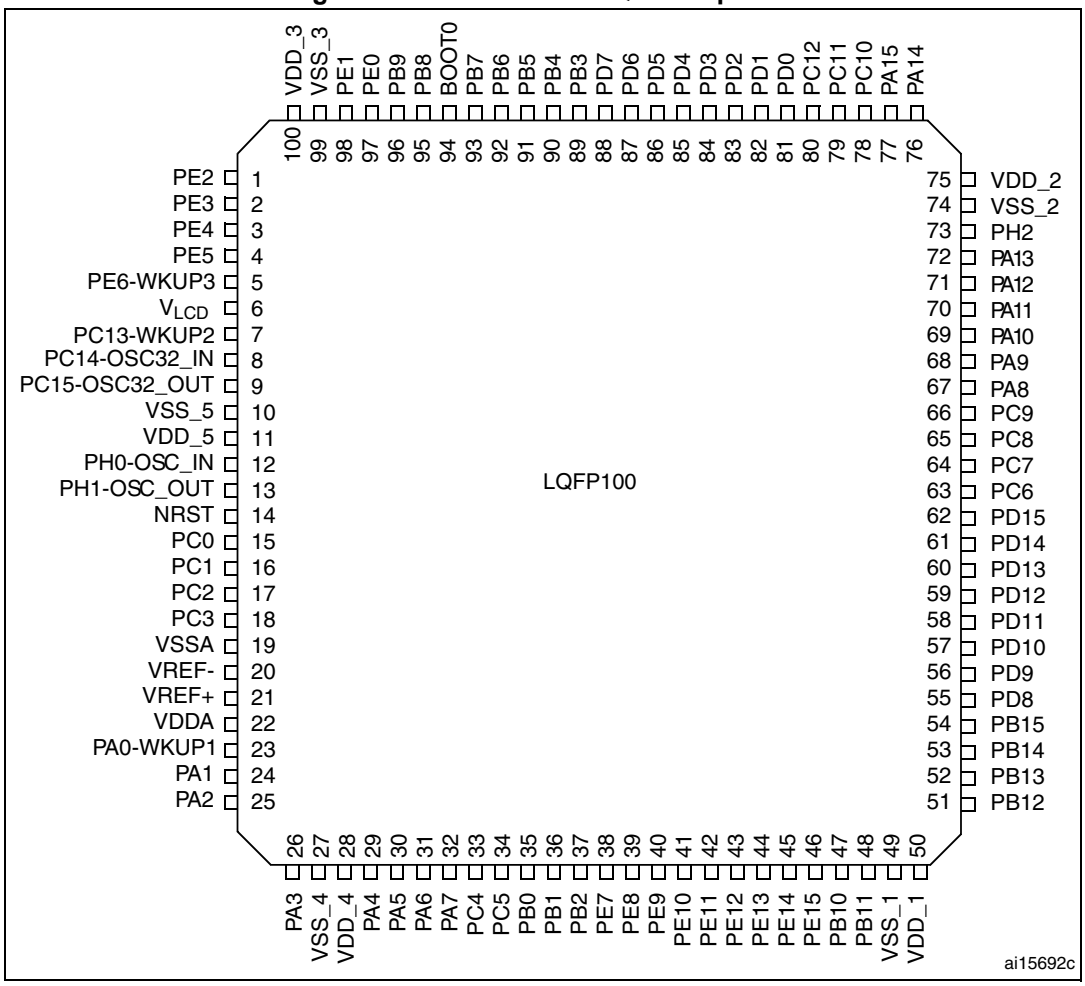
### 3.15.3 SysTick timer

This timer is dedicated to the OS, but could also be used as a standard downcounter. It is based on a 24-bit down-counter with autoreload capability and a programmable clock source. It features a maskable system interrupt generation when the counter reaches 0.

### 3.15.4 Independent watchdog (IWDG)

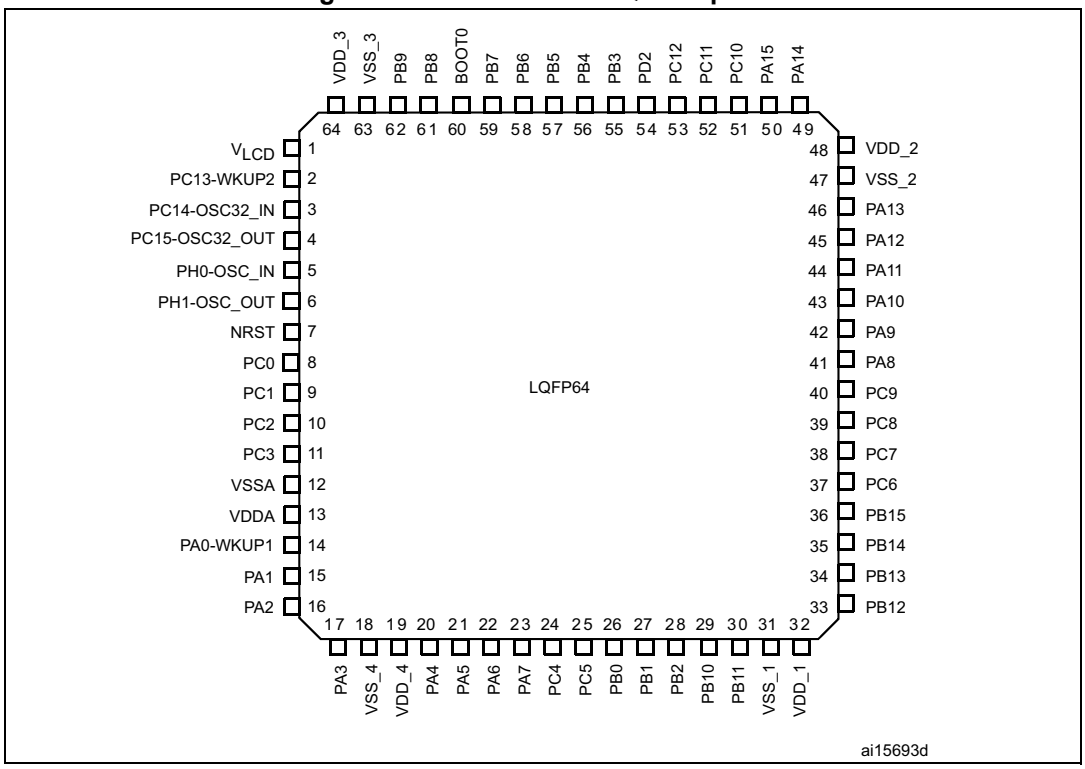
The independent watchdog is based on a 12-bit down-counter and 8-bit prescaler. It is clocked from an independent 37 kHz internal RC and, as it operates independently of the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes. The counter can be frozen in debug mode.

**Figure 4. STM32L15xVx LQFP100 pinout**



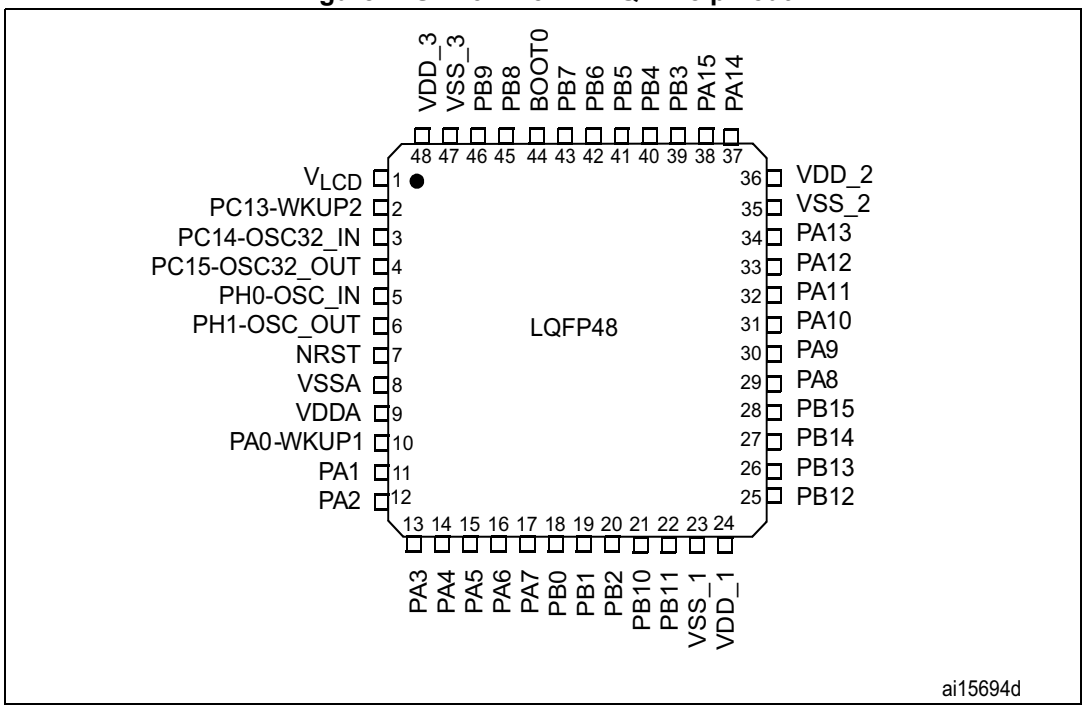

1. This figure shows the package top view.

**Figure 6. STM32L15xRx LQFP64 pinout**




1. This figure shows the package top view.

**Figure 7. STM32L15xCx LQFP48 pinout**




1. This figure shows the package top view.

**Table 7. Legend/abbreviations used in the pinout table**

| Name | | Abbreviation | Definition |
|---|---|---|---|
| Pin name | | Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name | |
| Pin type | | S | Supply pin |
| | | I | Input only pin |
| | | I/O | Input / output pin |
| I/O structure | | FT | 5 V tolerant I/O |
| | | TC | Standard 3.3 V I/O |
| | | B | Dedicated BOOT0 pin |
| | | RST | Bidirectional reset pin with embedded weak pull-up resistor |
| Notes | | Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset | |
| Pin functions | Alternate functions | Functions selected through GPIOx_AFR registers | |
| | Additional functions | Functions directly selected/enabled through peripheral registers | |

**Table 9. Alternate function input/output (continued)**

| Port name | Digital alternate function number | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | AFIO0 | AFIO1 | AFIO2 | AFIO3 | AFIO4 | AFIO5 | AFOI6 | AFIO7 | AFIO8 | AFIO9 | AFIO11 | AFIO12 | AFIO13 | AFIO14 | AFIO15 |
| | Alternate function | | | | | | | | | | | | | | |
| | SYSTEM | TIM2 | TIM3/4 | TIM9/10/11 | I2C1/2 | SPI1/2 | N/A | USART1/2/3 | N/A | N/A | LCD | N/A | N/A | RI | SYSTEM |
| PH1-OSC_OUT | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| PH2 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |

# 6 Electrical characteristics

## 6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to $V_{SS}$.

### 6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A$ = 25 °C and $T_A$ = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

Please refer to device ErrataSheet for possible latest changes of electrical characteristics.

### 6.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A$ = 25 °C, $V_{DD}$ = 3.6 V (for the 1.65 V ≤ $V_{DD}$ ≤ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

### 6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

### 6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 10*.

### 6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 11*.

**Figure 10. Pin loading conditions**

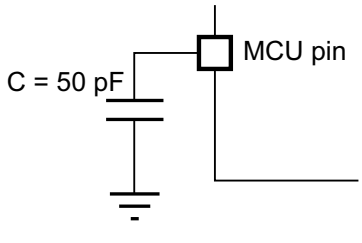



**Figure 11. Pin input voltage**

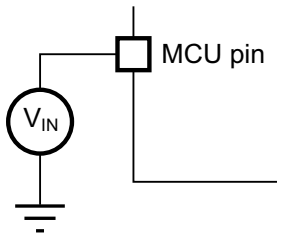


**Table 21. Current consumption in Low power sleep mode**

| Symbol | Parameter | Conditions | | | Typ | Max (1) | Unit |
|---|---|---|---|---|---|---|---|
| $I_{DD}$ (LP Sleep) | Supply current in Low power sleep mode | All peripherals OFF, $V_{DD}$ from 1.65 V to 3.6 V | MSI clock, 65 kHz $f_{HCLK}$ = 32 kHz Flash OFF | $T_A$ = -40 °C to 25 °C | 4.4 | - | µA |
| | | | MSI clock, 65 kHz $f_{HCLK}$ = 32 kHz Flash ON | $T_A$ = -40 °C to 25 °C | 17.5 | 25 | |
| | | | | $T_A$ = 85 °C | 22 | 27 | |
| | | | | $T_A$ = 105 °C | 31 | 39 | |
| | | | MSI clock, 65 kHz $f_{HCLK}$ = 65 kHz, Flash ON | $T_A$ = -40 °C to 25 °C | 18 | 26 | |
| | | | | $T_A$ = 85 °C | 23 | 28 | |
| | | | | $T_A$ = 105 °C | 31 | 40 | |
| | | | MSI clock, 131 kHz $f_{HCLK}$ = 131 kHz, Flash ON | $T_A$ = -40 °C to 25 °C | 22 | 30 | |
| | | | | $T_A$ = 55 °C | 24 | 32 | |
| | | | | $T_A$ = 85 °C | 26 | 34 | |
| | | | | $T_A$ = 105 °C | 34 | 45 | |
| | | TIM9 and USART1 enabled, Flash ON, $V_{DD}$ from 1.65 V to 3.6 V | MSI clock, 65 kHz $f_{HCLK}$ = 32 kHz | $T_A$ = -40 °C to 25 °C | 17.5 | 25 | |
| | | | | $T_A$ = 85 °C | 22 | 27 | |
| | | | | $T_A$ = 105 °C | 31 | 39 | |
| | | | MSI clock, 65 kHz $f_{HCLK}$ = 65 kHz | $T_A$ = -40 °C to 25 °C | 18 | 26 | |
| | | | | $T_A$ = 85 °C | 23 | 28 | |
| | | | | $T_A$ = 105 °C | 31 | 40 | |
| | | | MSI clock, 131 kHz $f_{HCLK}$ = 131 kHz | $T_A$ = -40 °C to 25 °C | 22 | 30 | |
| | | | | $T_A$ = 55 °C | 24 | 32 | |
| | | | | $T_A$ = 85 °C | 26 | 34 | |
| | | | | $T_A$ = 105 °C | 34 | 45 | |
| $I_{DD}$ Max (LP Sleep) | Max allowed current in Low power Sleep mode | $V_{DD}$ from 1.65 V to 3.6 V | - | - | - | 200 | |

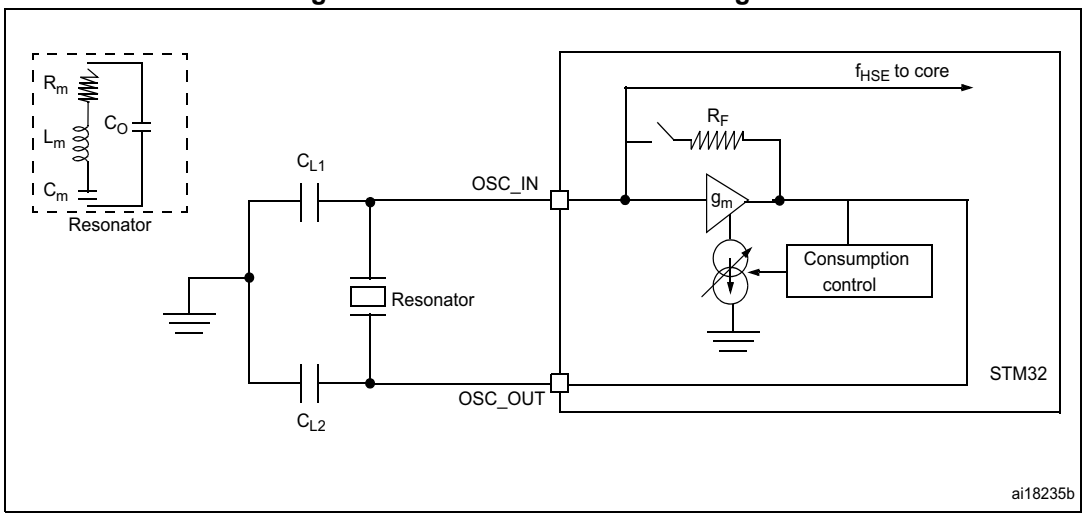
1. Guaranteed by characterization results, unless otherwise specified.

**Table 24. Peripheral current consumption(1) (continued)**

| Peripheral | | Typical consumption, $V_{DD}$ = 3.0 V, $T_A$ = 25 °C | | | | Unit |
|---|---|---|---|---|---|---|
| | | Range 1, $V_{CORE}$=1.8 V VOS[1:0] = 01 | Range 2, $V_{CORE}$=1.5 V VOS[1:0] = 10 | Range 3, $V_{CORE}$=1.2 V VOS[1:0] = 11 | Low power sleep and run | |
| AHB | GPIOA | 5 | 4.5 | 3.5 | 4 | µA/MHz ($f_{HCLK}$) |
| | GPIOB | 5 | 4.5 | 3.5 | 4.5 | |
| | GPIOC | 5 | 4.5 | 3.5 | 4.5 | |
| | GPIOD | 5 | 4.5 | 3.5 | 4.5 | |
| | GPIOE | 5 | 4.5 | 3.5 | 4.5 | |
| | GPIOH | 4 | 4 | 3 | 3.5 | |
| | CRC | 1 | 0.5 | 0.5 | 0.5 | |
| | FLASH | 13 | 11.5 | 9 | 18.5 | |
| | DMA1 | 12 | 10 | 8 | 10.5 | |
| All enabled | | 166 | 138 | 106 | 130 | |
| $I_{DD\ (RTC)}$ | | 0.47 | | | | µA |
| $I_{DD\ (LCD)}$ | | 3.1 | | | | |
| $I_{DD\ (ADC)}$(3) | | 1450 | | | | |
| $I_{DD\ (DAC)}$(4) | | 340 | | | | |
| $I_{DD\ (COMP1)}$ | | 0.16 | | | | |
| $I_{DD\ (COMP2)}$ | Slow mode | 2 | | | | |
| | Fast mode | 5 | | | | |
| $I_{DD\ (PVD\ /\ BOR)}$(5) | | 2.6 | | | | |
| $I_{DD\ (IWDG)}$ | | 0.25 | | | | |

1. Data based on differential $I_{DD}$ measurement between all peripherals OFF an one peripheral with clock enabled, in the following conditions: $f_{HCLK}$ = 32 MHz (Range 1), $f_{HCLK}$ = 16 MHz (Range 2), $f_{HCLK}$ = 4 MHz (Range 3), $f_{HCLK}$ = 64kHz (Low power run/sleep), $f_{APB1} = f_{HCLK}$, $f_{APB2} = f_{HCLK}$, default prescaler value for each peripheral. The CPU is in Sleep mode in both cases. No I/O pins toggling.
2. HSI oscillator is OFF for this measure.
3. Data based on a differential $I_{DD}$ measurement between ADC in reset configuration and continuous ADC conversion (HSI consumption not included).
4. Data based on a differential $I_{DD}$ measurement between DAC in reset configuration and continuous DAC conversion of $V_{DD}$/2. DAC is in buffered mode, output is left floating.
5. Including supply current of internal reference voltage.

**Figure 17. HSE oscillator circuit diagram**




1. $R_{EXT}$ value depends on the crystal characteristics.

## Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 29*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

**Table 29. LSE oscillator characteristics ($f_{LSE}$ = 32.768 kHz)(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LSE}$ | Low speed external oscillator frequency | - | - | 32.768 | - | kHz |
| $R_F$ | Feedback resistor | - | - | 1.2 | - | MΩ |
| $C^{(2)}$ | Recommended load capacitance versus equivalent serial resistance of the crystal ($R_S$)(3) | $R_S$ = 30 kΩ | - | 8 | - | pF |
| $I_{LSE}$ | LSE driving current | $V_{DD}$ = 3.3 V, $V_{IN}$ = $V_{SS}$ | - | - | 1.1 | µA |
| $I_{DD\ (LSE)}$ | LSE oscillator current consumption | $V_{DD}$ = 1.8 V | - | 450 | - | nA |
| | | $V_{DD}$ = 3.0 V | - | 600 | - | |
| | | $V_{DD}$ = 3.6V | - | 750 | - | |
| $g_m$ | Oscillator transconductance | - | 3 | - | - | µA/V |
| $t_{SU(LSE)}$(4) | Startup time | $V_{DD}$ is stabilized | - | 1 | - | s |

1. Guaranteed by characterization results.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
3. The oscillator selection can be optimized in terms of supply current using an high quality resonator with small $R_S$ value for example MSIV-TIN32.768kHz. Refer to crystal manufacturer for more details.

## 6.3.13 I/O port characteristics

### General input/output characteristics

Unless otherwise specified, the parameters given in *Table 42* are derived from tests performed under conditions summarized in *Table 13*. All I/Os are CMOS and TTL compliant.

**Table 42. I/O static characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IL}$ | Input low level voltage | - | - | - | - | $0.3V_{DD}$ (1) | V |
| $V_{IH}$ | Input high level voltage | Standard I/O | | $0.7\ V_{DD}$ | - | - | |
| | | FT I/O | | | - | - | |
| $V_{hys}$ | I/O Schmitt trigger voltage hysteresis(2) | Standard I/O | | - | 10% $V_{DD}$ (3) | - | |
| | | FT I/O | | - | 5% $V_{DD}$ (4) | - | |
| $I_{lkg}$ | Input leakage current (5) | $V_{SS} \le V_{IN} \le V_{DD}$ I/Os with LCD | | - | - | ±50 | nA |
| | | $V_{SS} \le V_{IN} \le V_{DD}$ I/Os with analog switches | | - | - | ±50 | |
| | | $V_{SS} \le V_{IN} \le V_{DD}$ I/Os with analog switches and LCD | | - | - | ±50 | |
| | | $V_{SS} \le V_{IN} \le V_{DD}$ I/Os with USB | | - | - | TBD | |
| | | FT I/O $V_{DD} \le V_{IN} \le 5V$ | | - | - | TBD | |
| | | $V_{SS} \le V_{IN} \le V_{DD}$ Standard I/Os | | - | - | ±50 | |
| $R_{PU}$ | Weak pull-up equivalent resistor(6)(1) | $V_{IN} = V_{SS}$ | | 30 | 45 | 60 | kΩ |
| $R_{PD}$ | Weak pull-down equivalent resistor(6) | $V_{IN} = V_{DD}$ | | 30 | 45 | 60 | kΩ |
| $C_{IO}$ | I/O pin capacitance | - | - | - | 5 | - | pF |

1. Tested in production
2. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization.
3. With a minimum of 200 mV. Based on characterization results.
4. With a minimum of 100 mV. Based on characterization results.
5. The max. value may be exceeded if negative current is injected on adjacent pins.
6. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This MOS/NMOS contribution to the series resistance is minimum (~10% order).

### Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with the non-standard $V_{OL}/V_{OH}$ specifications given in *Table 43*.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating $I_{VDD\Sigma}$ (see *Table 11*).
- The sum of the currents sunk by all the I/Os on $V_{SS}$ plus the maximum Run consumption of the MCU sunk on $V_{SS}$ cannot exceed the absolute maximum rating $I_{VSS\Sigma}$ (see *Table 11*).

### Output voltage levels

Unless otherwise specified, the parameters given in *Table 43* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 13*. All I/Os are CMOS and TTL compliant.

**Table 43. Output voltage characteristics**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OL}$ (1)(2) | Output low level voltage for an I/O pin | $I_{IO}$ = 8 mA<br>2.7 V < $V_{DD}$ < 3.6 V | - | 0.4 | V |
| $V_{OH}$ (3)(2) | Output high level voltage for an I/O pin | | 2.4 | - | |
| $V_{OL}$ (1)(4) | Output low level voltage for an I/O pin | $I_{IO}$ = 4 mA<br>1.65 V < $V_{DD}$ < 2.7 V | - | 0.45 | |
| $V_{OH}$ (3)(4) | Output high level voltage for an I/O pin | | $V_{DD}$-0.45 | - | |
| $V_{OL}$ (1)(4) | Output low level voltage for an I/O pin | $I_{IO}$ = 20 mA<br>2.7 V < $V_{DD}$ < 3.6 V | - | 1.3 | |
| $V_{OH}$ (3)(4) | Output high level voltage for an I/O pin | | $V_{DD}$-1.3 | - | |

1. The $I_{IO}$ current sunk by the device must always respect the absolute maximum rating specified in *Table 11* and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VSS}$.
2. Tested in production.
3. The $I_{IO}$ current sourced by the device must always respect the absolute maximum rating specified in *Table 11* and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VDD}$.
4. Guaranteed by characterization results.

### Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 19* and *Table 44*, respectively.

Unless otherwise specified, the parameters given in *Table 44* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 13*.

**Table 44. I/O AC characteristics(1)**

| OSPEEDRx [1:0] bit value(1) | Symbol | Parameter | Conditions | Min | Max(2) | Unit |
|---|---|---|---|---|---|---|
| 00 | $f_{max(IO)out}$ | Maximum frequency(3) | $C_L$ = 50 pF, $V_{DD}$ = 2.7 V to 3.6 V | - | 400 | kHz |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 1.65 V to 2.7 V | - | 400 | |
| | $t_{f(IO)out}$ $t_{r(IO)out}$ | Output rise and fall time | $C_L$ = 50 pF, $V_{DD}$ = 2.7 V to 3.6 V | - | 625 | ns |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 1.65 V to 2.7 V | - | 625 | |
| 01 | $f_{max(IO)out}$ | Maximum frequency(3) | $C_L$ = 50 pF, $V_{DD}$ = 2.7 V to 3.6 V | - | 2 | MHz |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 1.65 V to 2.7 V | - | 1 | |
| | $t_{f(IO)out}$ $t_{r(IO)out}$ | Output rise and fall time | $C_L$ = 50 pF, $V_{DD}$ = 2.7 V to 3.6 V | - | 125 | ns |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 1.65 V to 2.7 V | - | 250 | |
| 10 | $F_{max(IO)out}$ | Maximum frequency(3) | $C_L$ = 50 pF, $V_{DD}$ = 2.7 V to 3.6 V | - | 10 | MHz |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 1.65 V to 2.7 V | - | 2 | |
| | $t_{f(IO)out}$ $t_{r(IO)out}$ | Output rise and fall time | $C_L$ = 50 pF, $V_{DD}$ = 2.7 V to 3.6 V | - | 25 | ns |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 1.65 V to 2.7 V | - | 125 | |
| 11 | $F_{max(IO)out}$ | Maximum frequency(3) | $C_L$ = 50 pF, $V_{DD}$ = 2.7 V to 3.6 V | - | 50 | MHz |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 1.65 V to 2.7 V | - | 8 | |
| | $t_{f(IO)out}$ $t_{r(IO)out}$ | Output rise and fall time | $C_L$ = 30 pF, $V_{DD}$ = 2.7 V to 3.6 V | - | 5 | ns |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 1.65 V to 2.7 V | - | 30 | |
| - | $t_{EXTIpw}$ | Pulse width of external signals detected by the EXTI controller | - | 8 | - | |

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the STM32L151x6/8/B and STM32L152x6/8/B reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design.
3. The maximum frequency is defined in *Figure 19*.

**Figure 22. SPI timing diagram - slave mode and CPHA = 0**

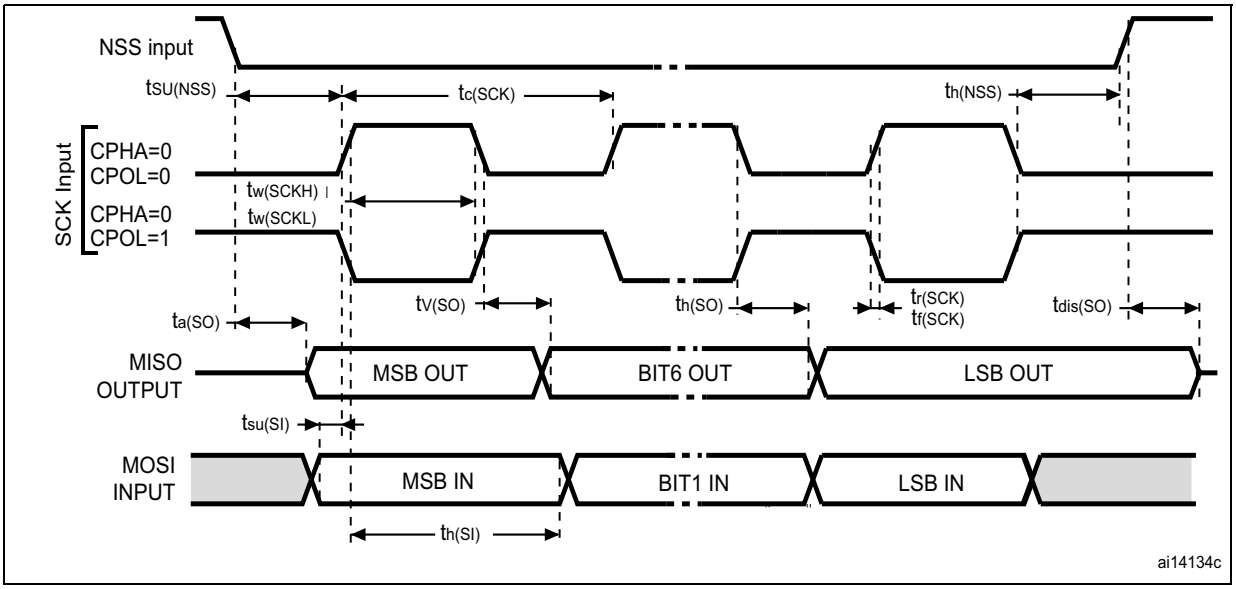
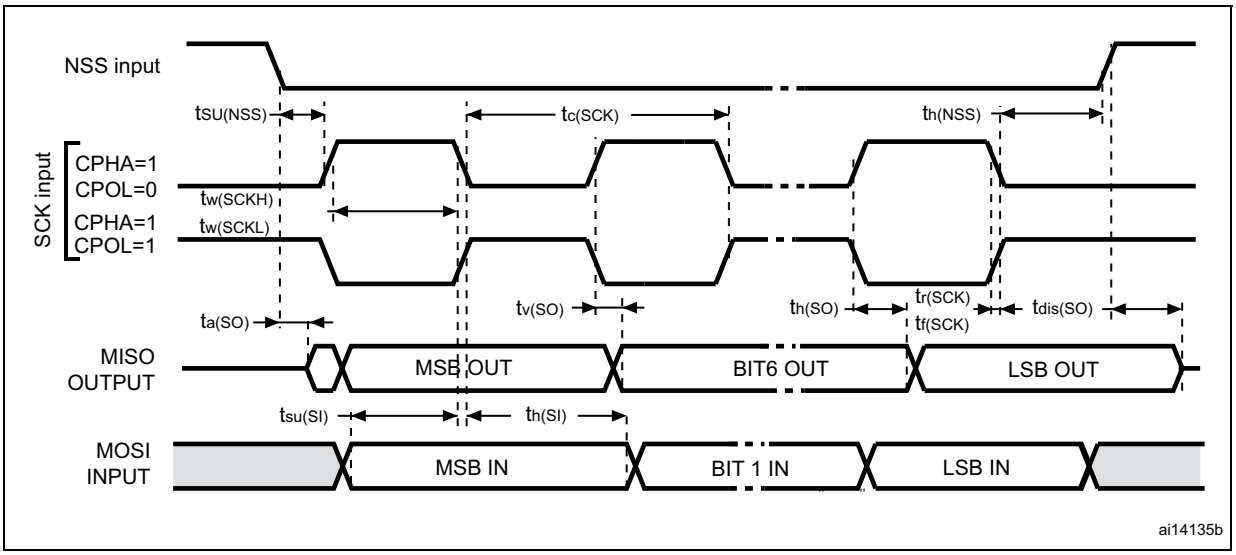



**Figure 23. SPI timing diagram - slave mode and CPHA = 1(1)**




1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

**Table 55. ADC accuracy(1)(2)**

| Symbol | Parameter | Test conditions | Min(3) | Typ | Max(3) | Unit |
|---|---|---|---|---|---|---|
| ET | Total unadjusted error | $2.4\ V \le V_{DDA} \le 3.6\ V$<br>$2.4\ V \le V_{REF+} \le 3.6\ V$<br>$f_{ADC} = 8\ MHz$, $R_{AIN} = 50\ \Omega$<br>$T_A = -40$ to $105\ °C$ | - | 2 | 4 | LSB |
| EO | Offset error | | - | 1 | 2 | |
| EG | Gain error | | - | 1.5 | 3.5 | |
| ED | Differential linearity error | | - | 1 | 2 | |
| EL | Integral linearity error | | - | 1.7 | 3 | |
| ENOB | Effective number of bits | $2.4\ V \le V_{DDA} \le 3.6\ V$<br>$V_{DDA} = V_{REF+}$<br>$f_{ADC} = 16\ MHz$, $R_{AIN} = 50\ \Omega$<br>$T_A = -40$ to $105\ °C$<br>$1\ kHz \le F_{input} \le 100\ kHz$ | 9.2 | 10 | - | bits |
| SINAD | Signal-to-noise and distortion ratio | | 57.5 | 62 | - | dB |
| SNR | Signal-to-noise ratio | | 57.5 | 62 | - | |
| THD | Total harmonic distortion | | -74 | -75 | - | |
| ET | Total unadjusted error | $2.4\ V \le V_{DDA} \le 3.6\ V$<br>$1.8\ V \le V_{REF+} \le 2.4\ V$<br>$f_{ADC} = 4\ MHz$, $R_{AIN} = 50\ \Omega$<br>$T_A = -40$ to $105\ °C$ | - | 4 | 6.5 | LSB |
| EO | Offset error | | - | 2 | 4 | |
| EG | Gain error | | - | 4 | 6 | |
| ED | Differential linearity error | | - | 1 | 2 | |
| EL | Integral linearity error | | - | 1.5 | 3 | |
| ET | Total unadjusted error | $1.8\ V \le V_{DDA} \le 2.4\ V$<br>$1.8\ V \le V_{REF+} \le 2.4\ V$<br>$f_{ADC} = 4\ MHz$, $R_{AIN} = 50\ \Omega$<br>$T_A = -40$ to $105\ °C$ | - | 2 | 3 | LSB |
| EO | Offset error | | - | 1 | 1.5 | |
| EG | Gain error | | - | 1.5 | 2 | |
| ED | Differential linearity error | | - | 1 | 2 | |
| EL | Integral linearity error | | - | 1 | 1.5 | |

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative injection current: Injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.12* does not affect the ADC accuracy.
3. Guaranteed by characterization results.

**Table 57. DAC characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| dOffset/dT(1) | Offset error temperature coefficient (code 0x800) | $V_{DDA}$ = 3.3V, $T_A$ = 0 to 50 °C DAC output buffer OFF | -20 | -10 | 0 | µV/°C |
| | | $V_{DDA}$ = 3.3V, $T_A$ = 0 to 50 °C DAC output buffer ON | 0 | 20 | 50 | |
| Gain(1) | Gain error(6) | $C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON | - | +0.1 / -0.2% | +0.2 / -0.5% | % |
| | | No $R_{LOAD}$, $C_L \leq 50$ pF DAC output buffer OFF | - | +0 / -0.2% | +0 / -0.4% | |
| dGain/dT(1) | Gain error temperature coefficient | $V_{DDA}$ = 3.3V, $T_A$ = 0 to 50 °C DAC output buffer OFF | -10 | -2 | 0 | µV/°C |
| | | $V_{DDA}$ = 3.3V, $T_A$ = 0 to 50 °C DAC output buffer ON | -40 | -8 | 0 | |
| TUE(1) | Total unadjusted error | $C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON | - | 12 | 30 | LSB |
| | | No $R_{LOAD}$, $C_L \leq 50$ pF DAC output buffer OFF | - | 8 | 12 | |
| $t_{SETTLING}$ | Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes till DAC_OUT reaches final value ±1LSB | $C_L \leq 50$ pF, $R_L \geq 5$ kΩ | - | 7 | 12 | µs |
| Update rate | Max frequency for a correct DAC_OUT change (95% of final value) with 1 LSB variation in the input code | $C_L \leq 50$ pF, $R_L \geq 5$ kΩ | - | - | 1 | Msps |
| $t_{WAKEUP}$ | Wakeup time from off state (setting the ENx bit in the DAC Control register)(7) | $C_L \leq 50$ pF, $R_L \geq 5$ kΩ | - | 9 | 15 | µs |
| PSRR+ | $V_{DDA}$ supply rejection ratio (static DC measurement) | $C_L \leq 50$ pF, $R_L \geq 5$ kΩ | - | -60 | -35 | dB |

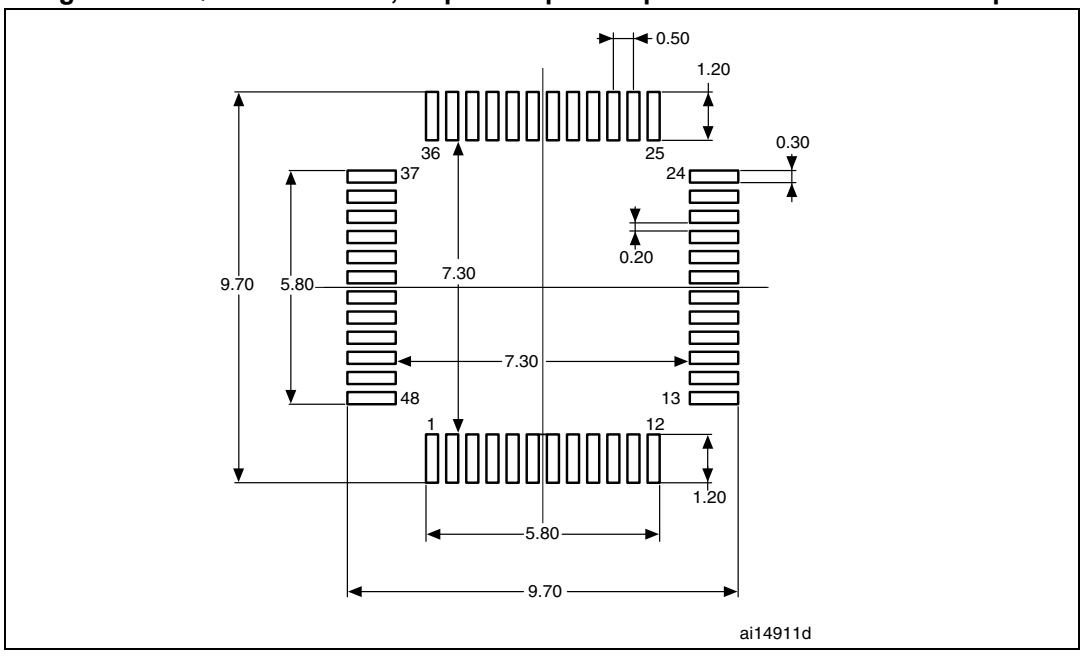
1. Guaranteed by characterization results.
2. Difference between two consecutive codes - 1 LSB.
3. Difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095.
4. Difference between the value measured at Code (0x800) and the ideal value = V/2.
5. Difference between the value measured at Code (0x001) and the ideal value.
6. Difference between ideal slope of the transfer function and measured slope computed from code 0x000 and 0xFFF when buffer is OFF, and from code giving 0.2 V and ($V_{DDA}$ – 0.2) V when buffer is ON.
7. In buffered mode, the output can overshoot above the final value for low input code (starting from min value).

**Table 65. LQFP48 7 x 7 mm, 48-pin low-profile quad flat package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| D1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| D3 | - | 5.500 | - | - | 0.2165 | - |
| E | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| E1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| E3 | - | 5.500 | - | - | 0.2165 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| k | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 39. LQFP48 7 x 7 mm, 48-pin low-profile quad flat recommended footprint**

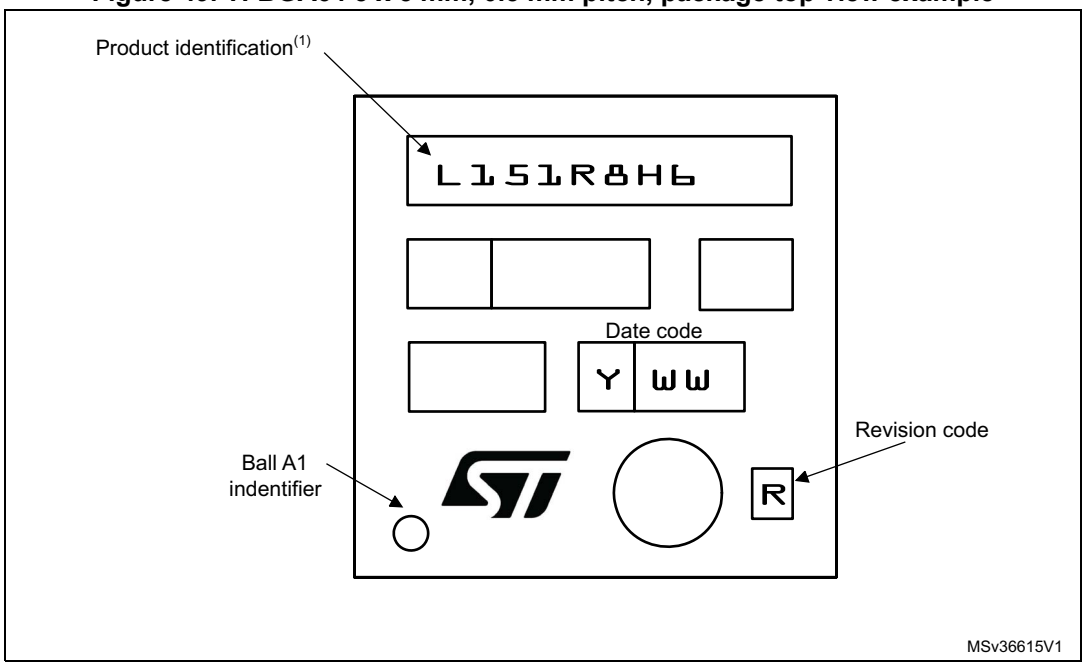



1. Dimensions are in millimeters.

### TFBGA64 device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

**Figure 49. TFBGA64 5 x 5 mm, 0.5 mm pitch, package top view example**




1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

# 8 Ordering information

**Table 72. Ordering information scheme**

Example: STM32 L 151 C 8 T 6 T TR

**Device family**

STM32 = ARM-based 32-bit microcontroller

**Product type**

L = Low power

Device subfamily

151: Devices without LCD

152: Devices with LCD

Pin count

C = 48 pins

R = 64 pins

V = 100 pins

**Flash memory size**

6 = 32 Kbytes of Flash memory

8 = 64 Kbytes of Flash memory

B = 128 Kbytes of Flash memory

**Package**

H = BGA

T = LQFP

U = UFQFPN

**Temperature range**

6 = Industrial temperature range, –40 to 85 °C

Options

No character = $V_{DD}$ range: 1.8 to 3.6 V and BOR enabled

T = $V_{DD}$ range: 1.65 to 3.6 V and BOR disabled

Packing

TR = tape and reel

No character = tray or tube

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.