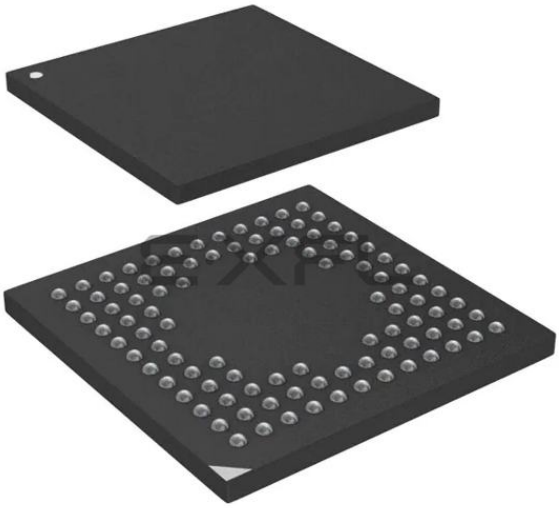

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Cap Sense, DMA, I²S, POR, PWM, WDT
Number of I/O	83
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-UFBGA
Supplier Device Package	100-UFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l151vbh6d

List of figures

2.1 Device overview

Table 2. Ultra-low-power STM32L151x6/8/B and STM32L152x6/8/B device features and peripheral counts

Peripheral		STM32L15xCx			STM32L15xRx			STM32L15xVx	
Flash (Kbytes)		32	64	128	32	64	128	64	128
Data EEPROM (Kbytes)		4							
RAM (Kbytes)		10	10	16	10	10	16	10	16
Timers	General-purpose	6							
	Basic	2							
Communication interfaces	SPI	2							
	I^2C	2							
	USART	3							
	USB	1							
GPIOs		37			51			83	
12-bit synchronized ADC Number of channels		1 14 channels			1 20 channels			1 24 channels	
12-bit DAC Number of channels		2 2							
LCD (STM32L152xx Only) COM x SEG		4x18			4x32 8x28			4x44 8x40	
Comparator		2							
Capacitive sensing channels		13			20				
Max. CPU frequency		32 MHz							
Operating voltage		1.8 V to 3.6 V (down to 1.65 V at power-down) with BOR option 1.65 V to 3.6 V without BOR option							
Operating temperatures		Ambient temperatures: –40 to +85 °C Junction temperature: –40 to + 105 °C							
Packages		LQFP48, UFQFPN48			LQFP64, BGA64			LQFP100, BGA100	

3.1 Low power modes

The ultra-low-power STM32L151x6/8/B and STM32L152x6/8/B devices support dynamic voltage scaling to optimize its power consumption in run mode. The voltage from the internal low-drop regulator that supplies the logic can be adjusted according to the system's maximum operating frequency and the external voltage supply:

- In Range 1 (V_{DD} range limited to 1.71-3.6 V), the CPU runs at up to 32 MHz (refer to *Table 17* for consumption).
- In Range 2 (full V_{DD} range), the CPU runs at up to 16 MHz (refer to *Table 17* for consumption)
- In Range 3 (full V_{DD} range), the CPU runs at up to 4 MHz (generated only with the multispeed internal RC oscillator clock source). Refer to *Table 17* for consumption.

Seven low power modes are provided to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

  Sleep mode power consumption: refer to *Table 19*.

- **Low power run** mode

  This mode is achieved with the multispeed internal (MSI) RC oscillator set to the minimum clock (65 kHz), execution from SRAM or Flash memory, and internal regulator in low power mode to minimize the regulator's operating current. In the Low power run mode, the clock frequency and the number of enabled peripherals are both limited.

  Low power run mode consumption: refer to *Table 20: Current consumption in Low power run mode*.

- **Low power sleep** mode

  This mode is achieved by entering the Sleep mode with the internal voltage regulator in Low power mode to minimize the regulator's operating current. In the Low power sleep mode, both the clock frequency and the number of enabled peripherals are limited; a typical example would be to have a timer running at 32 kHz.
  When wakeup is triggered by an event or an interrupt, the system reverts to the run mode with the regulator on.

  Low power sleep mode consumption: refer to *Table 21: Current consumption in Low power sleep mode*.

- **Stop** mode with RTC

  Stop mode achieves the lowest power consumption while retaining the RAM and register contents and real time clock. All clocks in the V_{CORE} domain are stopped, the PLL, MSI RC, HSI RC and HSE crystal oscillators are disabled. The LSE or LSI is still running. The voltage regulator is in the low power mode.

  The device can be woken up from Stop mode by any of the EXTI line, in 8 µs. The EXTI line source can be one of the 16 external lines. It can be the PVD output, the Comparator 1 event or Comparator 2 event (if internal reference voltage is on), it can be the RTC alarm(s), the USB wakeup, the RTC tamper events, the RTC timestamp event or the RTC wakeup.

- **Stop** mode without RTC

  Stop mode achieves the lowest power consumption while retaining the RAM and register contents. All clocks are stopped, the PLL, MSI RC, HSI and LSI RC, LSE and

Nested vectored interrupt controller (NVIC)

The ultra-low-power STM32L151x6/8/B and STM32L152x6/8/B devices embed a nested vectored interrupt controller able to handle up to 45 maskable interrupt channels (not including the 16 interrupt lines of Cortex®-M3) and 16 priority levels.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving*, higher-priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.3 Reset and supply management

3.3.1 Power supply schemes

- V_{DD} = 1.65 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 1.65 to 3.6 V: external analog power supplies for ADC, reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 1.8 V when the ADC is used). V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.

3.3.2 Power supply supervisor

The device has an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR) that can be coupled with a brownout reset (BOR) circuitry.

The device exists in two versions:

- The version with BOR activated at power-on operates between 1.8 V and 3.6 V.
- The other version without BOR operates between 1.65 V and 3.6 V.

After the V_{DD} threshold is reached (1.65 V or 1.8 V depending on the BOR which is active or not at power-on), the option byte loading process starts, either to confirm or modify default thresholds, or to disable the BOR permanently: in this case, the V_{DD} min value becomes 1.65 V (whatever the version, BOR active or not, at power-on).

When BOR is active at power-on, it ensures proper operation starting from 1.8 V whatever the power ramp-up phase before it reaches 1.8 V. When BOR is not active at power-up, the power ramp-up should guarantee that 1.65 V is reached on V_{DD} at least 1 ms after it exits the POR area.

Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Stop mode, it is possible to automatically switch off the internal reference voltage (V_{REFINT}) in Stop mode. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for any external reset circuit.

Note: The start-up time at power-on is typically 3.3 ms when BOR is active at power-up, the start-up time at power-on can be decreased down to 1 ms typically for devices with BOR inactive at power-up.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.3.3 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in Run mode (nominal regulation)
- LPR is used in the Low-power run, Low-power sleep and Stop modes
- Power down is used in Standby mode. The regulator output is high impedance, the kernel circuitry is powered down, inducing zero consumption but the contents of the registers and RAM are lost are lost except for the standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE crystal 32K osc, RCC_CSR).

3.3.4 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from Flash memory
- Boot from System Memory
- Boot from embedded RAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART1 or USART2. See STM32™ microcontroller system memory boot mode AN2606 for details.

3.17 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.18 Development support

Serial wire JTAG debug port (SWJ-DP)

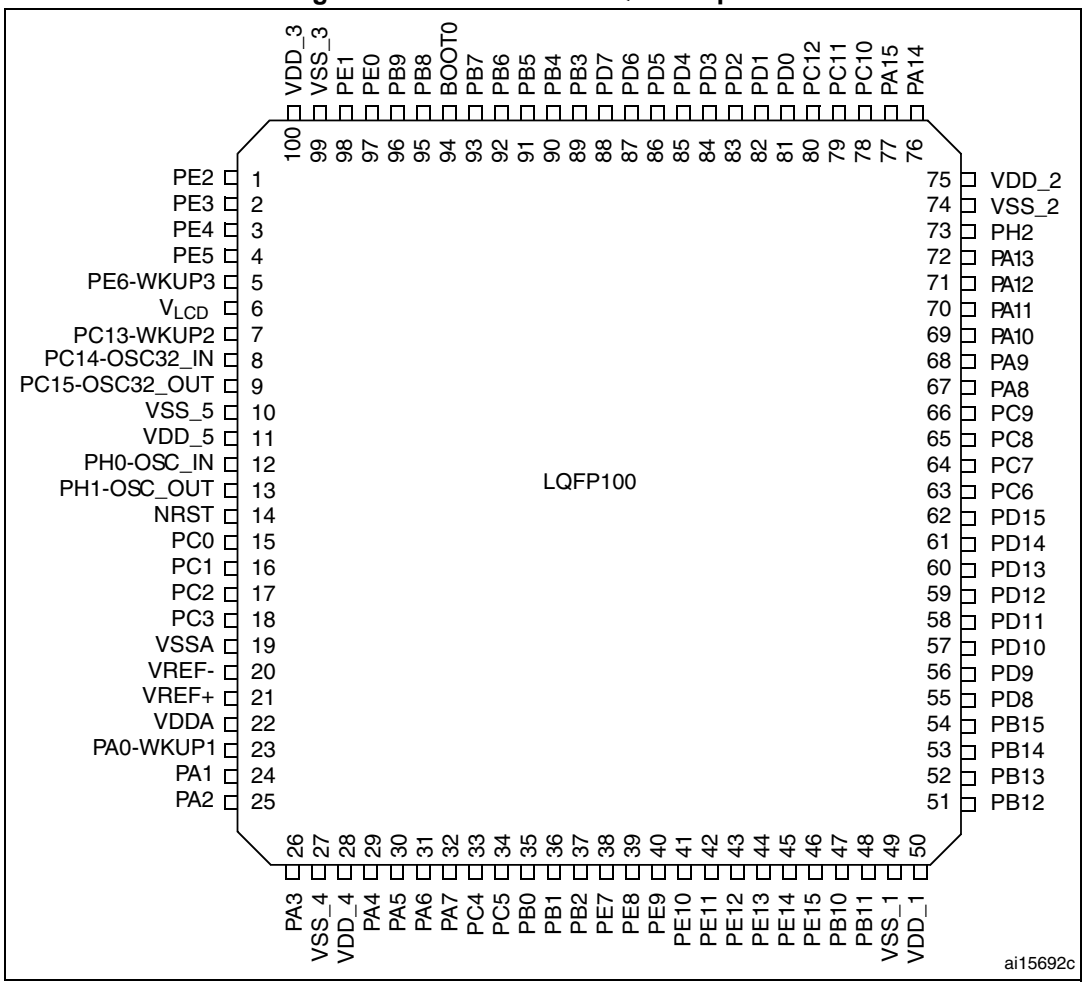
The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG JTMS and JTCK pins are shared with SWDAT and SWCLK, respectively, and a specific sequence on the JTMS pin is used to switch between JTAG-DP and SW-DP.

The JTAG port can be permanently disabled with a JTAG fuse.

Embedded Trace Macrocell™

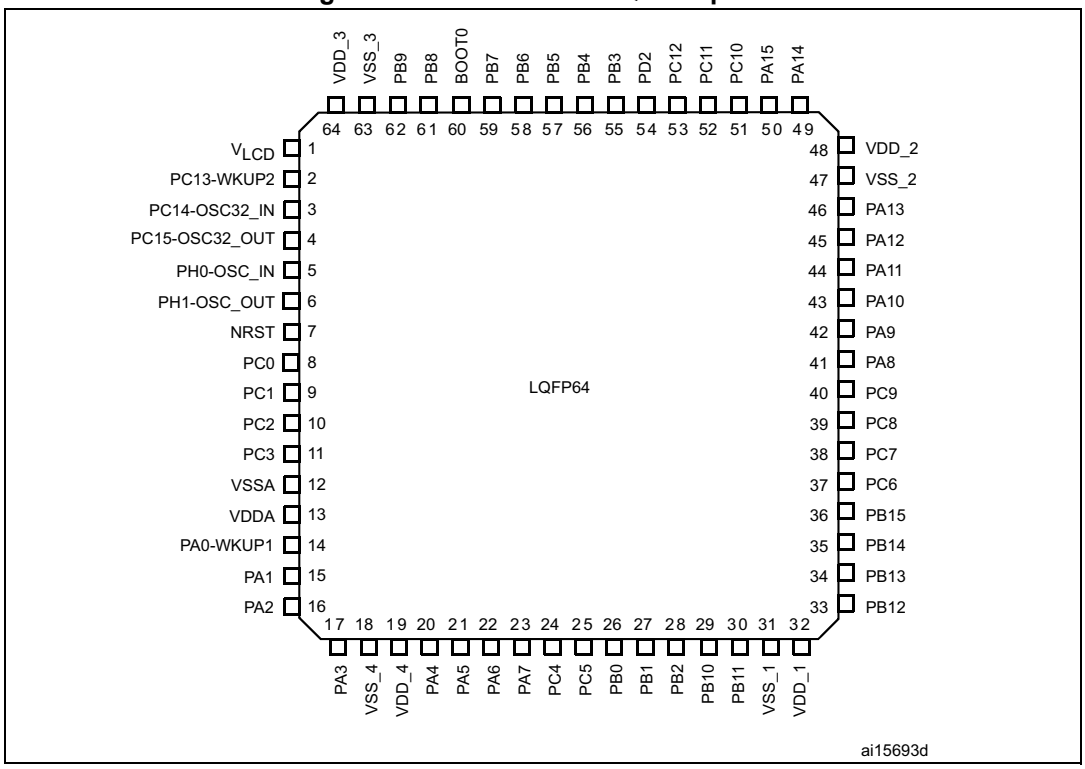
The ARM Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32L151x6/8/B and STM32L152x6/8/B device through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer running debugger software. TPA hardware is commercially available from common development tool vendors. It operates with third party debugger software tools.

Figure 4. STM32L15xVx LQFP100 pinout



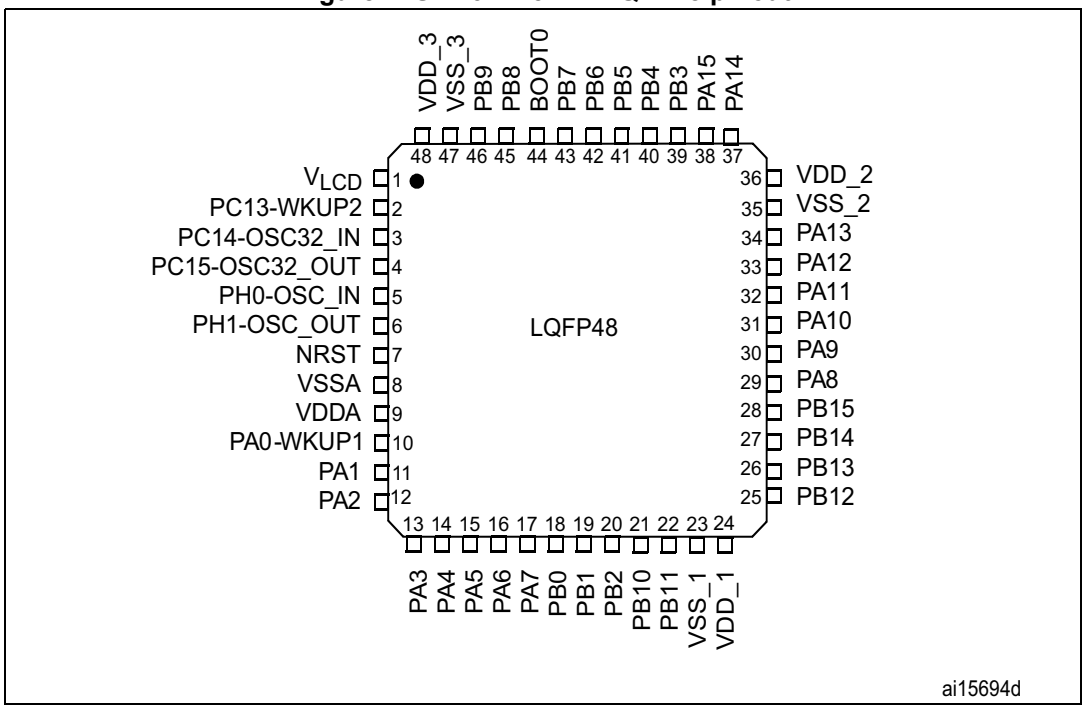
1. This figure shows the package top view.

Figure 6. STM32L15xRx LQFP64 pinout



1. This figure shows the package top view.

Figure 7. STM32L15xCx LQFP48 pinout



1. This figure shows the package top view.

Table 7. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		TC	Standard 3.3 V I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 8. STM32L151x6/8/B and STM32L152x6/8/B pin definitions (continued)

Pins					Pin name	Pin type[1]	I/O structure	Main function[2] (after reset)	Pins functions	
LQFP100	LQFP64	TFBGA64	UFBGA100	LQFP48 or UFQFPN48					Alternate functions	Additional functions
19	12	F1	J1	8	V_{SSA}	S	-	V_{SSA}	-	-
20	-	-	K1	-	V_{REF-}	S	-	V_{REF-}	-	-
21	-	G1 (6)	L1	-	V_{REF+}	S	-	V_{REF+}	-	-
22	13	H1	M1	9	V_{DDA}	S	-	V_{DDA}	-	-
23	14	G2	L2	10	PA0-WKUP1	I/O	FT	PA0	USART2_CTS/ TIM2_CH1_ETR	WKUP1/ ADC_IN0/ COMP1_INP
24	15	H2	M2	11	PA1	I/O	FT	PA1	USART2_RTS/ TIM2_CH2/LCD_SEG0	ADC_IN1/ COMP1_INP
25	16	F3	K3	12	PA2	I/O	FT	PA2	USART2_TX/TIM2_CH3/ TIM9_CH1/LCD_SEG1	ADC_IN2/ COMP1_INP
26	17	G3	L3	13	PA3	I/O	TC	PA3	USART2_RX/TIM2_CH4/ TIM9_CH2/LCD_SEG2	ADC_IN3/ COMP1_INP
27	18	C2	E3	-	V_{SS_4}	S	-	V_{SS_4}	-	-
28	19	D2	H3	-	V_{DD_4}	S	-	V_{DD_4}	-	-
29	20	H3	M3	14	PA4	I/O	TC	PA4	SPI1_NSS/USART2_CK	ADC_IN4/ DAC_OUT1/ COMP1_INP
30	21	F4	K4	15	PA5	I/O	TC	PA5	SPI1_SCK/ TIM2_CH1_ETR	ADC_IN5/ DAC_OUT2/ COMP1_INP
31	22	G4	L4	16	PA6	I/O	FT	PA6	SPI1_MISO/TIM3_CH1/ LCD_SEG3/TIM10_CH1	ADC_IN6 /COMP1_INP
32	23	H4	M4	17	PA7	I/O	FT	PA7	SPI1_MOSI//TIM3_CH2/ LCD_SEG4/TIM11_CH1	ADC_IN7/ COMP1_INP
33	24	H5	K5	-	PC4	I/O	FT	PC4	LCD_SEG22	ADC_IN14/ COMP1_INP
34	25	H6	L5	-	PC5	I/O	FT	PC5	LCD_SEG23	ADC_IN15/ COMP1_INP

Table 17. Current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max(1)			Unit
						55 °C	85 °C	105 °C	
I_{DD} (Run from Flash)	Supply current in Run mode, code executed from Flash	$f_{HSE} = f_{HCLK}$ up to 16 MHz, included $f_{HSE} = f_{HCLK}/2$ above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	1 MHz	270	400	400	400	µA
				2 MHz	470	600	600	600	
				4 MHz	890	1025	1025	1025	
			Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	4 MHz	1	1.3	1.3	1.3	mA
				8 MHz	2	2.5	2.5	2.5	
				16 MHz	3.9	5	5	5	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	8 MHz	2.16	3	3	3	
				16 MHz	4.8	5.5	5.5	5.5	
				32 MHz	9.6	11	11	11	
		HSI clock source (16 MHz)	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	16 MHz	4	5	5	5	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	32 MHz	9.4	11	11	11	
		MSI clock, 65 kHz	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	65 kHz	0.05	0.085	0.09	0.1	
		MSI clock, 524 kHz		524 kHz	0.15	0.185	0.19	0.2	
		MSI clock, 4.2 MHz		4.2 MHz	0.9	1	1	1	

1. Guaranteed by characterization results, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 22. Typical and maximum current consumptions in Stop mode (continued)

Symbol	Parameter	Conditions		Typ (1)	Max (1)(2)	Unit
$I_{DD\ (Stop)}$	Supply current in Stop mode (RTC disabled)	Regulator in LP mode, HSI and HSE OFF, independent watchdog and LSI enabled	T_A = -40°C to 25°C	1.1	2.2	µA
		Regulator in LP mode, LSI, HSI and HSE OFF (no independent watchdog)	T_A = -40°C to 25°C	0.5	0.9	
			T_A = 55°C	1.9	5	
			T_A= 85°C	3.7	8	
			T_A = 105°C	8.9	20(6)	
$I_{DD\ (WU\ from\ Stop)}$	RMS (root mean square) supply current during wakeup time when exiting from Stop mode	MSI = 4.2 MHz	V_{DD} = 3.0 V T_A = -40°C to 25°C	2	-	mA
		MSI = 1.05 MHz		1.45	-	
		MSI = 65 kHz(7)		1.45	-	

1. The typical values are given for V_{DD} = 3.0 V and max values are given for V_{DD} = 3.6 V, unless otherwise specified.
2. Guaranteed by characterization results, unless otherwise specified
3. LCD enabled with external VLCD, static duty, division ratio = 256, all pixels active, no LCD connected
4. LCD enabled with external VLCD, 1/8 duty, 1/3 bias, division ratio = 64, all pixels active, no LCD connected.
5. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8pF loading capacitors.
6. Tested in production
7. When MSI = 64 kHz, the RMS current is measured over the first 15 µs following the wakeup event. For the remaining time of the wakeup period, the current is similar to the Run mode current.

6.3.13 I/O port characteristics

General input/output characteristics

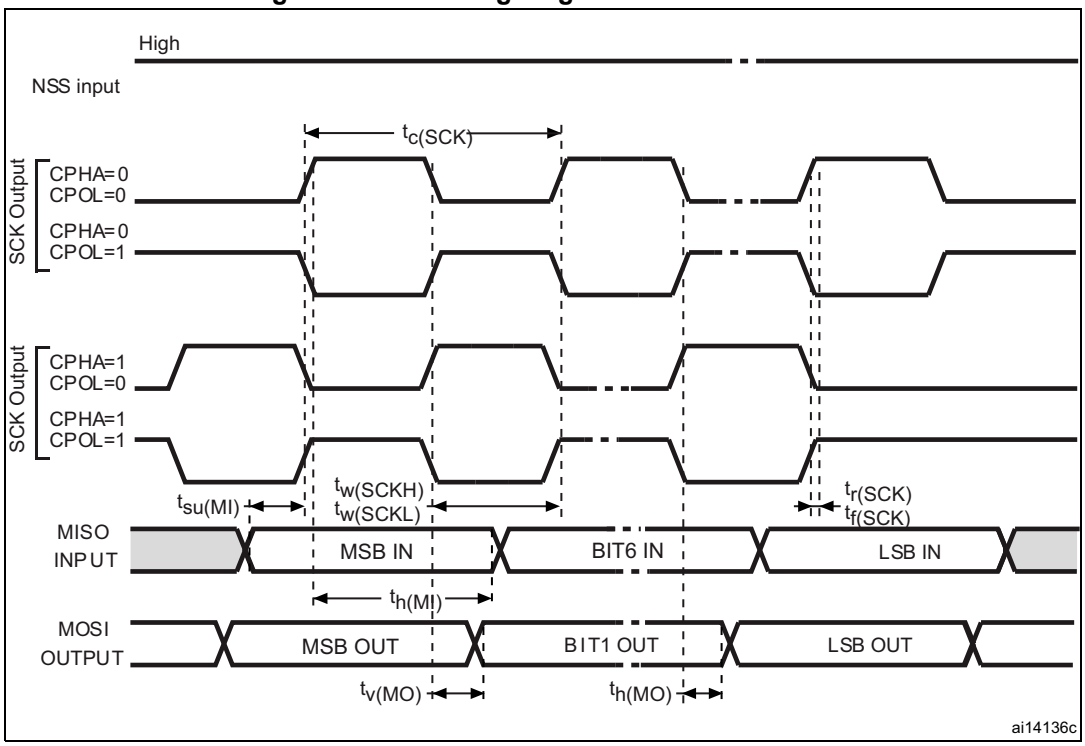
Unless otherwise specified, the parameters given in *Table 42* are derived from tests performed under conditions summarized in *Table 13*. All I/Os are CMOS and TTL compliant.

Table 42. I/O static characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IL}	Input low level voltage	-	-	-	-	$0.3V_{DD}$ (1)	V
V_{IH}	Input high level voltage	Standard I/O		$0.7\ V_{DD}$	-	-	
		FT I/O			-	-	
V_{hys}	I/O Schmitt trigger voltage hysteresis(2)	Standard I/O		-	10% V_{DD} (3)	-	
		FT I/O		-	5% V_{DD} (4)	-	
I_{lkg}	Input leakage current (5)	$V_{SS} \le V_{IN} \le V_{DD}$ I/Os with LCD		-	-	±50	nA
		$V_{SS} \le V_{IN} \le V_{DD}$ I/Os with analog switches		-	-	±50	
		$V_{SS} \le V_{IN} \le V_{DD}$ I/Os with analog switches and LCD		-	-	±50	
		$V_{SS} \le V_{IN} \le V_{DD}$ I/Os with USB		-	-	TBD	
		FT I/O $V_{DD} \le V_{IN} \le 5V$		-	-	TBD	
		$V_{SS} \le V_{IN} \le V_{DD}$ Standard I/Os		-	-	±50	
R_{PU}	Weak pull-up equivalent resistor(6)(1)	$V_{IN} = V_{SS}$		30	45	60	kΩ
R_{PD}	Weak pull-down equivalent resistor(6)	$V_{IN} = V_{DD}$		30	45	60	kΩ
C_{IO}	I/O pin capacitance	-	-	-	5	-	pF

1. Tested in production
2. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization.
3. With a minimum of 200 mV. Based on characterization results.
4. With a minimum of 100 mV. Based on characterization results.
5. The max. value may be exceeded if negative current is injected on adjacent pins.
6. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This MOS/NMOS contribution to the series resistance is minimum (~10% order).

Figure 24. SPI timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

USB characteristics

The USB interface is USB-IF certified (full speed).

Table 50. USB startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB transceiver startup time	1	µs

1. Guaranteed by design.

Figure 28. Maximum dynamic current consumption on V_{REF+} supply pin during ADC conversion

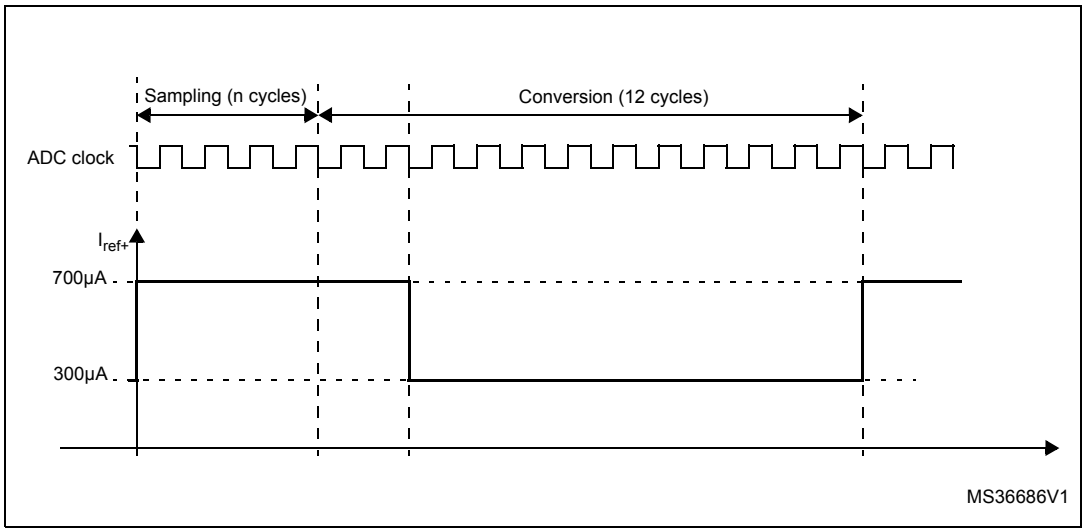


Table 56. Maximum source impedance R_{AIN} max(1)

Ts (µs)	R_{AIN} max (kOhm)				Ts (cycles) f_{ADC}= 16 MHz(2)
	Multiplexed channels		Direct channels		
	2.4 V < V_{DDA}< 3.6 V	1.8 V < V_{DDA} < 2.4 V	2.4 V < V_{DDA}< 3.3 V	1.8 V < V_{DDA} < 2.4 V	
0.25	Not allowed	Not allowed	0.7	Not allowed	4
0.5625	0.8	Not allowed	2.0	1.0	9
1	2.0	0.8	4.0	3.0	16
1.5	3.0	1.8	6.0	4.5	24
3	6.8	4.0	15.0	10.0	48
6	15.0	10.0	30.0	20.0	96
12	32.0	25.0	50.0	40.0	192
24	50.0	50.0	50.0	50.0	384

1. Guaranteed by design.
2. Number of samples calculated for **f_{ADC} = 16 MHz. F**or **f_{ADC} = 8 and 4 MHz the number of sampling cycles can be reduced with respect to the minimum sampling time Ts (us).**

General PCB design guidelines

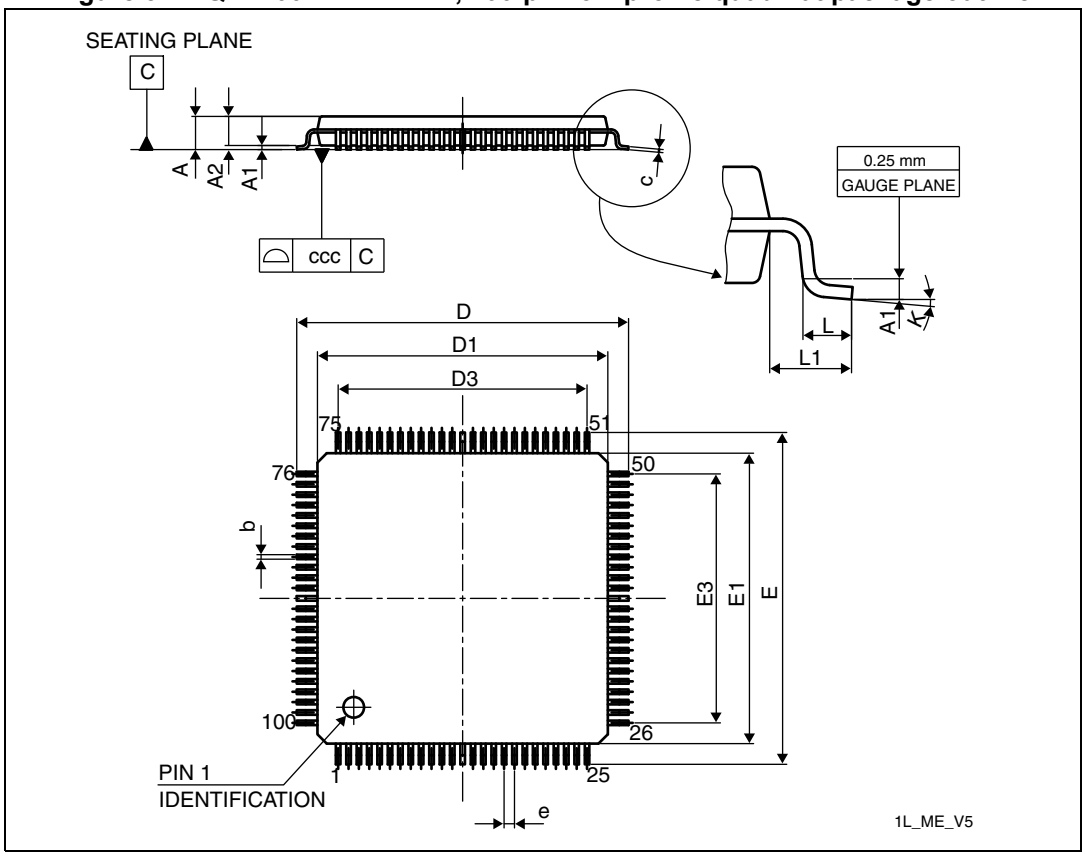
Power supply decoupling should be performed as shown in The 10 nF capacitors should be ceramic (good quality). They should be placed as close as possible to the chip.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.1 LQFP100 14 x 14 mm, 100-pin low-profile quad flat package information

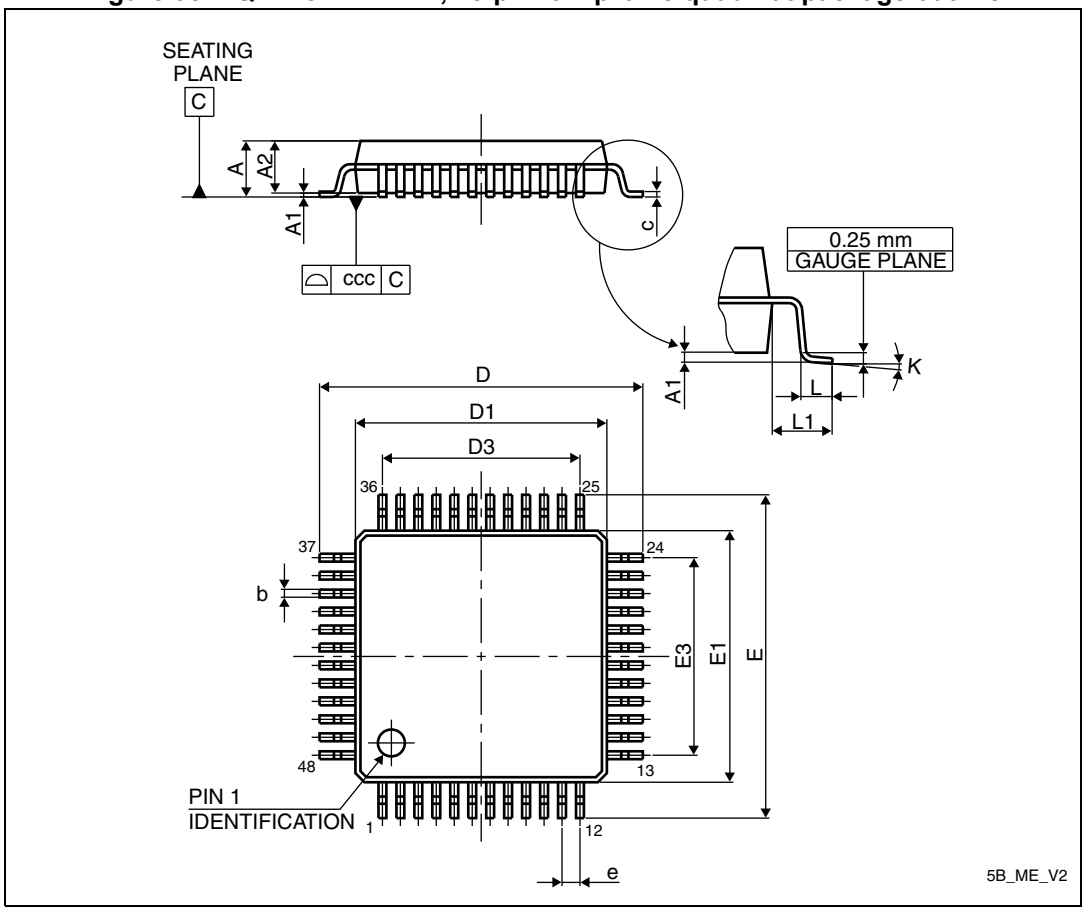
Figure 32. LQFP100 14 x 14 mm, 100-pin low-profile quad flat package outline



1. Drawing is not to scale.

7.3 LQFP48 7 x 7 mm, 48-pin low-profile quad flat package information

Figure 38. LQFP48 7 x 7 mm, 48-pin low-profile quad flat package outline



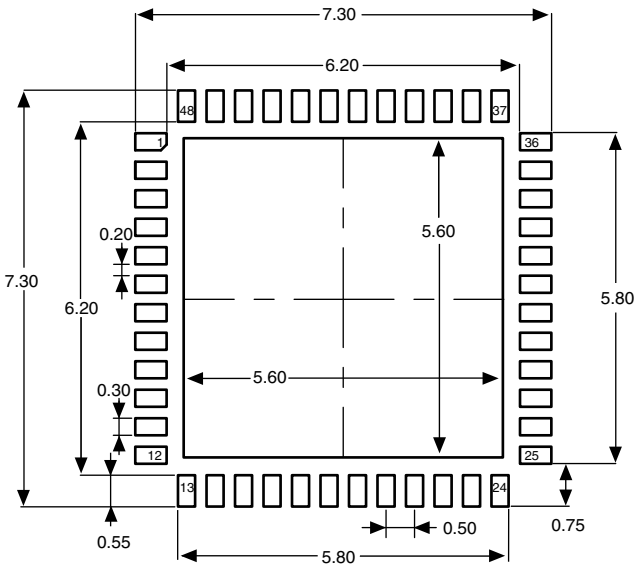
1. Drawing is not to scale.

Table 66. UFQFPN48 7 x 7 mm, 0.5 mm pitch, package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 42. UFQFPN48 7 x 7 mm, 0.5 mm pitch, package recommended footprint



1. Dimensions are in millimeters.

9 Revision history

Table 73. Document revision history

Date	Revision	Changes
02-Jul-2010	1	Initial release.
01-Oct-2010	2	Removed 5 V tolerance (FT) from PA3, PB0 and PC3 in *Table 8: STM32L15xx6/8/B pin definitions* Updated *Table 14: Embedded reset and power control block characteristics* Updated *Table 16: Embedded internal reference voltage* Added *Table 53: ADC clock frequency* Updated *Table 54: ADC characteristics*
16-Dec-2010	3	Modified consumptions on page 1 and in *Section 3.1: Low power modes* LED_SEG8 removed on PB6. Updated *Section 6: Electrical characteristics* VFQFPN48 replaced by UFQFPN48
25-Feb-2011	4	*Section 3.3.2: Power supply supervisor*: updated note. *Table 8: STM32L15xx6/8/B pin definitions:* modified main function (after reset) and alternate function for OSC_IN and OSC_OUT pins; modified footnote 5; added footnote to OSC32_IN and OSC32_OUT pins; C1 and D1 removed on PD0 and PD1 pins (TFBGA64 column). *Section 3.11: DAC (digital-to-analog converter)*: updated bullet list. *Table 10: Voltage characteristics on page 52*: updated footnote 3 regarding $I_{INJ(PIN)}$. *Table 11: Current characteristics on page 52*: updated footnote 4 regarding positive and negative injection. *Table 14: Embedded reset and power control block characteristics on page 54*: updated typ and max values for $T_{RSTTEMPO}$ (V_{DD} rising, BOR enabled). *Table 17: Current consumption in Run mode, code with data processing running from Flash on page 58*: removed values for HSI clock source (16 MHz), Range 3. *Table 18: Current consumption in Run mode, code with data processing running from RAM on page 59*: removed values for HSI clock source (16 MHz), Range 3. *Table 19: Current consumption in Sleep mode on page 60* removed values for HSI clock source (16 MHz), Range 3 for both RAM and Flash; changed units. *Table 20: Current consumption in Low power run mode on page 62*: updated parameter and max value of I_{DD} Max (LP Run). *Table 21: Current consumption in Low power sleep mode on page 63*: updated symbol, parameter, and max value of I_{DD} Max (LP Sleep). *Table 22: Typical and maximum current consumptions in Stop mode on page 64* updated values for $I_{DD\ (Stop\ with\ RTC)}$ - RTC clocked by LSE external clock (32.768 kHz), regulator in LP mode, HSI and HSE OFF (no independent watchdog).