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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, Cap Sense, DMA, I ² S, POR, PWM, WDT
Number of I/O	83
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l151vbt6

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1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32L151x6/8/B and STM32L152x6/8/B ultra-low-power ARM® Cortex®-M3 based microcontrollers product line.

The ultra-low-power STM32L151x6/8/B and STM32L152x6/8/B family includes devices in 3 different package types: from 48 to 100 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the ultra-low-power STM32L151x6/8/B and STM32L152x6/8/B microcontroller family suitable for a wide range of applications:

- Medical and handheld equipment
- Application control and user interface
- PC peripherals, gaming, GPS and sport equipment
- Alarm systems, Wired and wireless sensors, Video intercom
- Utility metering

This STM32L151x6/8/B and STM32L152x6/8/B datasheet should be read in conjunction with the STM32L1xxxx reference manual (RM0038).

The document "Getting started with STM32L1xxxx hardware development" AN3216 gives a hardware implementation overview. Both documents are available from the STMicroelectronics website www.st.com.

For information on the ARM® Cortex®-M3 core please refer to the Cortex®-M3 Technical Reference Manual, available from the www.arm.com website.

Figure 1 shows the general block diagram of the device family.

Caution: This datasheet does not apply to STM32L15xx6/8/B-A covered by a separate datasheet.

3.4 Clock management

The clock controller distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low power modes and ensures clock robustness. It features:

- **Clock prescaler:** to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler
- **Safe clock switching:** clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management:** to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **Master clock source:** three different clock sources can be used to drive the master clock:
 - 1-24 MHz high-speed external crystal (HSE), that can supply a PLL
 - 16 MHz high-speed internal RC oscillator (HSI), trimmable by software, that can supply a PLL
 - Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 7 frequencies (65.5 kHz, 131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.1 MHz, 4.2 MHz) with a consumption proportional to speed, down to 750 nA typical. When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be trimmed by software down to a $\pm 0.5\%$ accuracy.
- **Auxiliary clock source:** two ultra-low-power clock sources that can be used to drive the LCD controller and the real-time clock:
 - 32.768 kHz low-speed external crystal (LSE)
 - 37 kHz low-speed internal RC (LSI), also used to drive the independent watchdog. The LSI clock can be measured using the high-speed internal RC oscillator for greater precision.
- **RTC and LCD clock sources:** the LSI, LSE or HSE sources can be chosen to clock the RTC and the LCD, whatever the system clock.
- **USB clock source:** the embedded PLL has a dedicated 48 MHz clock output to supply the USB interface.
- **Startup clock:** after reset, the microcontroller restarts by default with an internal 2.1 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** this feature can be enabled by software. If a HSE clock failure occurs, the master clock is automatically switched to HSI and a software interrupt is generated if enabled.
- **Clock-out capability (MCO: microcontroller clock output):** it outputs one of the internal clocks for external use by the application.

Several prescalers allow the configuration of the AHB frequency, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the AHB and the APB domains is 32 MHz. See [Figure 2](#) for details on the clock tree.

3.15.5 Window watchdog (WWDG)

The window watchdog is based on a 7-bit down-counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.16 Communication interfaces

3.16.1 I²C bus

Up to two I²C bus interfaces can operate in multimaster and slave modes. They can support standard and fast modes.

They support dual slave addressing (7-bit only) and both 7- and 10-bit addressing in master mode. A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SM Bus 2.0/PM Bus.

3.16.2 Universal synchronous/asynchronous receiver transmitter (USART)

All USART interfaces are able to communicate at speeds of up to 4 Mbit/s. They provide hardware management of the CTS and RTS signals and are ISO 7816 compliant. They support IrDA SIR ENDEC and have LIN Master/Slave capability.

All USART interfaces can be served by the DMA controller.

3.16.3 Serial peripheral interface (SPI)

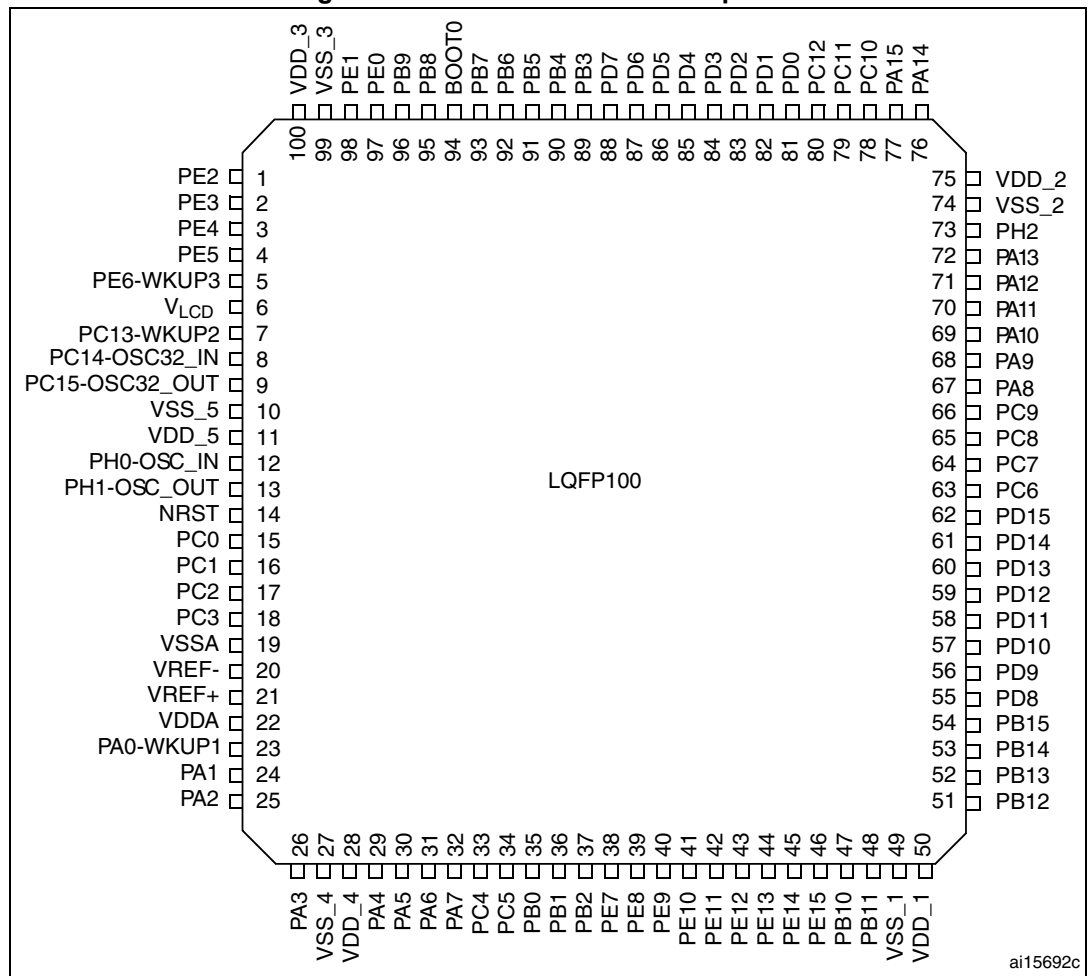
Up to two SPIs are able to communicate at up to 16 Mbits/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

Both SPIs can be served by the DMA controller.

3.16.4 Universal serial bus (USB)

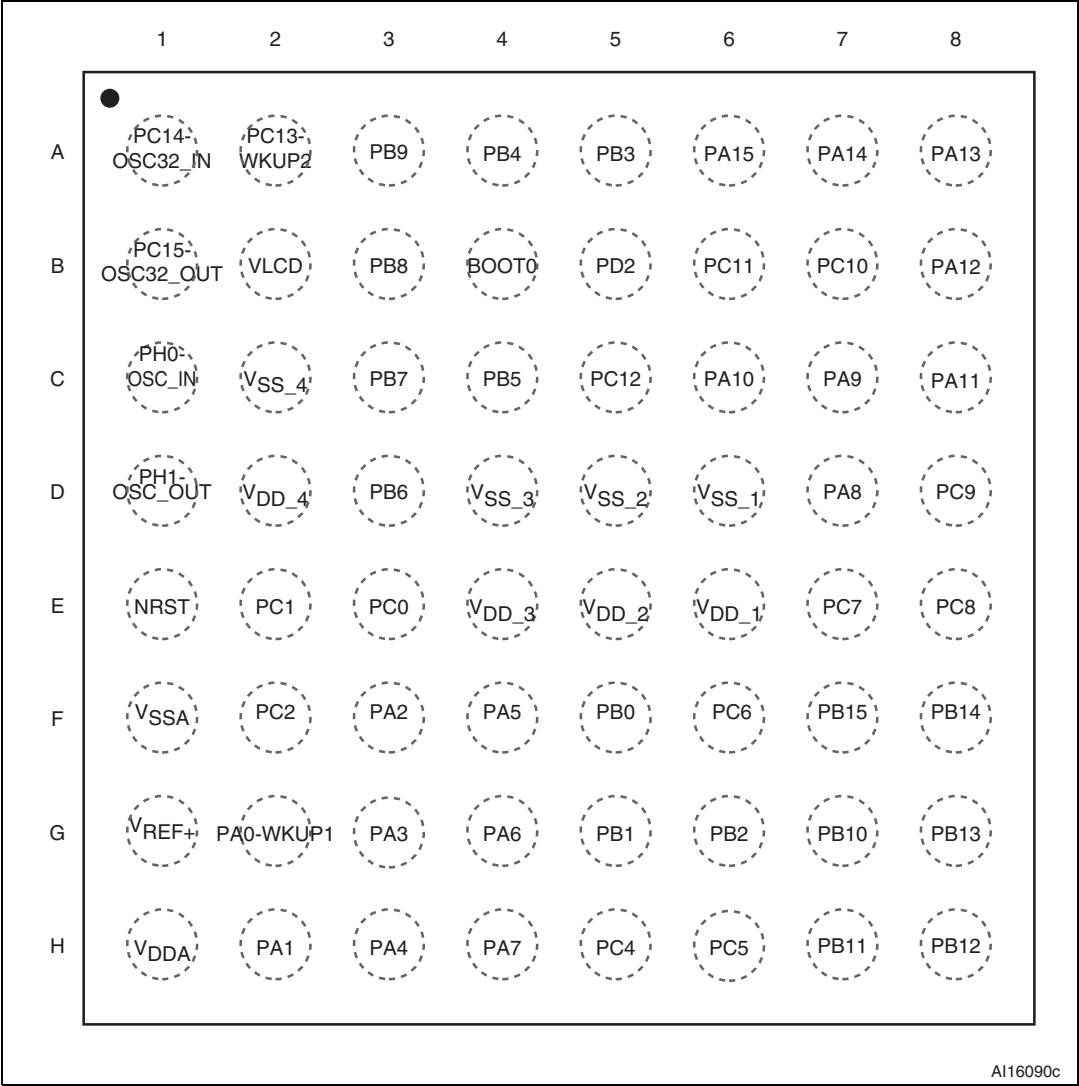
The STM32L151x6/8/B and STM32L152x6/8/B devices embed a USB device peripheral compatible with the USB full speed 12 Mbit/s. The USB interface implements a full speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and supports suspend/resume. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

Figure 4. STM32L15xVx LQFP100 pinout



1. This figure shows the package top view.

Figure 5. STM32L15xRx TFBGA64 ballout



1. This figure shows the package top view.

Table 7. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S		Supply pin
	I		Input only pin
	I/O		Input / output pin
I/O structure	FT		5 V tolerant I/O
	TC		Standard 3.3 V I/O
	B		Dedicated BOOT0 pin
	RST		Bidirectional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 8. STM32L151x6/8/B and STM32L152x6/8/B pin definitions (continued)

Pins					Pin name	Pin type ⁽¹⁾	I/O structure	Main function ⁽²⁾ (after reset)	Pins functions	Additional functions
LQFP100	LQFP64	TFBGA64	UFBGA100	LQFP48 or UQFPN48					Alternate functions	
35	26	F5	M5	18	PB0	I/O	TC	PB0	TIM3_CH3/LCD_SEG5	ADC_IN8/ COMP1_INP/ VREF_OUT
36	27	G5	M6	19	PB1	I/O	FT	PB1	TIM3_CH4/LCD_SEG6	ADC_IN9/ COMP1_INP/ VREF_OUT
37	28	G6	L6	20	PB2	I/O	FT	PB2/BOOT1	BOOT1	-
38	-	-	M7	-	PE7	I/O	TC	PE7	-	ADC_IN22/ COMP1_INP
39	-	-	L7	-	PE8	I/O	TC	PE8	-	ADC_IN23/ COMP1_INP
40	-	-	M8	-	PE9	I/O	TC	PE9	TIM2_CH1_ETR	ADC_IN24/ COMP1_INP
41	-	-	L8	-	PE10	I/O	TC	PE10	TIM2_CH2	ADC_IN25/ COMP1_INP
42	-	-	M9	-	PE11	I/O	FT	PE11	TIM2_CH3	-
43	-	-	L9	-	PE12	I/O	FT	PE12	TIM2_CH4/SPI1_NSS	-
44	-	-	M10	-	PE13	I/O	FT	PE13	SPI1_SCK	-
45	-	-	M11	-	PE14	I/O	FT	PE14	SPI1_MISO	-
46	-	-	M12	-	PE15	I/O	FT	PE15	SPI1_MOSI	-
47	29	G7	L10	21	PB10	I/O	FT	PB10	I2C2_SCL/USART3_TX/ TIM2_CH3/LCD_SEG10	-
48	30	H7	L11	22	PB11	I/O	FT	PB11	I2C2_SDA/USART3_RX/ TIM2_CH4/LCD_SEG11	-
49	31	D6	F12	23	V _{SS_1}	S	-	V _{SS_1}	-	-
50	32	E6	G12	24	V _{DD_1}	S	-	V _{DD_1}	-	-
51	33	H8	L12	25	PB12	I/O	FT	PB12	SPI2_NSS/I2C2_SMBA/ USART3_CK/ LCD_SEG12/TIM10_CH1	ADC_IN18/ COMP1_INP
52	34	G8	K12	26	PB13	I/O	FT	PB13	SPI2_SCK/USART3_CTS/ LCD_SEG13/ TIM9_CH1	ADC_IN19/ COMP1_INP

Table 9. Alternate function input/output (continued)

Port name	Digital alternate function number														
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFIO6	AFIO7	AFIO8	AFIO9	AFIO11	AFIO12	AFIO13	AFIO14	AFIO15
	Alternate function														
	SYSTEM	TIM2	TIM3/4	TIM9/10/11	I2C1/2	SPI1/2	N/A	USART1/2/3	N/A	N/A	LCD	N/A	N/A	RI	SYSTEM
PH1-OSC_OUT	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PH2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

6.3.3 Embedded internal reference voltage

The parameters given in the following table are based on characterization results, unless otherwise specified.

Table 15. Embedded internal reference voltage calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at temperature of 30 °C, $V_{DDA} = 3$ V	0x1FF8 0078-0x1FF8 0079

Table 16. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{REFINT_out}^{(1)}$	Internal reference voltage	$-40\text{ °C} < T_J < +105\text{ °C}$	1.202	1.224	1.242	V
I_{REFINT}	Internal reference current consumption	-	-	1.4	2.3	μA
$T_{VREFINT}$	Internal reference startup time	-	-	2	3	ms
V_{VREF_MEAS}	V_{DDA} and V_{REF+} voltage during V_{REFINT} factory measure	-	2.99	3	3.01	V
A_{VREF_MEAS}	Accuracy of factory-measured V_{REF} value ⁽²⁾	Including uncertainties due to ADC and V_{DDA}/V_{REF+} values	-	-	±5	mV
$T_{Coeff}^{(3)}$	Temperature coefficient	$-40\text{ °C} < T_J < +105\text{ °C}$	-	25	100	ppm/°C
$A_{Coeff}^{(3)}$	Long-term stability	1000 hours, $T = 25\text{ °C}$	-	-	1000	ppm
$V_{DDCoeff}^{(3)}$	Voltage coefficient	$3.0\text{ V} < V_{DDA} < 3.6\text{ V}$	-	-	2000	ppm/V
$T_{S_vrefint}^{(3)(4)}$	ADC sampling time when reading the internal reference voltage	-	5	10	-	μs
$T_{ADC_BUF}^{(3)}$	Startup time of reference voltage buffer for ADC	-	-	-	10	μs
$I_{BUF_ADC}^{(3)}$	Consumption of reference voltage buffer for ADC	-	-	13.5	25	μA
$I_{VREF_OUT}^{(3)}$	V_{REF_OUT} output current ⁽⁵⁾	-	-	-	1	μA
$C_{VREF_OUT}^{(3)}$	V_{REF_OUT} output load	-	-	-	50	pF
$I_{LPBUF}^{(3)}$	Consumption of reference voltage buffer for V_{REF_OUT} and COMP	-	-	730	1200	nA
$V_{REFINT_DIV1}^{(3)}$	1/4 reference voltage	-	24	25	26	% V_{REFINT}
$V_{REFINT_DIV2}^{(3)}$	1/2 reference voltage	-	49	50	51	
$V_{REFINT_DIV3}^{(3)}$	3/4 reference voltage	-	74	75	76	

1. Tested in production.

2. The internal V_{REF} value is individually measured in production and stored in dedicated EEPROM bytes.

3. Guaranteed by characterization results.

4. Shortest sampling time can be determined in the application by multiple iterations.

5. To guarantee less than 1% V_{REF_OUT} deviation.

6.3.4 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code. The current consumption is measured as described in [Figure 14: Current consumption measurement scheme](#).

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code.

The current consumption values are derived from the tests performed under ambient temperature $T_A=25^{\circ}\text{C}$ and V_{DD} supply voltage conditions summarized in [Table 13: General operating conditions](#), unless otherwise specified. The MCU is placed under the following conditions:

The MCU is placed under the following conditions:

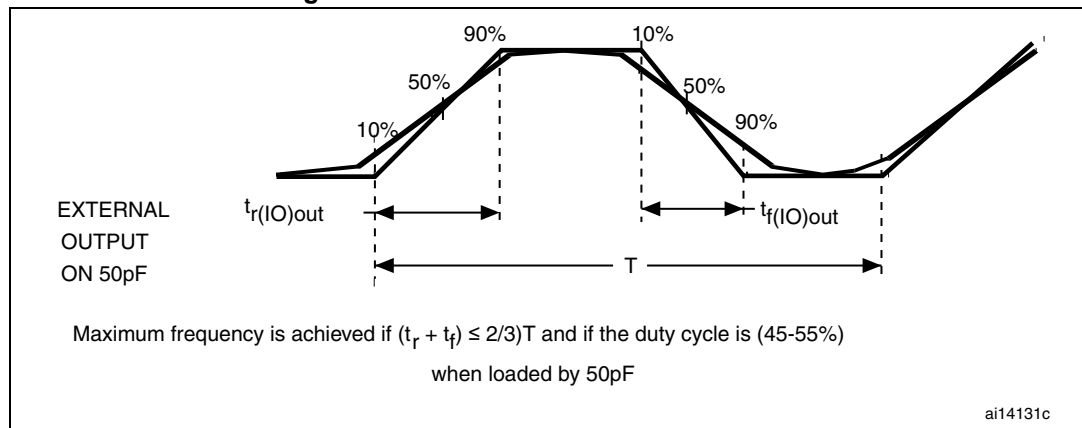
- $V_{DD} = 3.6\text{ V}$
- All I/O pins are configured in analog input mode.
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time, 64-bit access and prefetch is adjusted depending on f_{HCLK} frequency and voltage range to provide the best CPU performance.
- When the peripherals are enabled $f_{APB1} = f_{APB2} = f_{AHB}$
- When PLL is ON, the PLL inputs are equal to HSI = 16 MHz (if internal clock is used) or HSE = 16 MHz (if HSE bypass mode is used).
- The HSE user clock applied to OSC_IN input follows the characteristics specified in [Table 26: High-speed external user clock characteristics](#).

Table 21. Current consumption in Low power sleep mode

Symbol	Parameter	Conditions			Typ	Max (1)	Unit
I_{DD} (LP Sleep)	Supply current in Low power sleep mode	All peripherals OFF, V_{DD} from 1.65 V to 3.6 V	MSI clock, 65 kHz $f_{HCLK} = 32$ kHz Flash OFF	$T_A = -40$ °C to 25 °C	4.4	-	μA
			MSI clock, 65 kHz $f_{HCLK} = 32$ kHz Flash ON	$T_A = -40$ °C to 25 °C	17.5	25	
				$T_A = 85$ °C	22	27	
				$T_A = 105$ °C	31	39	
			MSI clock, 65 kHz $f_{HCLK} = 65$ kHz, Flash ON	$T_A = -40$ °C to 25 °C	18	26	
				$T_A = 85$ °C	23	28	
				$T_A = 105$ °C	31	40	
			MSI clock, 131 kHz $f_{HCLK} = 131$ kHz, Flash ON	$T_A = -40$ °C to 25 °C	22	30	
				$T_A = 55$ °C	24	32	
				$T_A = 85$ °C	26	34	
				$T_A = 105$ °C	34	45	
		TIM9 and USART1 enabled, Flash ON, V_{DD} from 1.65 V to 3.6 V	MSI clock, 65 kHz $f_{HCLK} = 32$ kHz	$T_A = -40$ °C to 25 °C	17.5	25	
				$T_A = 85$ °C	22	27	
				$T_A = 105$ °C	31	39	
			MSI clock, 65 kHz $f_{HCLK} = 65$ kHz	$T_A = -40$ °C to 25 °C	18	26	
				$T_A = 85$ °C	23	28	
				$T_A = 105$ °C	31	40	
			MSI clock, 131 kHz $f_{HCLK} = 131$ kHz	$T_A = -40$ °C to 25 °C	22	30	
				$T_A = 55$ °C	24	32	
				$T_A = 85$ °C	26	34	
				$T_A = 105$ °C	34	45	
I_{DD} Max (LP Sleep)	Max allowed current in Low power Sleep mode	V_{DD} from 1.65 V to 3.6 V	-	-	-	200	

1. Guaranteed by characterization results, unless otherwise specified.

Figure 19. I/O AC characteristics definition



6.3.14 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, RPU (see [Table 45](#)).

Unless otherwise specified, the parameters given in [Table 45](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 13](#).

Table 45. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}^{(1)}$	NRST input low level voltage	-	-	-	0.8	V
$V_{IH(NRST)}^{(1)}$	NRST input high level voltage	-	1.4	-		
$V_{OL(NRST)}^{(1)}$	NRST output low level voltage	$I_{OL} = 2 \text{ mA}$ $2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$	-	-	0.4	
		$I_{OL} = 1.5 \text{ mA}$ $1.65 \text{ V} < V_{DD} < 2.7 \text{ V}$	-	-		
$V_{hys(NRST)}^{(1)}$	NRST Schmitt trigger voltage hysteresis	-	-	$10\%V_{DD}^{(2)}$		mV
R_{PU}	Weak pull-up equivalent resistor ⁽³⁾	$V_{IN} = V_{SS}$	30	45	60	kΩ
$V_F(NRST)^{(1)}$	NRST input filtered pulse	-	-	-	50	ns
$V_{NF(NRST)}^{(1)}$	NRST input not filtered pulse	-	350	-		ns

1. Guaranteed by design.

2. 200 mV minimum value

3. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is around 10%.

SPI characteristics

Unless otherwise specified, the parameters given in the following table are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in [Table 13](#).

Refer to [Section 6.3.12: I/O current injection characteristics](#) for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 49. SPI characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Max ⁽²⁾	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	16	MHz
		Slave mode	-	16	
		Slave transmitter	-	12 ⁽³⁾	
$t_{r(SCK)}^{(2)}$ $t_{f(SCK)}^{(2)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	6	ns
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	30	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode	$4t_{HCLK}$	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	$2t_{HCLK}$	-	
$t_{w(SCKH)}^{(2)}$ $t_{w(SCKL)}^{(2)}$	SCK high and low time	Master mode	$t_{SCK}/2 - 5$	$t_{SCK}/2 + 3$	
$t_{su(MI)}^{(2)}$	Data input setup time	Master mode	5	-	
$t_{su(SI)}^{(2)}$		Slave mode	6	-	
$t_{h(MI)}^{(2)}$	Data input hold time	Master mode	5	-	
$t_{h(SI)}^{(2)}$		Slave mode	5	-	
$t_{a(SO)}^{(4)}$	Data output access time	Slave mode	0	$3t_{HCLK}$	
$t_{v(SO)}^{(2)}$	Data output valid time	Slave mode	-	33	
$t_{v(MO)}^{(2)}$	Data output valid time	Master mode	-	6.5	
$t_{h(SO)}^{(2)}$	Data output hold time	Slave mode	17	-	
$t_{h(MO)}^{(2)}$		Master mode	0.5	-	

1. The characteristics above are given for voltage Range 1.
2. Guaranteed by characterization results.
3. The maximum SPI clock frequency in slave transmitter mode is given for an SPI slave input clock duty cycle (DuCy(SCK)) ranging between 40 to 60%.
4. Min time is for the minimum time to drive the output and max time is for the maximum time to validate the data.

6.3.21 LCD controller (STM32L152xx only)

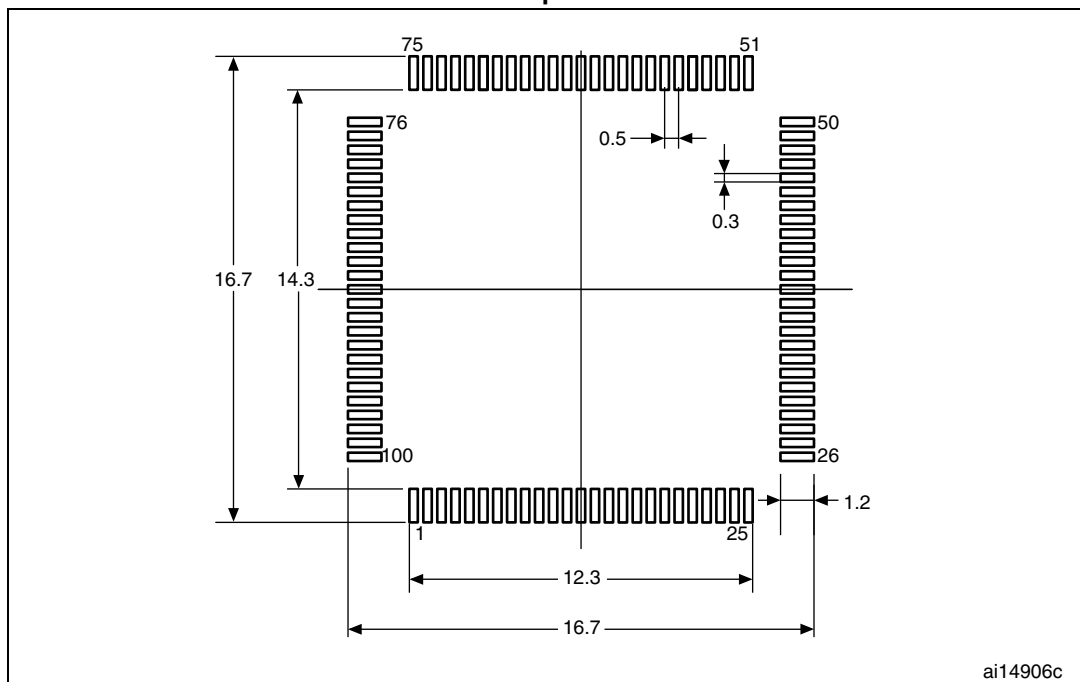
The STM32L152xx embeds a built-in step-up converter to provide a constant LCD reference voltage independently from the V_{DD} voltage. An external capacitor C_{ext} must be connected to the V_{LCD} pin to decouple this converter.

Table 62. LCD controller characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{LCD}	LCD external voltage	-	-	3.6	V
V_{LCD0}	LCD internal reference voltage 0	-	2.6	-	
V_{LCD1}	LCD internal reference voltage 1	-	2.73	-	
V_{LCD2}	LCD internal reference voltage 2	-	2.86	-	
V_{LCD3}	LCD internal reference voltage 3	-	2.98	-	
V_{LCD4}	LCD internal reference voltage 4	-	3.12	-	
V_{LCD5}	LCD internal reference voltage 5	-	3.26	-	
V_{LCD6}	LCD internal reference voltage 6	-	3.4	-	
V_{LCD7}	LCD internal reference voltage 7	-	3.55	-	
C_{ext}	V_{LCD} external capacitance	0.1	-	2	μF
$I_{LCD}^{(1)}$	Supply current at $V_{DD} = 2.2 V$	-	3.3	-	μA
	Supply current at $V_{DD} = 3.0 V$	-	3.1	-	
$R_{Htot}^{(2)}$	Low drive resistive network overall value	5.28	6.6	7.92	$M\Omega$
$R_L^{(2)}$	High drive resistive network total value	192	240	288	$k\Omega$
V_{44}	Segment/Common highest level voltage	-	-	V_{LCD}	V
V_{34}	Segment/Common 3/4 level voltage	-	$3/4 V_{LCD}$	-	V
V_{23}	Segment/Common 2/3 level voltage	-	$2/3 V_{LCD}$	-	
V_{12}	Segment/Common 1/2 level voltage	-	$1/2 V_{LCD}$	-	
V_{13}	Segment/Common 1/3 level voltage	-	$1/3 V_{LCD}$	-	
V_{14}	Segment/Common 1/4 level voltage	-	$1/4 V_{LCD}$	-	
V_0	Segment/Common lowest level voltage	0	-	-	
$\Delta V_{xx}^{(3)}$	Segment/Common level voltage error $T_A = -40$ to $85^\circ C$	-	-	± 50	mV

1. LCD enabled with 3 V internal step-up active, 1/8 duty, 1/4 bias, division ratio= 64, all pixels active, no LCD connected
2. Guaranteed by design.
3. Guaranteed by characterization results.

Figure 33. LQPF100 14 x 14 mm, 100-pin low-profile quad flat package recommended footprint

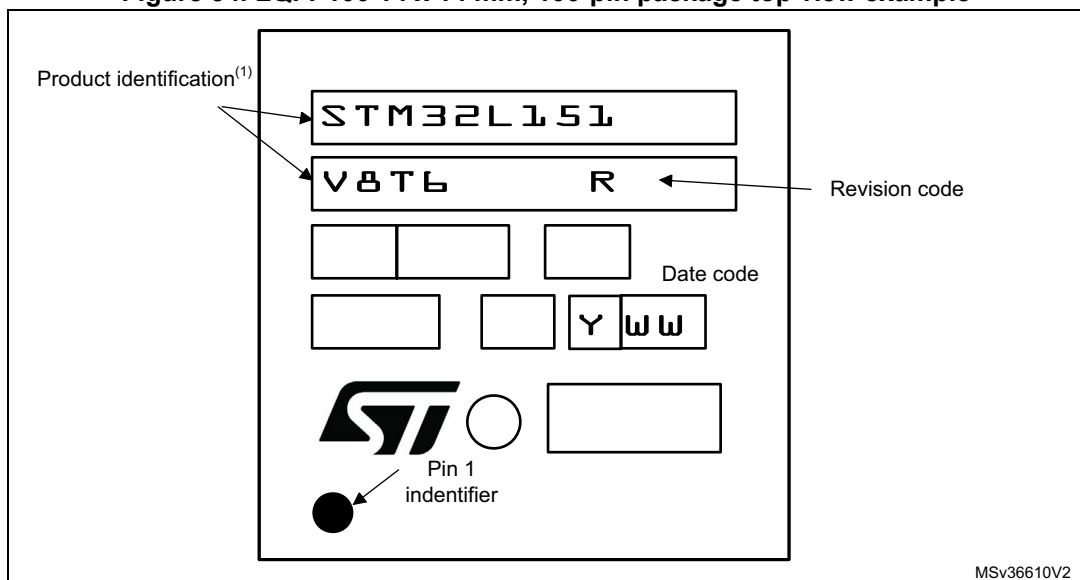


1. Dimensions are in millimeters.

LQFP100 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

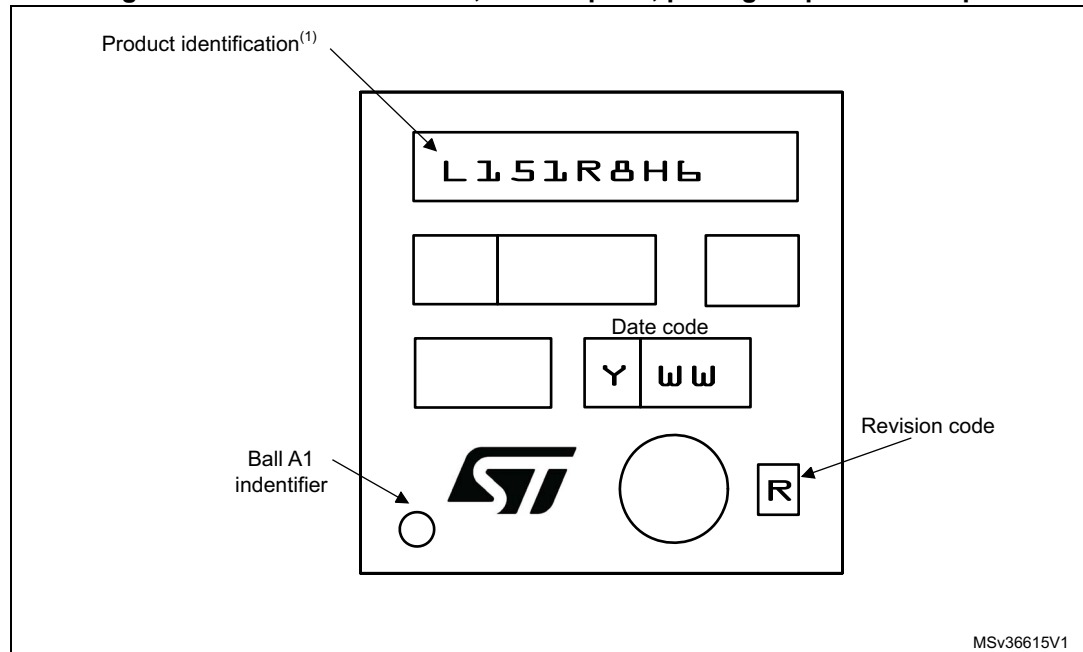
Figure 34. LQFP100 14 x 14 mm, 100-pin package top view example



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

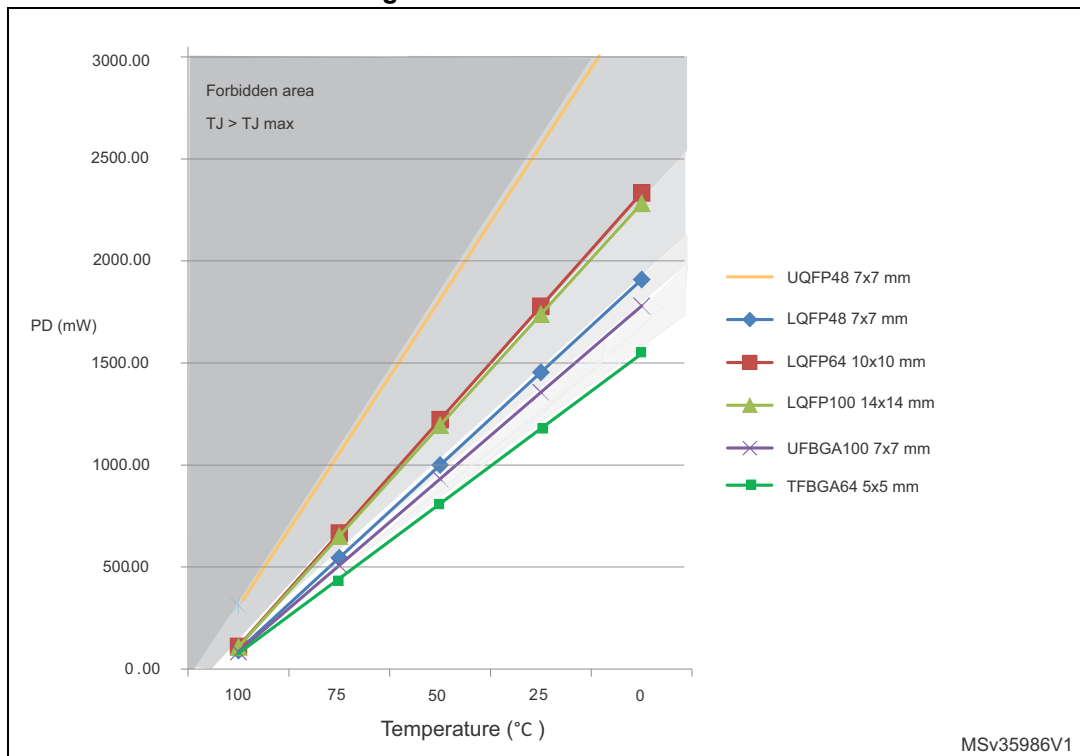
TFBGA64 device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Figure 49. TFBGA64 5 x 5 mm, 0.5 mm pitch, package top view example

1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Figure 50. Thermal resistance



7.7.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.