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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

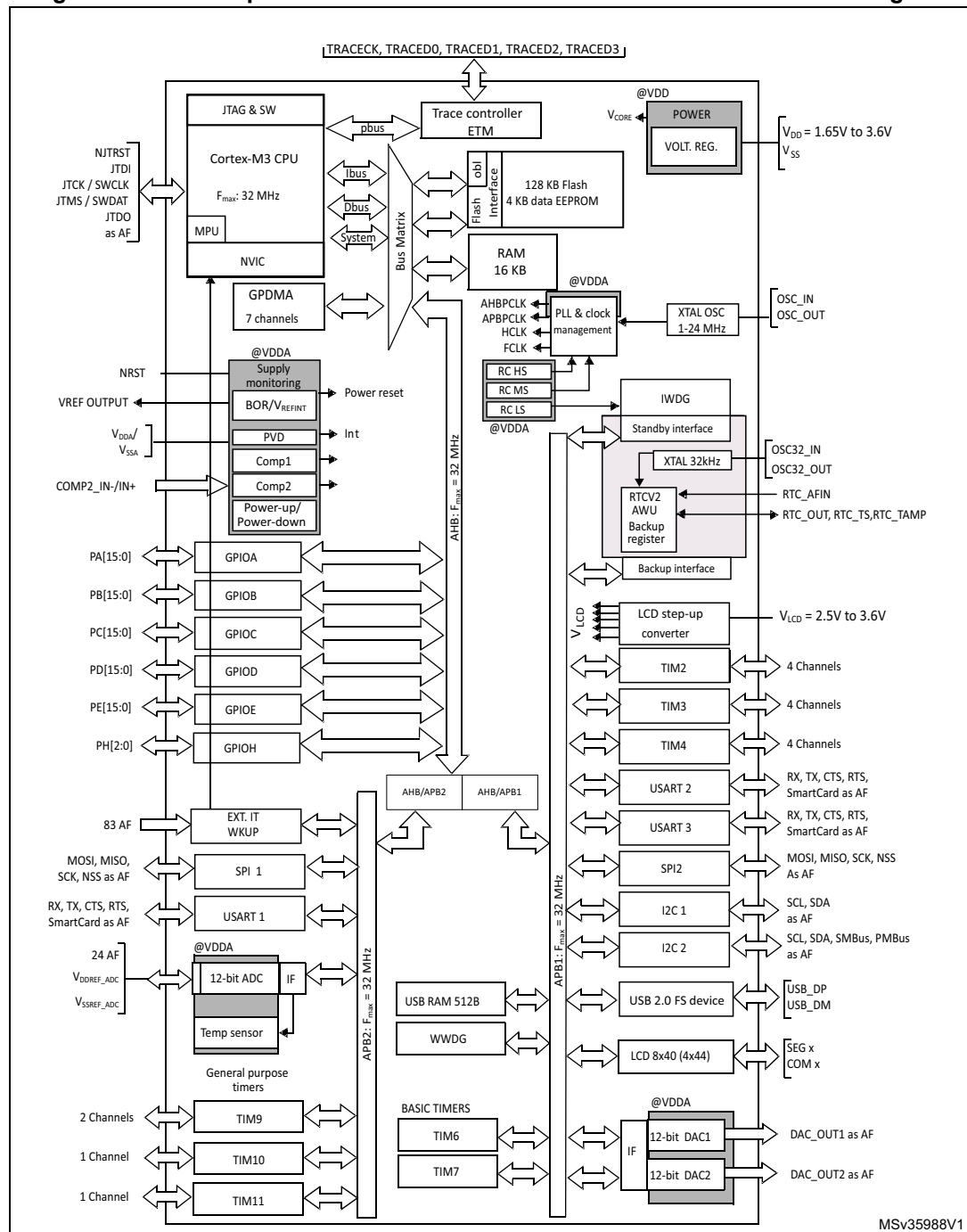
Details

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, Cap Sense, DMA, I ² S, LCD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UFQFPN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l152c6u6

3 Functional overview

Figure 1 shows the block diagram.

Figure 1. Ultra-low-power STM32L151x6/8/B and STM32L152x6/8/B block diagram



1. AF = alternate function on I/O port pin.

Nested vectored interrupt controller (NVIC)

The ultra-low-power STM32L151x6/8/B and STM32L152x6/8/B devices embed a nested vectored interrupt controller able to handle up to 45 maskable interrupt channels (not including the 16 interrupt lines of Cortex[®]-M3) and 16 priority levels.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving*, higher-priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.3 Reset and supply management

3.3.1 Power supply schemes

- $V_{DD} = 1.65$ to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA} , $V_{DDA} = 1.65$ to 3.6 V: external analog power supplies for ADC, reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 1.8 V when the ADC is used). V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} , respectively.

3.3.2 Power supply supervisor

The device has an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR) that can be coupled with a brownout reset (BOR) circuitry.

The device exists in two versions:

- The version with BOR activated at power-on operates between 1.8 V and 3.6 V.
- The other version without BOR operates between 1.65 V and 3.6 V.

After the V_{DD} threshold is reached (1.65 V or 1.8 V depending on the BOR which is active or not at power-on), the option byte loading process starts, either to confirm or modify default thresholds, or to disable the BOR permanently: in this case, the V_{DD} min value becomes 1.65 V (whatever the version, BOR active or not, at power-on).

When BOR is active at power-on, it ensures proper operation starting from 1.8 V whatever the power ramp-up phase before it reaches 1.8 V. When BOR is not active at power-up, the power ramp-up should guarantee that 1.65 V is reached on V_{DD} at least 1 ms after it exits the POR area.

3.7 Memories

The STM32L151x6/8/B and STM32L152x6/8/B devices have the following features:

- Up to 16 Kbytes of embedded RAM accessed (read/write) at CPU clock speed with 0 wait states. With the enhanced bus matrix, operating the RAM does not lead to any performance penalty during accesses to the system bus (AHB and APB buses).
- The non-volatile memory is divided into three arrays:
 - 32, 64 or 128 Kbytes of embedded Flash program memory
 - 4 Kbytes of data EEPROM
 - Options bytes

The options bytes are used to write-protect the memory (with 4 Kbytes granularity) and/or readout-protect the whole memory with the following options:

- Level 0: no readout protection
- Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
- Level 2: chip readout protection, debug features (Cortex[®]-M3 JTAG and serial wire) and boot in RAM selection disabled (JTAG fuse)

The whole non-volatile memory embeds the error correction code (ECC) feature.

3.8 DMA (direct memory access)

The flexible 7-channel, general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I²C, USART, general-purpose timers and ADC.

3.9 LCD (liquid crystal display)

The LCD drives up to 8 common terminals and 44 segment terminals to drive up to 320 pixels.

- Internal step-up converter to guarantee functionality and contrast control irrespective of V_{DD} . This converter can be deactivated, in which case the V_{LCD} pin is used to provide the voltage to the LCD
- Supports static, 1/2, 1/3, 1/4 and 1/8 duty
- Supports static, 1/2, 1/3 and 1/4 bias
- Phase inversion to reduce power consumption and EMI
- Up to 8 pixels can be programmed to blink
- Unneeded segments and common pins can be used as general I/O pins
- LCD RAM can be updated at any time owing to a double-buffer
- The LCD controller can operate in Stop mode

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channels' independent or simultaneous conversions
- DMA capability for each channel (including the underrun interrupt)
- external triggers for conversion
- input reference voltage V_{REF+}

Eight DAC trigger inputs are used in the STM32L151x6/8/B and STM32L152x6/8/B devices. The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

3.12 Ultra-low-power comparators and reference voltage

The STM32L151x6/8/B and STM32L152x6/8/B devices embed two comparators sharing the same current bias and reference voltage. The reference voltage can be internal or external (coming from an I/O).

- one comparator with fixed threshold
- one comparator with rail-to-rail inputs, fast or slow mode. The threshold can be one of the following:
 - DAC output
 - External I/O
 - Internal reference voltage (V_{REFINT}) or V_{REFINT} submultiple (1/4, 1/2, 3/4)

Both comparators can wake up from Stop mode, and be combined into a window comparator.

The internal reference voltage is available externally via a low power / low current output buffer (driving current capability of 1 μ A typical).

3.13 Routing interface

This interface controls the internal routing of I/Os to TIM2, TIM3, TIM4 and to the comparator and reference voltage output.

3.14 Touch sensing

The STM32L151x6/8/B and STM32L152x6/8/B devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 20 capacitive sensing channels distributed over 10 analog I/O groups. Only software capacitive sensing acquisition mode is supported.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (glass, plastic, ...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven

3.17 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.18 Development support

Serial wire JTAG debug port (SWJ-DP)

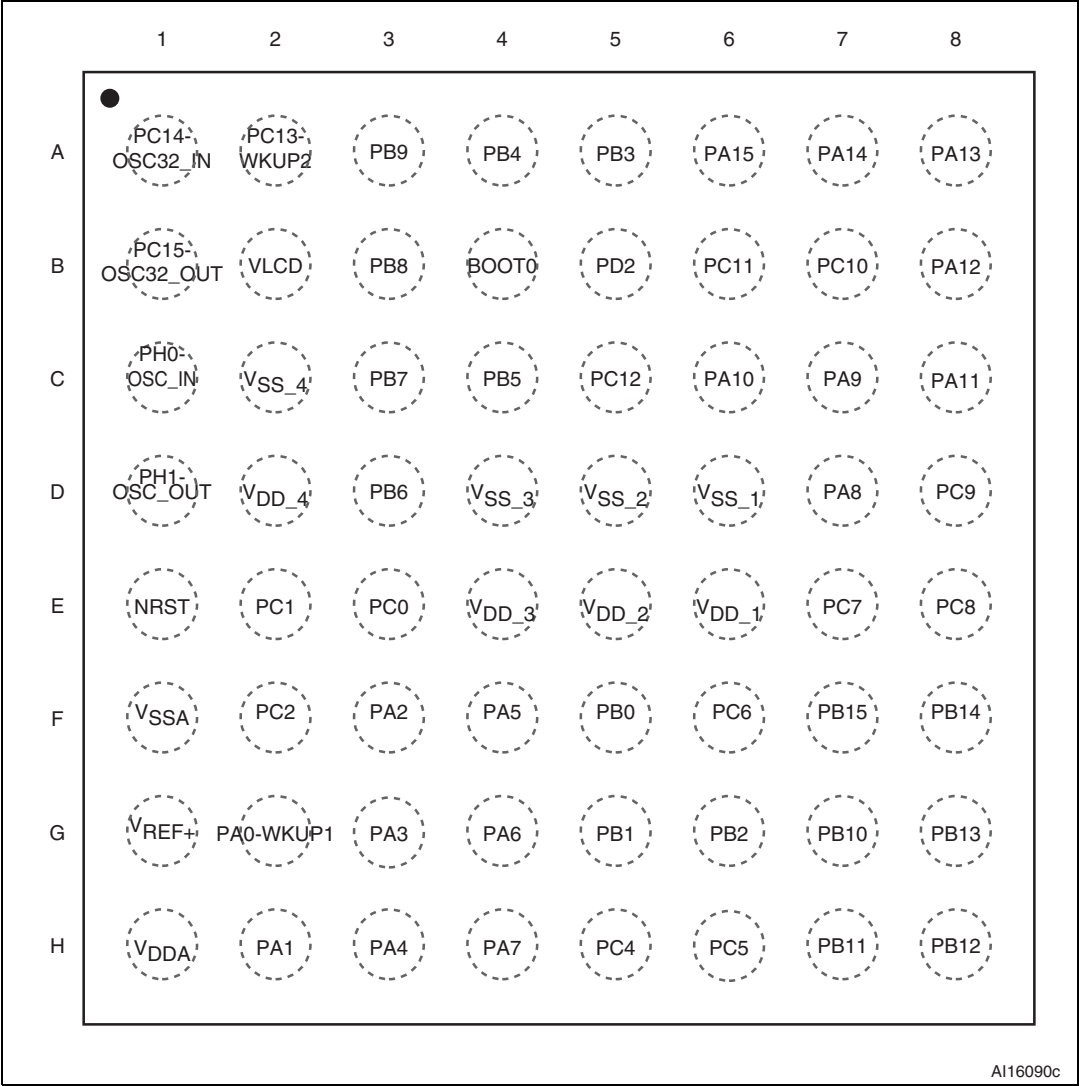
The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG JTMS and JTCK pins are shared with SWDAT and SWCLK, respectively, and a specific sequence on the JTMS pin is used to switch between JTAG-DP and SW-DP.

The JTAG port can be permanently disabled with a JTAG fuse.

Embedded Trace Macrocell™

The ARM Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32L151x6/8/B and STM32L152x6/8/B device through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer running debugger software. TPA hardware is commercially available from common development tool vendors. It operates with third party debugger software tools.

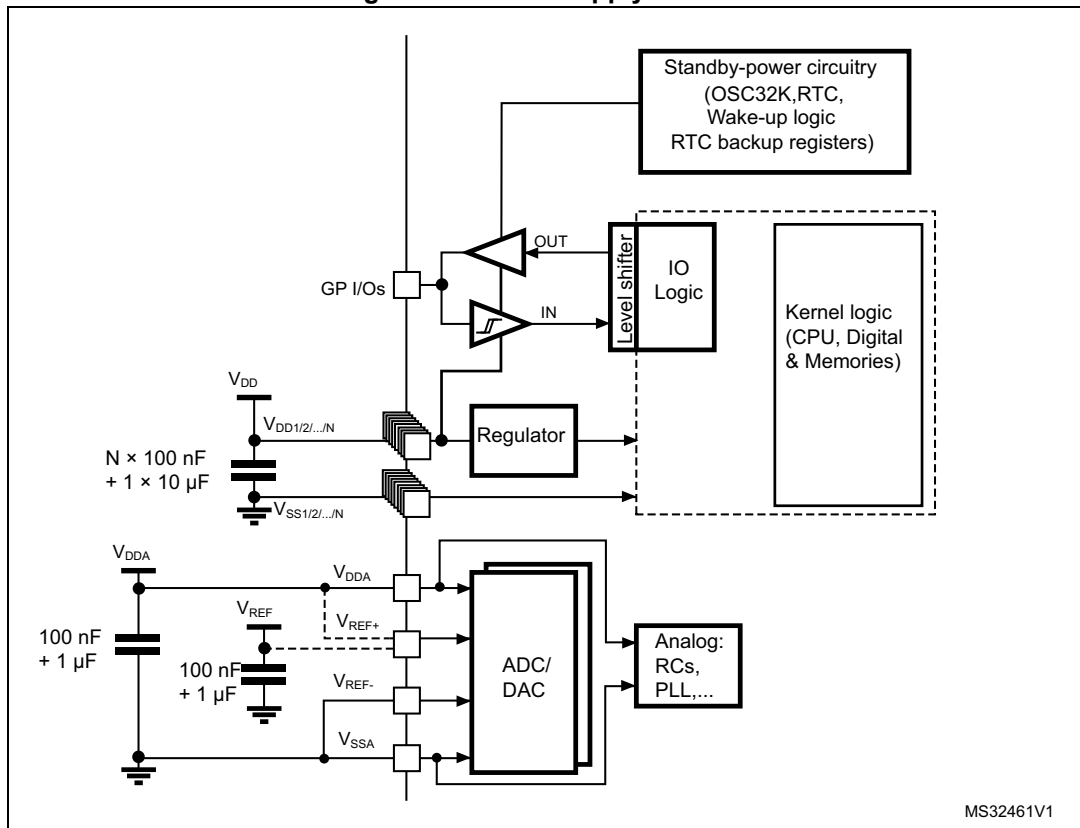
Figure 5. STM32L15xRx TFBGA64 ballout



1. This figure shows the package top view.

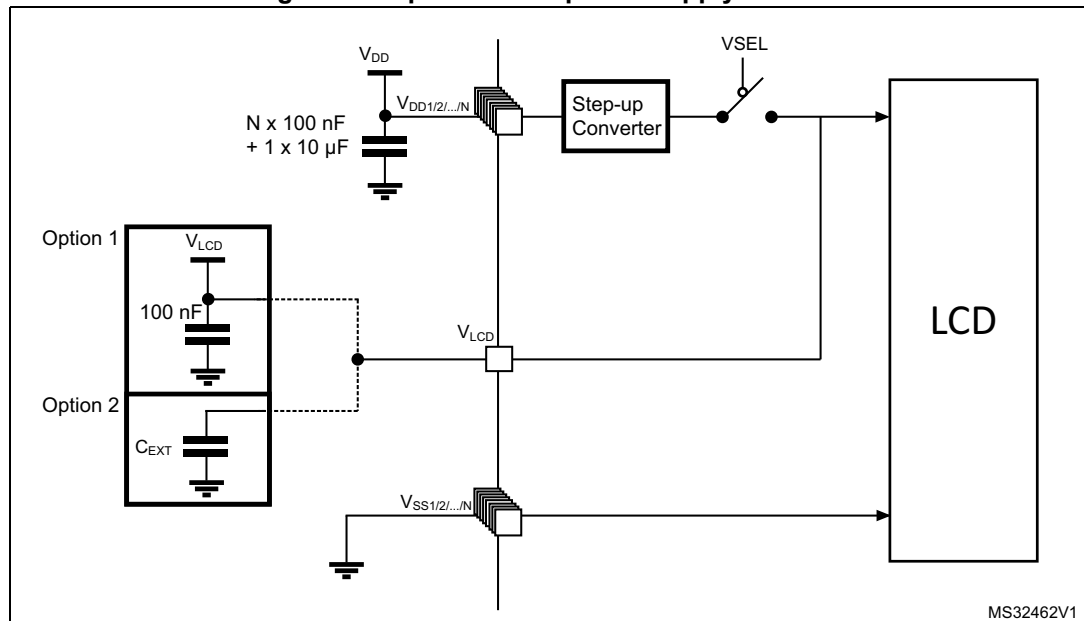
6.1.6 Power supply scheme

Figure 12. Power supply scheme



6.1.7 Optional LCD power supply scheme

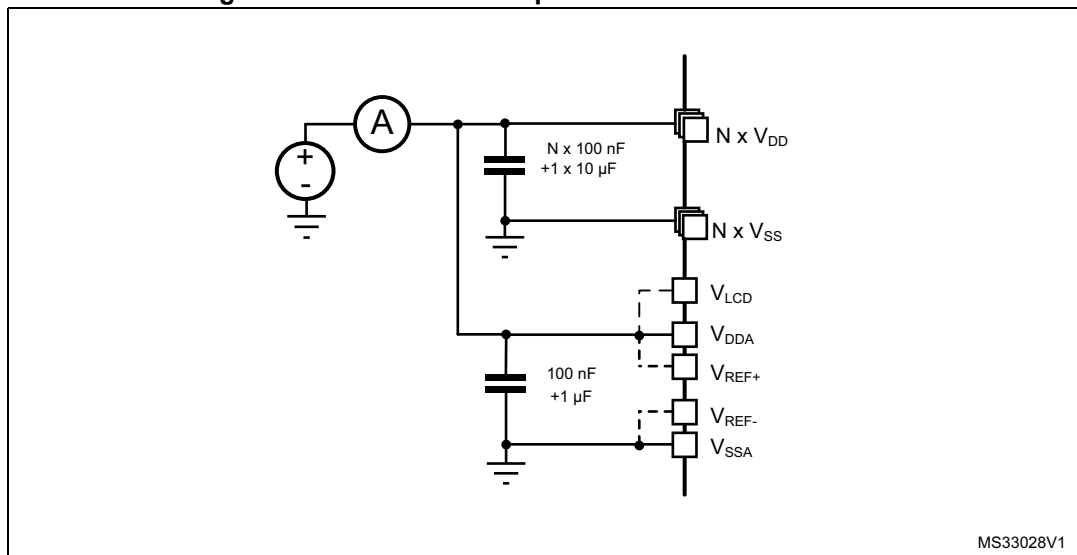
Figure 13. Optional LCD power supply scheme



1. Option 1: LCD power supply is provided by a dedicated V_{LCD} supply source, V_{SEL} switch is open.
2. Option 2: LCD power supply is provided by the internal step-up converter, V_{SEL} switch is closed, an external capacitance is needed for correct behavior of this converter.

6.1.8 Current consumption measurement

Figure 14. Current consumption measurement scheme



6.3.3 Embedded internal reference voltage

The parameters given in the following table are based on characterization results, unless otherwise specified.

Table 15. Embedded internal reference voltage calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at temperature of 30 °C, $V_{DDA} = 3$ V	0x1FF8 0078-0x1FF8 0079

Table 16. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{REFINT_out}^{(1)}$	Internal reference voltage	$-40\text{ °C} < T_J < +105\text{ °C}$	1.202	1.224	1.242	V
I_{REFINT}	Internal reference current consumption	-	-	1.4	2.3	μA
$T_{VREFINT}$	Internal reference startup time	-	-	2	3	ms
V_{VREF_MEAS}	V_{DDA} and V_{REF+} voltage during V_{REFINT} factory measure	-	2.99	3	3.01	V
A_{VREF_MEAS}	Accuracy of factory-measured V_{REF} value ⁽²⁾	Including uncertainties due to ADC and V_{DDA}/V_{REF+} values	-	-	±5	mV
$T_{Coeff}^{(3)}$	Temperature coefficient	$-40\text{ °C} < T_J < +105\text{ °C}$	-	25	100	ppm/°C
$A_{Coeff}^{(3)}$	Long-term stability	1000 hours, $T = 25\text{ °C}$	-	-	1000	ppm
$V_{DDCoeff}^{(3)}$	Voltage coefficient	$3.0\text{ V} < V_{DDA} < 3.6\text{ V}$	-	-	2000	ppm/V
$T_{S_vrefint}^{(3)(4)}$	ADC sampling time when reading the internal reference voltage	-	5	10	-	μs
$T_{ADC_BUF}^{(3)}$	Startup time of reference voltage buffer for ADC	-	-	-	10	μs
$I_{BUF_ADC}^{(3)}$	Consumption of reference voltage buffer for ADC	-	-	13.5	25	μA
$I_{VREF_OUT}^{(3)}$	$VREF_OUT$ output current ⁽⁵⁾	-	-	-	1	μA
$C_{VREF_OUT}^{(3)}$	$VREF_OUT$ output load	-	-	-	50	pF
$I_{LPBUF}^{(3)}$	Consumption of reference voltage buffer for $VREF_OUT$ and COMP	-	-	730	1200	nA
$V_{REFINT_DIV1}^{(3)}$	1/4 reference voltage	-	24	25	26	% V_{REFINT}
$V_{REFINT_DIV2}^{(3)}$	1/2 reference voltage	-	49	50	51	
$V_{REFINT_DIV3}^{(3)}$	3/4 reference voltage	-	74	75	76	

1. Tested in production.

2. The internal V_{REF} value is individually measured in production and stored in dedicated EEPROM bytes.

3. Guaranteed by characterization results.

4. Shortest sampling time can be determined in the application by multiple iterations.

5. To guarantee less than 1% $VREF_OUT$ deviation.

Table 20. Current consumption in Low power run mode

Symbol	Parameter	Conditions			Typ	Max (1)	Unit
I_{DD} (LP Run)	Supply current in Low power run mode	All peripherals OFF, code executed from RAM, Flash switched OFF, V_{DD} from 1.65 V to 3.6 V	MSI clock, 65 kHz $f_{HCLK} = 32$ kHz	$T_A = -40\text{ }^{\circ}\text{C}$ to $25\text{ }^{\circ}\text{C}$	9	12	μA
				$T_A = 85\text{ }^{\circ}\text{C}$	17.5	24	
				$T_A = 105\text{ }^{\circ}\text{C}$	31	46	
			MSI clock, 65 kHz $f_{HCLK} = 65$ kHz	$T_A = -40\text{ }^{\circ}\text{C}$ to $25\text{ }^{\circ}\text{C}$	14	17	
				$T_A = 85\text{ }^{\circ}\text{C}$	22	29	
				$T_A = 105\text{ }^{\circ}\text{C}$	35	51	
			MSI clock, 131 kHz $f_{HCLK} = 131$ kHz	$T_A = -40\text{ }^{\circ}\text{C}$ to $25\text{ }^{\circ}\text{C}$	37	42	
				$T_A = 55\text{ }^{\circ}\text{C}$	37	42	
				$T_A = 85\text{ }^{\circ}\text{C}$	37	42	
				$T_A = 105\text{ }^{\circ}\text{C}$	48	65	
		All peripherals OFF, code executed from Flash, V_{DD} from 1.65 V to 3.6 V	MSI clock, 65 kHz $f_{HCLK} = 32$ kHz	$T_A = -40\text{ }^{\circ}\text{C}$ to $25\text{ }^{\circ}\text{C}$	24	32	
				$T_A = 85\text{ }^{\circ}\text{C}$	33	42	
				$T_A = 105\text{ }^{\circ}\text{C}$	48	64	
			MSI clock, 65 kHz $f_{HCLK} = 65$ kHz	$T_A = -40\text{ }^{\circ}\text{C}$ to $25\text{ }^{\circ}\text{C}$	31	40	
				$T_A = 85\text{ }^{\circ}\text{C}$	40	48	
				$T_A = 105\text{ }^{\circ}\text{C}$	54	70	
			MSI clock, 131 kHz $f_{HCLK} = 131$ kHz	$T_A = -40\text{ }^{\circ}\text{C}$ to $25\text{ }^{\circ}\text{C}$	48	58	
				$T_A = 55\text{ }^{\circ}\text{C}$	54	63	
				$T_A = 85\text{ }^{\circ}\text{C}$	56	65	
				$T_A = 105\text{ }^{\circ}\text{C}$	70	90	
I_{DD} Max (LP Run) ⁽²⁾	Max allowed current in Low power run mode	V_{DD} from 1.65 V to 3.6 V	-	-	-	200	

1. Guaranteed by characterization results, unless otherwise specified.
2. This limitation is related to the consumption of the CPU core and the peripherals that are powered by the regulator. Consumption of the I/Os is not included in this limitation.

Table 28. HSE oscillator characteristics⁽¹⁾⁽²⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	1		24	MHz
R_F	Feedback resistor	-		200	-	k Ω
C	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S) ⁽³⁾	$R_S = 30 \Omega$	-	20	-	pF
I_{HSE}	HSE driving current	$V_{DD} = 3.3 V$, $V_{IN} = V_{SS}$ with 30 pF load	-	-	3	mA
$I_{DD(HSE)}$	HSE oscillator power consumption	$C = 20 \text{ pF}$ $f_{OSC} = 16 \text{ MHz}$	-	-	2.5 (startup) 0.7 (stabilized)	mA
		$C = 10 \text{ pF}$ $f_{OSC} = 16 \text{ MHz}$	-	-	2.5 (startup) 0.46 (stabilized)	
g_m	Oscillator transconductance	Startup	3.5	-	-	mA/ μ V
$t_{SU(HSE)}^{(4)}$	Startup time	V_{DD} is stabilized	-	1	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by characterization results.
3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

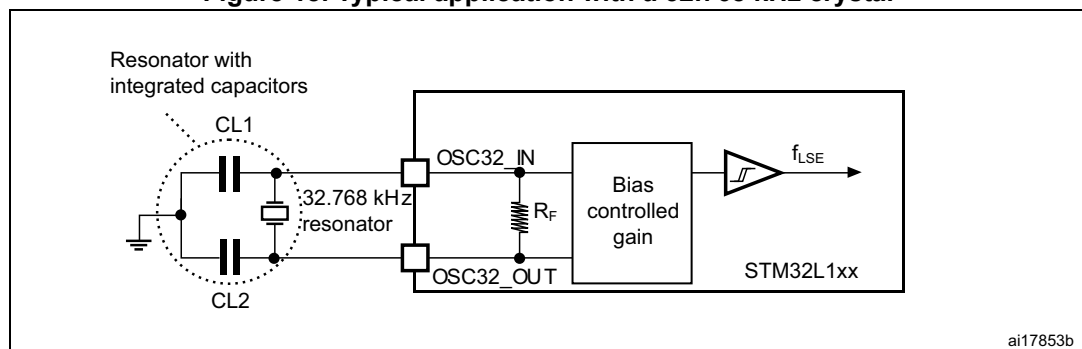
For C_{L1} and C_{L2} , it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see [Figure 17](#)). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2} . PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2} . Refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

4. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Note: For CL1 and CL2, it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator (see [Figure 18](#)). CL1 and CL2, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of CL1 and CL2. Load capacitance CL has the following formula: $CL = CL1 \times CL2 / (CL1 + CL2) + C_{stray}$ where C_{stray} is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

Caution: To avoid exceeding the maximum value of CL1 and CL2 (15 pF) it is strongly recommended to use a resonator with a load capacitance $CL \leq 7$ pF. Never use a resonator with a load capacitance of 12.5 pF. Example: if a resonator is chosen with a load capacitance of $CL = 6$ pF and $C_{stray} = 2$ pF, then $CL1 = CL2 = 8$ pF.

Figure 18. Typical application with a 32.768 kHz crystal



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ± 8 mA, and sink or source up to ± 20 mA (with the non-standard V_{OL}/V_{OH} specifications given in [Table 43](#)).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in [Section 6.2](#):

- The sum of the currents sourced by all the I/Os on V_{DD} , plus the maximum Run consumption of the MCU sourced on V_{DD} , cannot exceed the absolute maximum rating $I_{VDD\Sigma}$ (see [Table 11](#)).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating $I_{VSS\Sigma}$ (see [Table 11](#)).

Output voltage levels

Unless otherwise specified, the parameters given in [Table 43](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 13](#). All I/Os are CMOS and TTL compliant.

Table 43. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{OL}^{(1)(2)}$	Output low level voltage for an I/O pin	$I_{IO} = 8$ mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
$V_{OH}^{(3)(2)}$	Output high level voltage for an I/O pin		2.4	-	
$V_{OL}^{(1)(4)}$	Output low level voltage for an I/O pin	$I_{IO} = 4$ mA 1.65 V < V_{DD} < 2.7 V	-	0.45	
$V_{OH}^{(3)(4)}$	Output high level voltage for an I/O pin		$V_{DD}-0.45$	-	
$V_{OL}^{(1)(4)}$	Output low level voltage for an I/O pin	$I_{IO} = 20$ mA 2.7 V < V_{DD} < 3.6 V	-	1.3	
$V_{OH}^{(3)(4)}$	Output high level voltage for an I/O pin		$V_{DD}-1.3$	-	

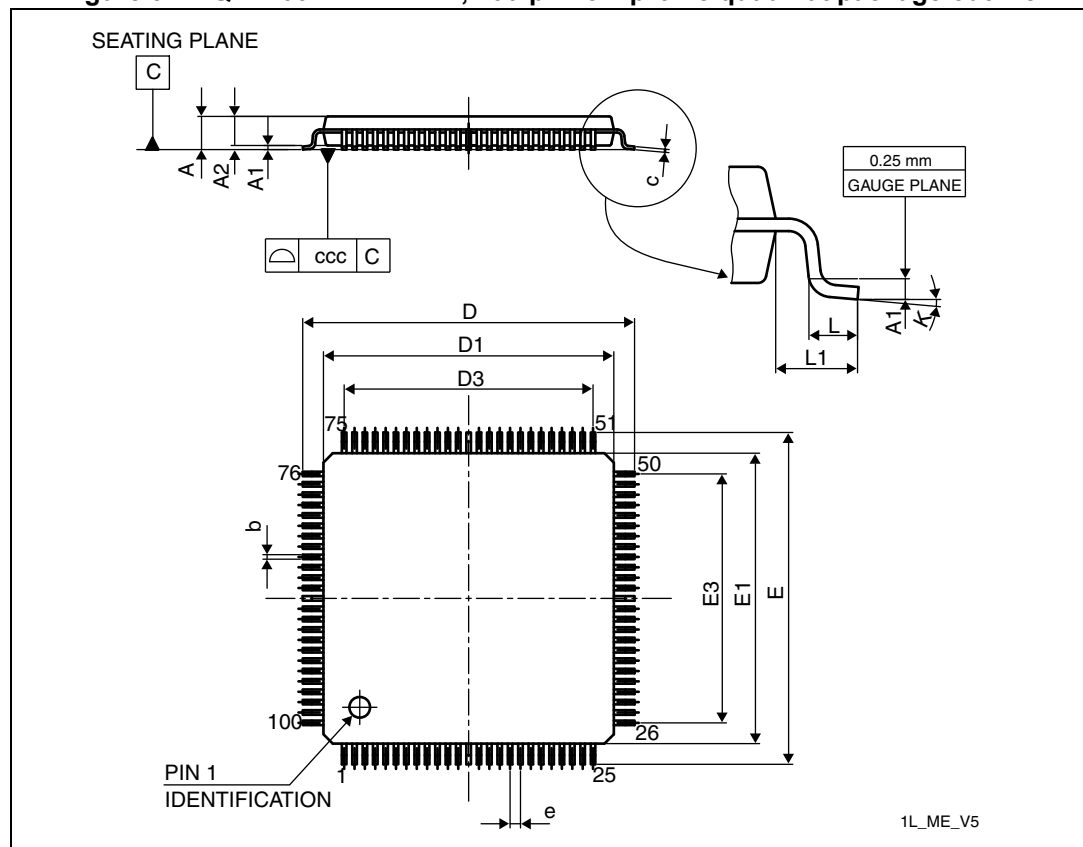
1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in [Table 11](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS} .
2. Tested in production.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in [Table 11](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD} .
4. Guaranteed by characterization results.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

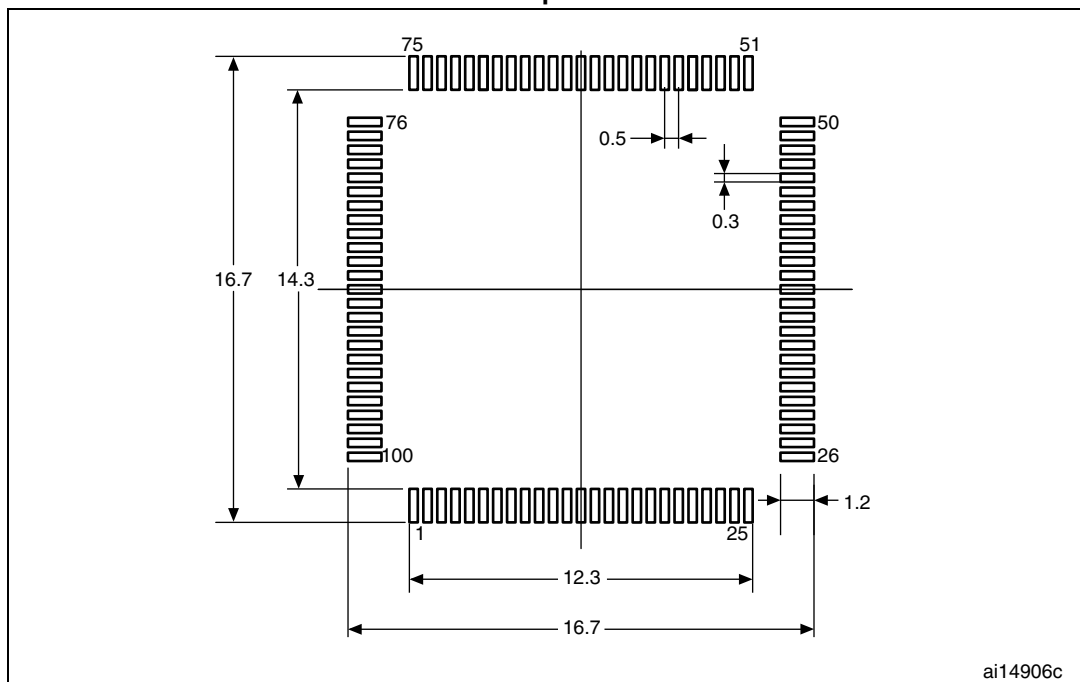
7.1 LQFP100 14 x 14 mm, 100-pin low-profile quad flat package information

Figure 32. LQFP100 14 x 14 mm, 100-pin low-profile quad flat package outline



1. Drawing is not to scale.

Figure 33. LQPF100 14 x 14 mm, 100-pin low-profile quad flat package recommended footprint

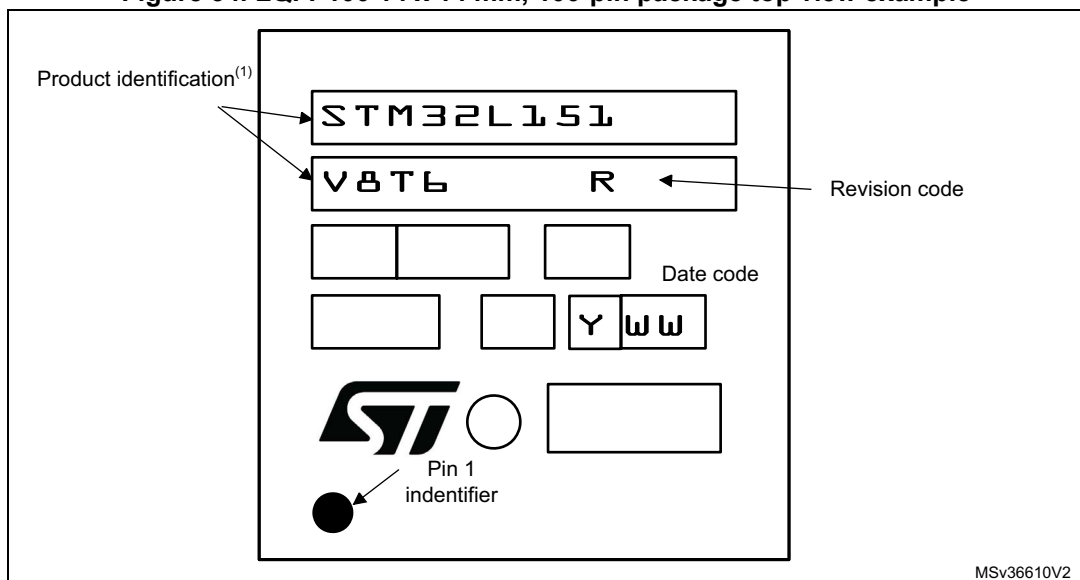


1. Dimensions are in millimeters.

LQFP100 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 34. LQFP100 14 x 14 mm, 100-pin package top view example

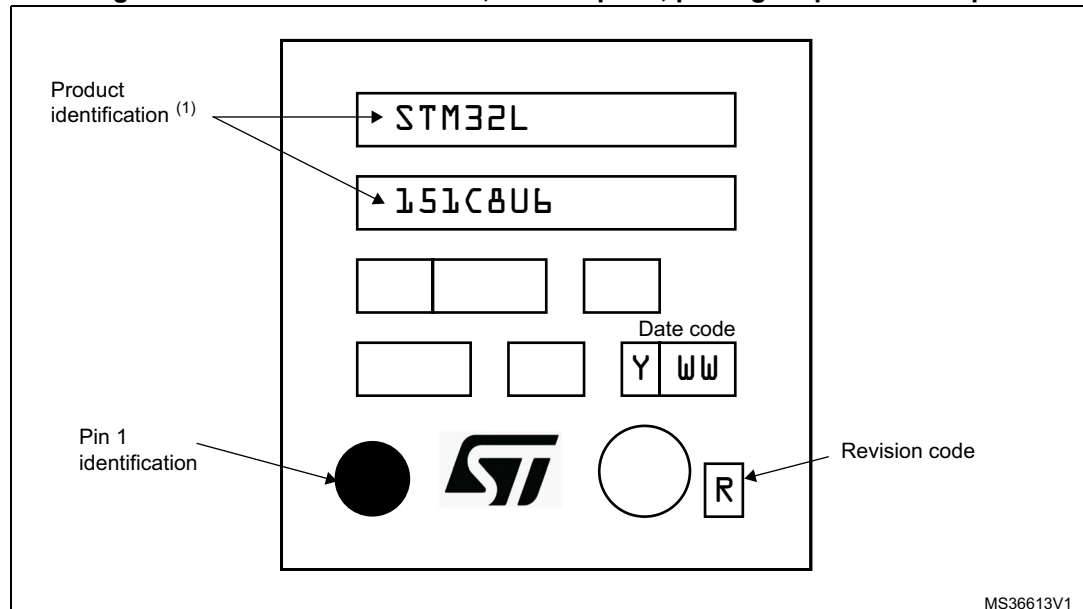


1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

UFQFPN48 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 43. UFQFPN48 7 x 7 mm, 0.5 mm pitch, package top view example

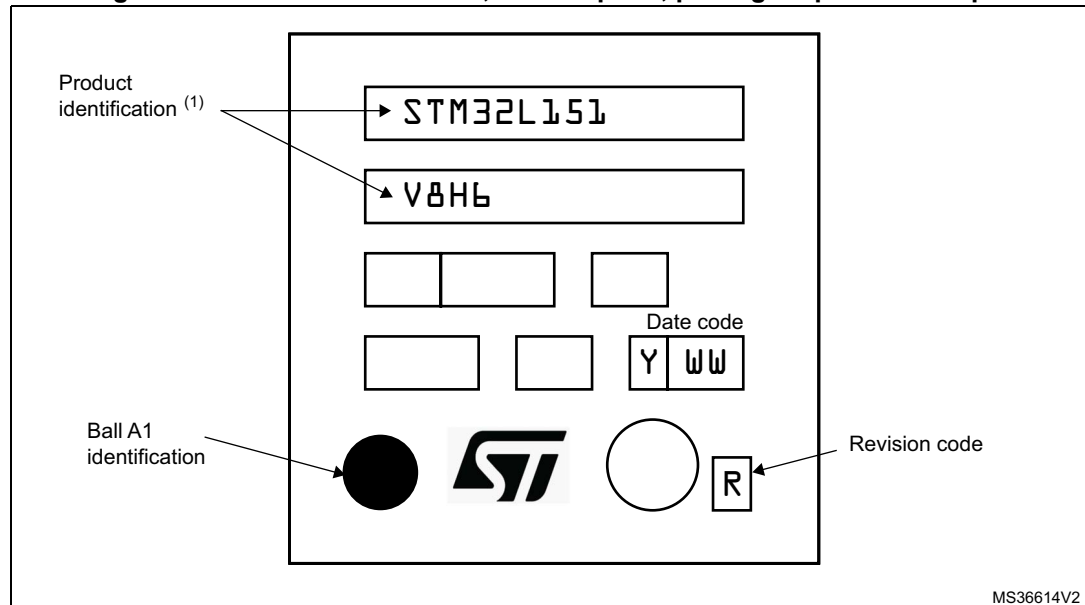


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UFBGA100 device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Figure 46. UFBGA100 7 x 7 mm, 0.5 mm pitch, package top view example



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Table 73. Document revision history (continued)

Date	Revision	Changes
17-June-2011	5	<p>Modified 1st page (low power features)</p> <p>Added STM32L15xC6 and STM32L15xR6 devices (32 Kbytes of Flash memory).</p> <p>Modified Section 3.6: GPIOs (general-purpose inputs/outputs) on page 22</p> <p>Modified Section 6.3: Operating conditions on page 53</p> <p>Modified Table 55: ADC accuracy on page 95, Table 57: DAC characteristics on page 99 and Table 60: Comparator 1 characteristics on page 102</p>
25-Jan-2012	6	<p>Features: updated internal multispeed low power RC.</p> <p>Table 2: Ultralow power STM32L15xx6/8/B device features and peripheral counts: LCD 4x44 and 8x40 available for both 64- and 128-Kbyte devices; two comparators available for all devices.</p> <p>Table 3: Functionalities depending on the operating power supply range: added footnote 1.</p> <p>Figure 8: STM32L15xCx UFQFPN48 pinout: replaced VFQPN48 by UFQFPN48 as name of package.</p> <p>Table 8: STM32L15xx6/8/B pin definitions: replaced PH0/PH1 by PC14/PC15.</p> <p>Table 9: Alternate function input/output: removed EVENT OUT from PH2 port, AFIO15 column.</p> <p>Table 19: Current consumption in Sleep mode: updated MSI conditions and f_{HCLK}.</p> <p>Table 20: Current consumption in Low power run mode: updated some temperature conditions; added footnote 2.</p> <p>Table 21: Current consumption in Low power sleep mode: updated some temperature conditions and one of the MSI clock conditions.</p> <p>Table 22: Typical and maximum current consumptions in Stop mode: updated I_{DD} (WU from Stop) parameter.</p> <p>Table 23: Typical and maximum current consumptions in Standby mode: updated I_{DD} (WU from Standby) parameter.</p> <p>Table 25: Low-power mode wakeup timings: updated f_{HCLK} value for $t_{WUSLEEP_LP}$; updated typical value of parameter "Wakeup from Stop mode, regulator in Run mode".</p> <p>Table 24: Peripheral current consumption: replaced GPIOF by GPIOH.</p> <p>Table 33: PLL characteristics: updated "PLL output clock"</p> <p>Table 35: Flash memory and data EEPROM characteristics: updated all information for I_{DD}.</p> <p>Figure 19: I/O AC characteristics definition: replaced the falling edge "$t_{f(I/O)out}$" by "$t_{f(I/O)out}$".</p> <p>Table 47: I2C characteristics: amended footnote 2.</p> <p>Table 54: ADC characteristics: updated f_S max value for direct channels, 6-bit sampling rate.</p> <p>Table 55: ADC accuracy: Updated the first, third and fourth f_{ADC} test condition.</p> <p>Table 59: Temperature sensor characteristics: updated typ, min, and max values of the T_{S_temp} parameter.</p>

Table 73. Document revision history (continued)

Date	Revision	Changes
12-Nov-2013	9 (continued)	<p>Updated Table 54: ADC characteristics and Figure 27: Typical connection diagram using the ADC.</p> <p>Table 58: Temperature sensor calibration values was previously in Section 3.10.1: Temperature sensor. Updated Table 59: Temperature sensor characteristics.</p> <p>In Table 61: Comparator 2 characteristics, parameter dThreshold/dt, replaced any occurrence of "VREF+" by "V_{REFINT}". Updated Table 63: LQPF100 14 x 14 mm, 100-pin low-profile quad flat package mechanical data, Table 64: LQFP64 10 x 10 mm 64-pin low-profile quad flat package mechanical data, Table 65: LQFP48 7 x 7 mm, 48-pin low-profile quad flat package mechanical data and Table 66: UFQFPN48 7 x 7 mm, 0.5 mm pitch, ultra thin fine-pitch quad flat no-lead package mechanical data.</p> <p>Updated Figure 33: LQFP100 recommended footprint.</p> <p>Updated Figure 46: TFBGA64 - 5.0x5.0x1.2 mm, 0.5 mm pitch, thin fine-pitch ball grid array package outline title.</p> <p>Remove minimum and typical values of A dimension in Table 67: UFBGA100 7 x 7 x 0.6 mm 0.5 mm pitch, ultra thin fine-pitch ball grid array package mechanical data</p> <p>Deleted second footnote in Figure 42: UFQFPN48 recommended footprint.</p> <p>Updated Section 8: Ordering information title and added first sentence.</p> <p>Changed BOR disabled option identifier in Table 72: Ordering information scheme.</p>
22-Jul-2014	10	<p>Updated Figure 14, Figure 15.</p> <p>Updated Table 5.</p> <p>Updated Figure 6.3.4.</p> <p>Updated note 5 inside Table 54.</p> <p>Updated Ro value inside Table 54.</p>