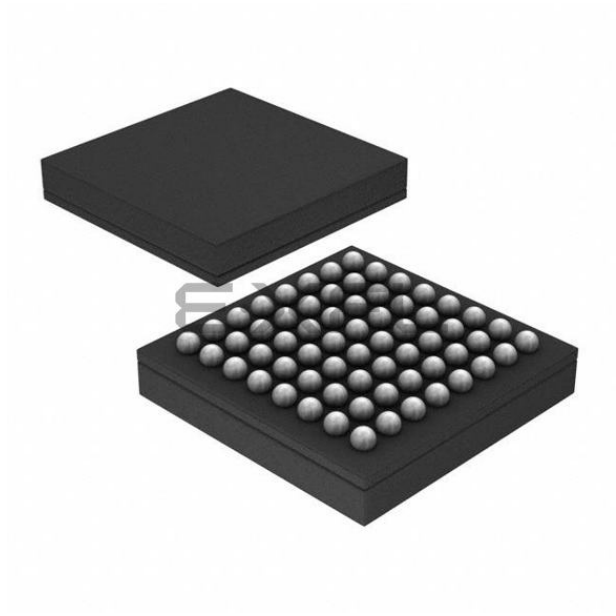

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 32MHz |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, Cap Sense, DMA, I²S, LCD, POR, PWM, WDT |
| Number of I/O | 51 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 4K x 8 |
| RAM Size | 10K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 20x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-TFBGA |
| Supplier Device Package | 64-TFBGA (5x5) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l152r6h6 |

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## 3.1 Low power modes

The ultra-low-power STM32L151x6/8/B and STM32L152x6/8/B devices support dynamic voltage scaling to optimize its power consumption in run mode. The voltage from the internal low-drop regulator that supplies the logic can be adjusted according to the system's maximum operating frequency and the external voltage supply:

- In Range 1 ($V_{DD}$ range limited to 1.71-3.6 V), the CPU runs at up to 32 MHz (refer to *Table 17* for consumption).
- In Range 2 (full $V_{DD}$ range), the CPU runs at up to 16 MHz (refer to *Table 17* for consumption)
- In Range 3 (full $V_{DD}$ range), the CPU runs at up to 4 MHz (generated only with the multispeed internal RC oscillator clock source). Refer to *Table 17* for consumption.

Seven low power modes are provided to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

  Sleep mode power consumption: refer to *Table 19*.

- **Low power run** mode

  This mode is achieved with the multispeed internal (MSI) RC oscillator set to the minimum clock (65 kHz), execution from SRAM or Flash memory, and internal regulator in low power mode to minimize the regulator's operating current. In the Low power run mode, the clock frequency and the number of enabled peripherals are both limited.

  Low power run mode consumption: refer to *Table 20: Current consumption in Low power run mode*.

- **Low power sleep** mode

  This mode is achieved by entering the Sleep mode with the internal voltage regulator in Low power mode to minimize the regulator's operating current. In the Low power sleep mode, both the clock frequency and the number of enabled peripherals are limited; a typical example would be to have a timer running at 32 kHz.
  When wakeup is triggered by an event or an interrupt, the system reverts to the run mode with the regulator on.

  Low power sleep mode consumption: refer to *Table 21: Current consumption in Low power sleep mode*.

- **Stop** mode with RTC

  Stop mode achieves the lowest power consumption while retaining the RAM and register contents and real time clock. All clocks in the $V_{CORE}$ domain are stopped, the PLL, MSI RC, HSI RC and HSE crystal oscillators are disabled. The LSE or LSI is still running. The voltage regulator is in the low power mode.

  The device can be woken up from Stop mode by any of the EXTI line, in 8 µs. The EXTI line source can be one of the 16 external lines. It can be the PVD output, the Comparator 1 event or Comparator 2 event (if internal reference voltage is on), it can be the RTC alarm(s), the USB wakeup, the RTC tamper events, the RTC timestamp event or the RTC wakeup.

- **Stop** mode without RTC

  Stop mode achieves the lowest power consumption while retaining the RAM and register contents. All clocks are stopped, the PLL, MSI RC, HSI and LSI RC, LSE and

HSE crystal oscillators are disabled. The voltage regulator is in the low power mode. The device can be woken up from Stop mode by any of the EXTI line, in 8 µs. The EXTI line source can be one of the 16 external lines. It can be the PVD output, the Comparator 1 event or Comparator 2 event (if internal reference voltage is on). It can also be wakened by the USB wakeup.

Stop mode consumption: refer to *Table 22: Typical and maximum current consumptions in Stop mode*.

- **Standby** mode with RTC

  Standby mode is used to achieve the lowest power consumption and real time clock. The internal voltage regulator is switched off so that the entire $V_{CORE}$ domain is powered off. The PLL, MSI RC, HSI RC and HSE crystal oscillators are also switched off. The LSE or LSI is still running. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC_CSR).

  The device exits Standby mode in 60 µs when an external reset (NRST pin), an IWDG reset, a rising edge on one of the three WKUP pins, RTC alarm (Alarm A or Alarm B), RTC tamper event, RTC timestamp event or RTC Wakeup event occurs.

- **Standby** mode without RTC

  Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire $V_{CORE}$ domain is powered off. The PLL, MSI, RC, HSI and LSI RC, HSE and LSE crystal oscillators are also switched off. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC_CSR).

  The device exits Standby mode in 60 µs when an external reset (NRST pin) or a rising edge on one of the three WKUP pin occurs.

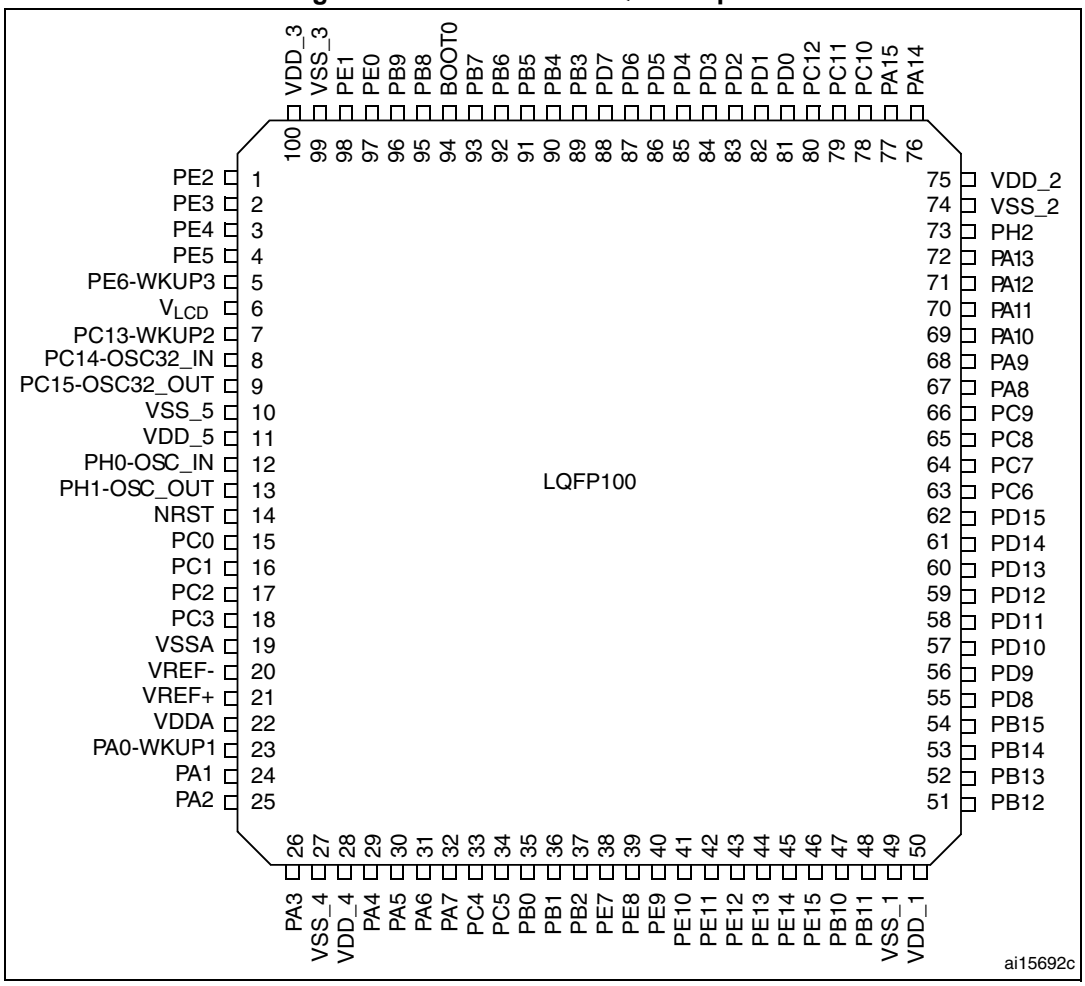
  Standby mode consumption: refer to *Table 23*.

*Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering the Stop or Standby mode.*

**Table 3. Functionalities depending on the operating power supply range**

| Operating power supply range | Functionalities depending on the operating power supply range | | | |
|---|---|---|---|---|
| | DAC and ADC operation | USB | Dynamic voltage scaling range | I/O operation |
| $V_{DD}$ = 1.65 to 1.71 V | Not functional | Not functional | Range 2 or Range 3 | Degraded speed performance |
| $V_{DD}$ = 1.71 to 1.8 V(1) | Not functional | Not functional | Range 1, Range 2 or Range 3 | Degraded speed performance |
| $V_{DD}$ = 1.8 to 2.0 V(1) | Conversion time up to 500 Ksps | Not functional | Range 1, Range 2 or Range 3 | Degraded speed performance |

**Figure 4. STM32L15xVx LQFP100 pinout**




1. This figure shows the package top view.

**Table 9. Alternate function input/output (continued)**

| Port name | Digital alternate function number | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | AFIO0 | AFIO1 | AFIO2 | AFIO3 | AFIO4 | AFIO5 | AFOI6 | AFIO7 | AFIO8 | AFIO9 | AFIO11 | AFIO12 | AFIO13 | AFIO14 | AFIO15 |
| | Alternate function | | | | | | | | | | | | | | |
| | SYSTEM | TIM2 | TIM3/4 | TIM9/10/11 | I2C1/2 | SPI1/2 | N/A | USART1/2/3 | N/A | N/A | LCD | N/A | N/A | RI | SYSTEM |
| PB5 | - | - | TIM3_CH2 | - | I2C1_ SMBA | SPI1_MOSI | - | - | - | - | [SEG9] | - | - | - | EVENTOUT |
| PB6 | - | - | TIM4_CH1 | - | I2C1_SCL | - | - | USART1_TX | - | - | - | - | - | - | EVENTOUT |
| PB7 | - | - | TIM4_CH2 | - | I2C1_SDA | - | - | USART1_RX | - | - | - | - | - | - | EVENTOUT |
| PB8 | - | - | TIM4_CH3 | TIM10_CH1* | I2C1_SCL | - | - | - | - | - | SEG16 | - | - | - | EVENTOUT |
| PB9 | - | - | TIM4_CH4 | TIM11_CH1* | I2C1_SDA | - | - | - | - | - | [COM3] | - | - | - | EVENTOUT |
| PB10 | - | TIM2_CH3 | - | - | I2C2_SCL | - | - | USART3_TX | - | - | SEG10 | - | - | - | EVENTOUT |
| PB11 | - | TIM2_CH4 | - | - | I2C2_SDA | - | - | USART3_RX | - | - | SEG11 | - | - | - | EVENTOUT |
| PB12 | - | - | - | TIM10_CH1 | I2C2_ SMBA | SPI2_NSS | - | USART3_CK | - | - | SEG12 | - | - | - | EVENTOUT |
| PB13 | - | - | - | TIM9_CH1 | - | SPI2_SCK | - | USART3_CTS | - | - | SEG13 | - | - | - | EVENTOUT |
| PB14 | - | - | - | TIM9_CH2 | - | SPI2_MISO | - | USART3_RTS | - | - | SEG14 | - | - | - | EVENTOUT |
| PB15 | - | - | - | TIM11_CH1 | - | SPI2_MOSI | - | - | - | - | SEG15 | - | - | - | EVENTOUT |
| PC0 | - | - | - | - | - | - | - | - | - | - | SEG18 | - | - | TIMx_IC1 | EVENTOUT |
| PC1 | - | - | - | - | - | - | - | - | - | - | SEG19 | - | - | TIMx_IC2 | EVENTOUT |
| PC2 | - | - | - | - | - | - | - | - | - | - | SEG20 | - | - | TIMx_IC3 | EVENTOUT |
| PC3 | - | - | - | - | - | - | - | - | - | - | SEG21 | - | - | TIMx_IC4 | EVENTOUT |
| PC4 | - | - | - | - | - | - | - | - | - | - | SEG22 | - | - | TIMx_IC1 | EVENTOUT |
| PC5 | - | - | - | - | - | - | - | - | - | - | SEG23 | - | - | TIMx_IC2 | EVENTOUT |
| PC6 | - | - | TIM3_CH1 | - | - | - | - | - | - | - | SEG24 | - | - | TIMx_IC3 | EVENTOUT |
| PC7 | - | - | TIM3_CH2 | - | - | - | - | - | - | - | SEG25 | - | - | TIMx_IC4 | EVENTOUT |
| PC8 | - | - | TIM3_CH3 | - | - | - | - | - | - | - | SEG26 | - | - | TIMx_IC1 | EVENTOUT |
| PC9 | - | - | TIM3_CH4 | - | - | - | - | - | - | - | SEG27 | - | - | TIMx_IC2 | EVENTOUT |
| PC10 | - | - | - | - | - | - | - | USART3_TX | - | - | COM4 / SEG28 / SEG40 | - | - | TIMx_IC3 | EVENTOUT |

**Table 9. Alternate function input/output (continued)**

| Port name | Digital alternate function number | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | AFIO0 | AFIO1 | AFIO2 | AFIO3 | AFIO4 | AFIO5 | AFOI6 | AFIO7 | AFIO8 | AFIO9 | AFIO11 | AFIO12 | AFIO13 | AFIO14 | AFIO15 |
| | Alternate function | | | | | | | | | | | | | | |
| | SYSTEM | TIM2 | TIM3/4 | TIM9/10/11 | I2C1/2 | SPI1/2 | N/A | USART1/2/3 | N/A | N/A | LCD | N/A | N/A | RI | SYSTEM |
| PH1-OSC_OUT | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| PH2 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |

### 6.3.3 Embedded internal reference voltage

The parameters given in the following table are based on characterization results, unless otherwise specified.

**Table 15. Embedded internal reference voltage calibration values**

| Calibration value name | Description | Memory address |
|---|---|---|
| VREFINT_CAL | Raw data acquired at temperature of 30 °C, $V_{DDA}$= 3 V | 0x1FF8 0078-0x1FF8 0079 |

**Table 16. Embedded internal reference voltage**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{REFINT\ out}$(1) | Internal reference voltage | – 40 °C < $T_J$ < +105 °C | 1.202 | 1.224 | 1.242 | V |
| $I_{REFINT}$ | Internal reference current consumption | - | - | 1.4 | 2.3 | µA |
| $T_{VREFINT}$ | Internal reference startup time | - | - | 2 | 3 | ms |
| $V_{VREF\_MEAS}$ | $V_{DDA}$ and $V_{REF+}$voltage during $V_{REFINT}$ factory measure | - | 2.99 | 3 | 3.01 | V |
| $A_{VREF\_MEAS}$ | Accuracy of factory-measured $V_{REF}$ value (2) | Including uncertainties due to ADC and $V_{DDA}/V_{REF+}$ values | - | - | ±5 | mV |
| $T_{Coeff}$(3) | Temperature coefficient | –40 °C < $T_J$ < +105 °C | - | 25 | 100 | ppm/°C |
| $A_{Coeff}$(3) | Long-term stability | 1000 hours, T= 25 °C | - | - | 1000 | ppm |
| $V_{DDCoeff}$(3) | Voltage coefficient | 3.0 V < $V_{DDA}$ < 3.6 V | - | - | 2000 | ppm/V |
| $T_{S\_vrefint}$(3)(4) | ADC sampling time when reading the internal reference voltage | - | 5 | 10 | - | µs |
| $T_{ADC\_BUF}$(3) | Startup time of reference voltage buffer for ADC | - | - | - | 10 | µs |
| $I_{BUF\_ADC}$(3) | Consumption of reference voltage buffer for ADC | - | - | 13.5 | 25 | µA |
| $I_{VREF\_OUT}$(3) | VREF_OUT output current(5) | - | - | - | 1 | µA |
| $C_{VREF\_OUT}$(3) | VREF_OUT output load | - | - | - | 50 | pF |
| $I_{LPBUF}$(3) | Consumption of reference voltage buffer for VREF_OUT and COMP | - | - | 730 | 1200 | nA |
| $V_{REFINT\_DIV1}$(3) | 1/4 reference voltage | - | 24 | 25 | 26 | % $V_{REFINT}$ |
| $V_{REFINT\_DIV2}$(3) | 1/2 reference voltage | - | 49 | 50 | 51 | |
| $V_{REFINT\_DIV3}$(3) | 3/4 reference voltage | - | 74 | 75 | 76 | |

1. Tested in production.
2. The internal $V_{REF}$ value is individually measured in production and stored in dedicated EEPROM bytes.
3. Guaranteed by characterization results.
4. Shortest sampling time can be determined in the application by multiple iterations.
5. To guarantee less than 1% VREF_OUT deviation.

**Table 20. Current consumption in Low power run mode**

| Symbol | Parameter | Conditions | | | Typ | Max (1) | Unit |
|---|---|---|---|---|---|---|---|
| $I_{DD\ (LP\ Run)}$ | Supply current in Low power run mode | All peripherals OFF, code executed from RAM, Flash switched OFF, $V_{DD}$ from 1.65 V to 3.6 V | MSI clock, 65 kHz $f_{HCLK}$ = 32 kHz | $T_A$ = -40 °C to 25 °C | 9 | 12 | µA |
| | | | | $T_A$ = 85 °C | 17.5 | 24 | |
| | | | | $T_A$ = 105 °C | 31 | 46 | |
| | | | MSI clock, 65 kHz $f_{HCLK}$ = 65 kHz | $T_A$ = -40 °C to 25 °C | 14 | 17 | |
| | | | | $T_A$ = 85 °C | 22 | 29 | |
| | | | | $T_A$ = 105 °C | 35 | 51 | |
| | | | MSI clock, 131 kHz $f_{HCLK}$ = 131 kHz | $T_A$ = -40 °C to 25 °C | 37 | 42 | |
| | | | | $T_A$ = 55 °C | 37 | 42 | |
| | | | | $T_A$ = 85 °C | 37 | 42 | |
| | | | | $T_A$ = 105 °C | 48 | 65 | |
| | | All peripherals OFF, code executed from Flash, $V_{DD}$ from 1.65 V to 3.6 V | MSI clock, 65 kHz $f_{HCLK}$ = 32 kHz | $T_A$ = -40 °C to 25 °C | 24 | 32 | |
| | | | | $T_A$ = 85 °C | 33 | 42 | |
| | | | | $T_A$ = 105 °C | 48 | 64 | |
| | | | MSI clock, 65 kHz $f_{HCLK}$ = 65 kHz | $T_A$ = -40 °C to 25 °C | 31 | 40 | |
| | | | | $T_A$ = 85 °C | 40 | 48 | |
| | | | | $T_A$ = 105 °C | 54 | 70 | |
| | | | MSI clock, 131 kHz $f_{HCLK}$ = 131 kHz | $T_A$ = -40 °C to 25 °C | 48 | 58 | |
| | | | | $T_A$ = 55 °C | 54 | 63 | |
| | | | | $T_A$ = 85 °C | 56 | 65 | |
| | | | | $T_A$ = 105 °C | 70 | 90 | |
| $I_{DD}$ Max (LP Run)(2) | Max allowed current in Low power run mode | $V_{DD}$ from 1.65 V to 3.6 V | - | - | - | 200 | |

1. Guaranteed by characterization results, unless otherwise specified.
2. This limitation is related to the consumption of the CPU core and the peripherals that are powered by the regulator. Consumption of the I/Os is not included in this limitation.

**Table 22. Typical and maximum current consumptions in Stop mode**

| Symbol | Parameter | Conditions | | | Typ (1) | Max (1)(2) | Unit |
|---|---|---|---|---|---|---|---|
| $I_{DD}$ (Stop with RTC) | Supply current in Stop mode with RTC enabled | RTC clocked by LSI, regulator in LP mode, HSI and HSE OFF (no independent watchdog) | LCD OFF | $T_A$ = -40°C to 25°C $V_{DD}$ = 1.8 V | 1.2 | 2.75 | µA |
| | | | | $T_A$ = -40°C to 25°C | 1.4 | 4 | |
| | | | | $T_A$ = 55°C | 2.6 | 6 | |
| | | | | $T_A$= 85°C | 4.8 | 10 | |
| | | | | $T_A$ = 105°C | 10.2 | 23 | |
| | | | LCD ON (static duty)(3) | $T_A$ = -40°C to 25°C | 3.3 | 6 | |
| | | | | $T_A$ = 55°C | 4.5 | 8 | |
| | | | | $T_A$= 85°C | 6.6 | 12 | |
| | | | | $T_A$ = 105°C | 13.6 | 27 | |
| | | | LCD ON (1/8 duty)(4) | $T_A$ = -40°C to 25°C | 7.7 | 10 | |
| | | | | $T_A$ = 55°C | 8.6 | 12 | |
| | | | | $T_A$= 85°C | 10.7 | 16 | |
| | | | | $T_A$ = 105°C | 19.8 | 40 | |
| | | RTC clocked by LSE external clock (32.768 kHz), regulator in LP mode, HSI and HSE OFF (no independent watchdog) | LCD OFF | $T_A$ = -40°C to 25°C | 1.6 | 4 | |
| | | | | $T_A$ = 55°C | 2.7 | 6 | |
| | | | | $T_A$= 85°C | 4.8 | 10 | |
| | | | | $T_A$ = 105°C | 10.3 | 23 | |
| | | | LCD ON (static duty)(3) | $T_A$ = -40°C to 25°C | 3.6 | 6 | |
| | | | | $T_A$ = 55°C | 4.6 | 8 | |
| | | | | $T_A$= 85°C | 6.7 | 12 | |
| | | | | $T_A$ = 105°C | 10.9 | 23 | |
| | | | LCD ON (1/8 duty)(4) | $T_A$ = -40°C to 25°C | 7.6 | 10 | |
| | | | | $T_A$ = 55°C | 8.6 | 12 | |
| | | | | $T_A$= 85°C | 10.7 | 16 | |
| | | | | $T_A$ = 105°C | 19.8 | 40 | |
| | | RTC clocked by LSE (no independent watchdog)(5) | LCD OFF | $T_A$ = -40°C to 25°C $V_{DD}$ = 1.8 V | 1.45 | - | |
| | | | | $T_A$ = -40°C to 25°C $V_{DD}$ = 3.0 V | 1.9 | - | |
| | | | | $T_A$ = -40°C to 25°C $V_{DD}$ = 3.6 V | 2.2 | - | |

### Low-speed external user clock generated from an external source

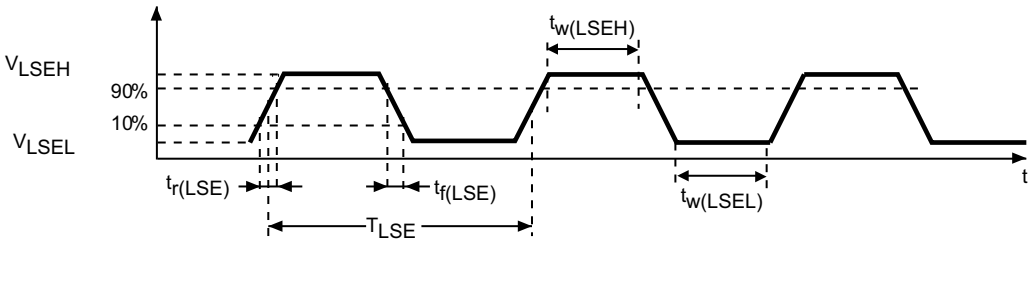
The characteristics given in the following table result from tests performed using a low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 13*.

**Table 27. Low-speed external user clock characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LSE\_ext}$ | User external clock source frequency | - | 1 | 32.768 | 1000 | kHz |
| $V_{LSEH}$ | OSC32_IN input pin high level voltage | | $0.7V_{DD}$ | - | $V_{DD}$ | V |
| $V_{LSEL}$ | OSC32_IN input pin low level voltage | | $V_{SS}$ | - | $0.3V_{DD}$ | |
| $t_{w(LSEH)}$ $t_{w(LSEL)}$ | OSC32_IN high or low time | | 465 | - | - | ns |
| $t_{r(LSE)}$ $t_{f(LSE)}$ | OSC32_IN rise or fall time | | - | - | 10 | |
| $C_{IN(LSE)}$ | OSC32_IN input capacitance | - | - | 0.6 | - | pF |
| $DuCy_{(LSE)}$ | Duty cycle | - | 45 | - | 55 | % |
| $I_L$ | OSC32_IN Input leakage current | $V_{SS} \leq V_{IN} \leq V_{DD}$ | - | - | ±1 | µA |

1. Guaranteed by design.

**Figure 16. Low-speed external clock source AC timing diagram**




### High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 1 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 28*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

**Table 32. MSI oscillator characteristics (continued)**

| Symbol | Parameter | Condition | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{STAB(MSI)}$(2) | MSI oscillator stabilization time | MSI range 0 | - | 40 | µs |
| | | MSI range 1 | - | 20 | |
| | | MSI range 2 | - | 10 | |
| | | MSI range 3 | - | 4 | |
| | | MSI range 4 | - | 2.5 | |
| | | MSI range 5 | - | 2 | |
| | | MSI range 6, Voltage range 1 and 2 | - | 2 | |
| | | MSI range 3, Voltage Range 3 | - | 3 | |
| $f_{OVER(MSI)}$ | MSI oscillator frequency overshoot | Any range to range 5 | - | 4 | MHz |
| | | Any range to range 6 | - | 6 | |

1. This is a deviation for an individual part, once the initial frequency has been measured.
2. Guaranteed by characterization results.

### 6.3.8 PLL characteristics

The parameters given in *Table 33* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 13*.

**Table 33. PLL characteristics**

| Symbol | Parameter | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max(1) | |
| $f_{PLL\_IN}$ | PLL input clock(2) | 2 | - | 24 | MHz |
| | PLL input clock duty cycle | 45 | - | 55 | % |
| $f_{PLL\_OUT}$ | PLL output clock | 2 | - | 32 | MHz |
| $t_{LOCK}$ | Worst case PLL lock time<br>PLL input = 2 MHz<br>PLL VCO = 96 MHz | - | 100 | 130 | µs |
| Jitter | Cycle-to-cycle jitter | - | - | ± 600 | ps |
| $I_{DDA}$(PLL) | Current consumption on $V_{DDA}$ | - | 220 | 450 | µA |
| $I_{DD}$(PLL) | Current consumption on $V_{DD}$ | - | 120 | 150 | |

1. Guaranteed by characterization results.
2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by $f_{PLL\_OUT}$.

### 6.3.9 Memory characteristics

The characteristics are given at $T_A$ = -40 to 105 °C unless otherwise specified.

#### RAM memory

**Table 34. RAM and hardware registers**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| VRM | Data retention mode(1) | STOP mode (or RESET) | 1.65 | - | - | V |

1. Minimum supply voltage without losing data stored in RAM (in Stop mode or under Reset) or in hardware registers (only in Stop mode).

#### Flash memory and data EEPROM

**Table 35. Flash memory and data EEPROM characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Operating voltage Read / Write / Erase | - | 1.65 | - | 3.6 | V |
| $t_{prog}$ | Programming / erasing time for byte / word / double word / half-page | Erasing | - | 3.28 | 3.94 | ms |
| | | Programming | - | 3.28 | 3.94 | |
| $I_{DD}$ | Average current during whole program/erase operation | $T_A$ = 25 °C, $V_{DD}$ = 3.6 V | - | 300 | - | µA |
| | Maximum current (peak) during program/erase operation | | - | 1.5 | 2.5 | mA |

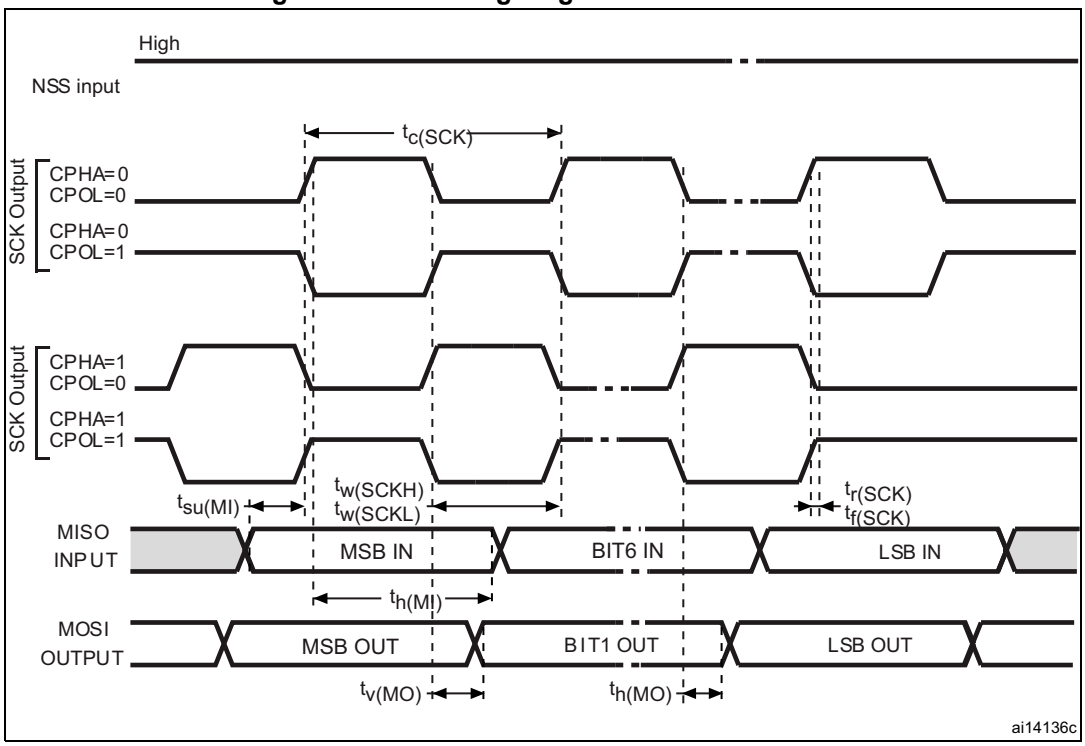
1. Guaranteed by design.

**Table 36. Flash memory, data EEPROM endurance and data retention**

| Symbol | Parameter | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min(1) | Typ | Max | |
| NCYC(2) | Cycling (erase / write) Program memory | $T_A$ = -40°C to 105 °C | 10 | - | - | kcycles |
| | Cycling (erase / write) EEPROM data memory | | 300 | - | - | |
| $t_{RET}$(2) | Data retention (program memory) after 10 kcycles at $T_A$ = 85 °C | TRET = +85 °C | 30 | - | - | years |
| | Data retention (EEPROM data memory) after 300 kcycles at $T_A$ = 85 °C | | 30 | - | - | |
| | Data retention (program memory) after 10 kcycles at $T_A$ = 105 °C | TRET = +105 °C | 10 | - | - | |
| | Data retention (EEPROM data memory) after 300 kcycles at $T_A$ = 105 °C | | 10 | - | - | |

1. Guaranteed by characterization results.
2. Characterization is done according to JEDEC JESD22-A117.

**Figure 24. SPI timing diagram - master mode(1)**




1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

## USB characteristics

The USB interface is USB-IF certified (full speed).

**Table 50. USB startup time**

| Symbol | Parameter | Max | Unit |
|---|---|---|---|
| $t_{STARTUP}$(1) | USB transceiver startup time | 1 | µs |

1. Guaranteed by design.

**Table 51. USB DC electrical characteristics**

| Symbol | Parameter | Conditions | Min.(1) | Max.(1) | Unit |
|---|---|---|---|---|---|
| **Input levels** | | | | | |
| $V_{DD}$ | USB operating voltage(2) | - | 3.0 | 3.6 | V |
| $V_{DI}$(3) | Differential input sensitivity | I(USB_DP, USB_DM) | 0.2 | - | V |
| $V_{CM}$(3) | Differential common mode range | Includes $V_{DI}$ range | 0.8 | 2.5 | |
| $V_{SE}$(3) | Single ended receiver threshold | - | 1.3 | 2.0 | |
| **Output levels** | | | | | |
| $V_{OL}$(4) | Static output level low | $R_L$ of 1.5 kΩ to 3.6 V(5) | - | 0.3 | V |
| $V_{OH}$(4) | Static output level high | $R_L$ of 15 kΩ to $V_{SS}$(5) | 2.8 | 3.6 | |

1. All the voltages are measured from the local ground potential.
2. To be compliant with the USB 2.0 full speed electrical specification, the USB_DP (D+) pin should be pulled up with a 1.5 kΩ resistor to a 3.0-to-3.6 V voltage range.
3. Guaranteed by characterization results.
4. Tested in production.
5. $R_L$ is the load connected on the USB drivers.

**Figure 25. USB timings: definition of data signal rise and fall time**

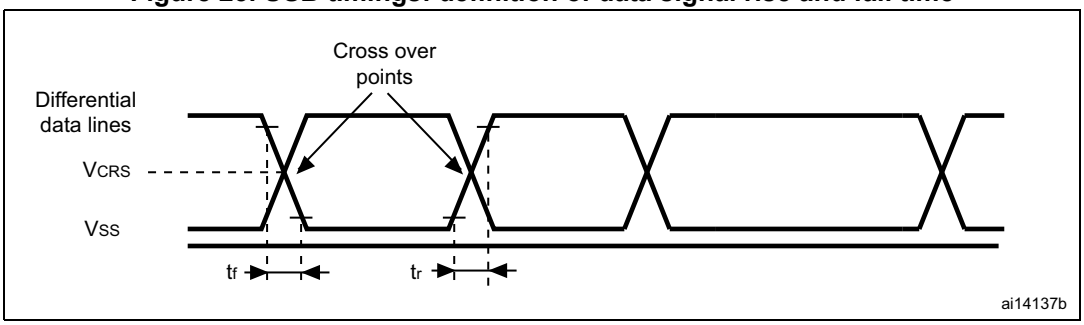



**Table 52. USB: full speed electrical characteristics**

| Driver characteristics(1) | | | | | |
|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Unit** |
| $t_r$ | Rise time(2) | $C_L$ = 50 pF | 4 | 20 | ns |
| $t_f$ | Fall Time(2) | $C_L$ = 50 pF | 4 | 20 | ns |
| $t_{rfm}$ | Rise/ fall time matching | $t_r/t_f$ | 90 | 110 | % |
| $V_{CRS}$ | Output signal crossover voltage | | 1.3 | 2.0 | V |

1. Guaranteed by design.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

**Figure 28. Maximum dynamic current consumption on $V_{REF+}$ supply pin during ADC conversion**

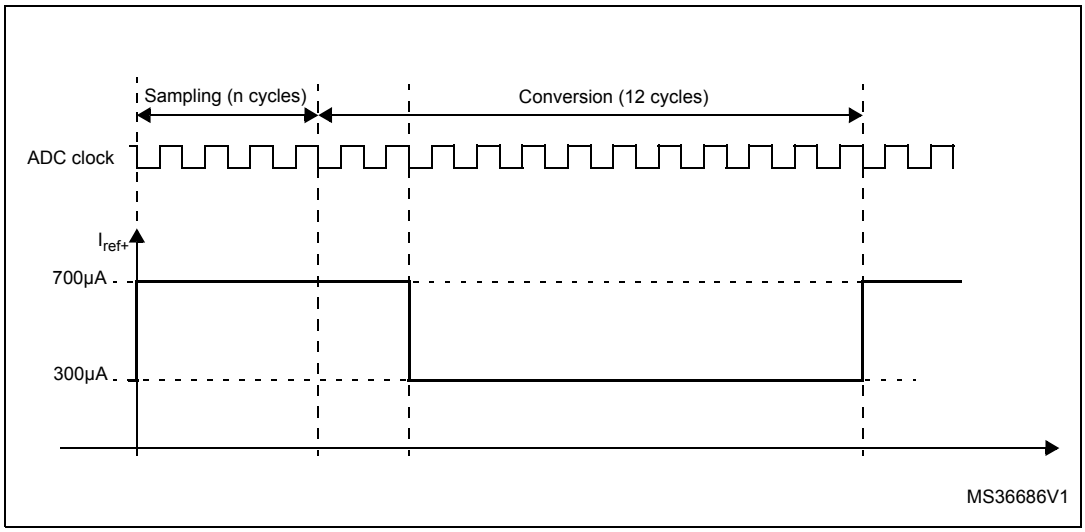



**Table 56. Maximum source impedance $R_{AIN}$ max(1)**

| Ts (µs) | $R_{AIN}$ max (kOhm) | | | | Ts (cycles) $f_{ADC}$= 16 MHz(2) |
|---|---|---|---|---|---|
| | Multiplexed channels | | Direct channels | | |
| | 2.4 V < $V_{DDA}$< 3.6 V | 1.8 V < $V_{DDA}$ < 2.4 V | 2.4 V < $V_{DDA}$< 3.3 V | 1.8 V < $V_{DDA}$ < 2.4 V | |
| 0.25 | Not allowed | Not allowed | 0.7 | Not allowed | 4 |
| 0.5625 | 0.8 | Not allowed | 2.0 | 1.0 | 9 |
| 1 | 2.0 | 0.8 | 4.0 | 3.0 | 16 |
| 1.5 | 3.0 | 1.8 | 6.0 | 4.5 | 24 |
| 3 | 6.8 | 4.0 | 15.0 | 10.0 | 48 |
| 6 | 15.0 | 10.0 | 30.0 | 20.0 | 96 |
| 12 | 32.0 | 25.0 | 50.0 | 40.0 | 192 |
| 24 | 50.0 | 50.0 | 50.0 | 50.0 | 384 |

1. Guaranteed by design.
2. Number of samples calculated for **$f_{ADC}$ = 16 MHz. F**or **$f_{ADC}$ = 8 and 4 MHz the number of sampling cycles can be reduced with respect to the minimum sampling time Ts (us).**

## General PCB design guidelines

Power supply decoupling should be performed as shown in  The 10 nF capacitors should be ceramic (good quality). They should be placed as close as possible to the chip.

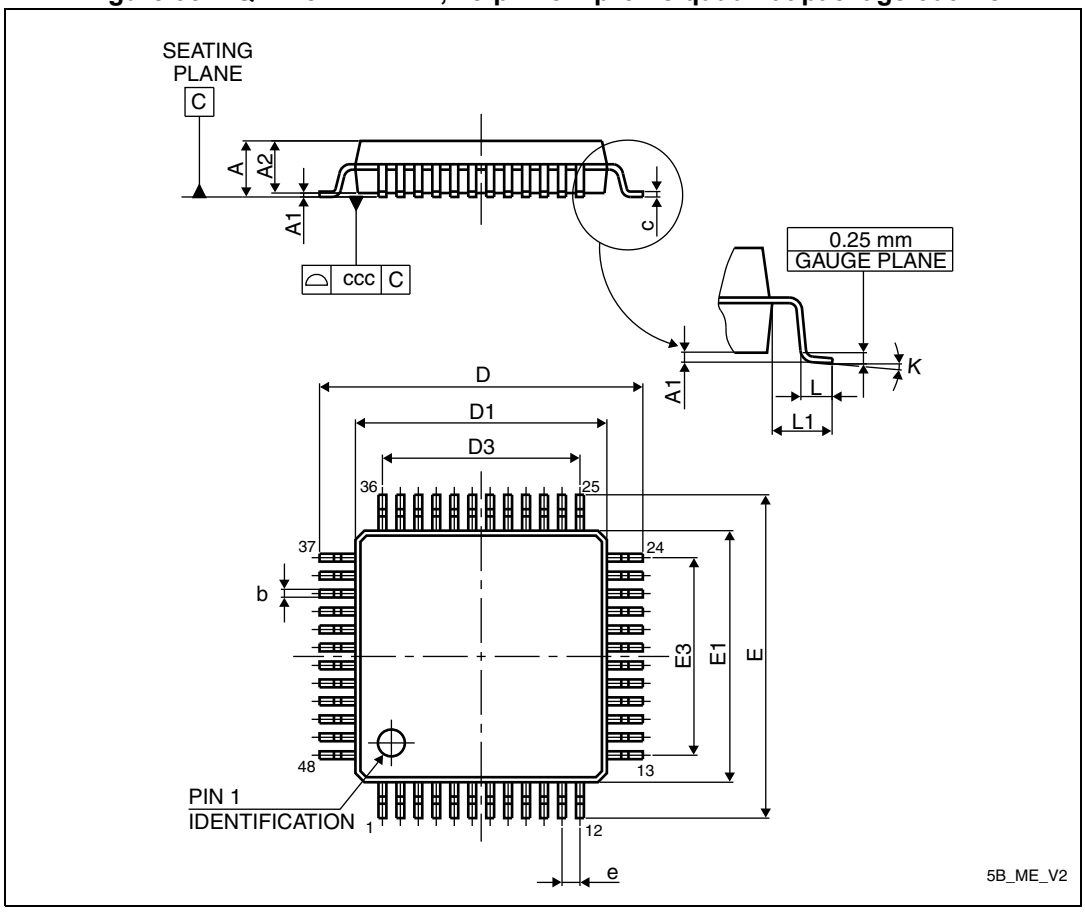
**Table 57. DAC characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| dOffset/dT(1) | Offset error temperature coefficient (code 0x800) | $V_{DDA}$ = 3.3V, $T_A$ = 0 to 50 °C DAC output buffer OFF | -20 | -10 | 0 | µV/°C |
| | | $V_{DDA}$ = 3.3V, $T_A$ = 0 to 50 °C DAC output buffer ON | 0 | 20 | 50 | |
| Gain(1) | Gain error(6) | $C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON | - | +0.1 / -0.2% | +0.2 / -0.5% | % |
| | | No $R_{LOAD}$, $C_L \leq 50$ pF DAC output buffer OFF | - | +0 / -0.2% | +0 / -0.4% | |
| dGain/dT(1) | Gain error temperature coefficient | $V_{DDA}$ = 3.3V, $T_A$ = 0 to 50 °C DAC output buffer OFF | -10 | -2 | 0 | µV/°C |
| | | $V_{DDA}$ = 3.3V, $T_A$ = 0 to 50 °C DAC output buffer ON | -40 | -8 | 0 | |
| TUE(1) | Total unadjusted error | $C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON | - | 12 | 30 | LSB |
| | | No $R_{LOAD}$, $C_L \leq 50$ pF DAC output buffer OFF | - | 8 | 12 | |
| $t_{SETTLING}$ | Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes till DAC_OUT reaches final value ±1LSB | $C_L \leq 50$ pF, $R_L \geq 5$ kΩ | - | 7 | 12 | µs |
| Update rate | Max frequency for a correct DAC_OUT change (95% of final value) with 1 LSB variation in the input code | $C_L \leq 50$ pF, $R_L \geq 5$ kΩ | - | - | 1 | Msps |
| $t_{WAKEUP}$ | Wakeup time from off state (setting the ENx bit in the DAC Control register)(7) | $C_L \leq 50$ pF, $R_L \geq 5$ kΩ | - | 9 | 15 | µs |
| PSRR+ | $V_{DDA}$ supply rejection ratio (static DC measurement) | $C_L \leq 50$ pF, $R_L \geq 5$ kΩ | - | -60 | -35 | dB |

1. Guaranteed by characterization results.
2. Difference between two consecutive codes - 1 LSB.
3. Difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095.
4. Difference between the value measured at Code (0x800) and the ideal value = V/2.
5. Difference between the value measured at Code (0x001) and the ideal value.
6. Difference between ideal slope of the transfer function and measured slope computed from code 0x000 and 0xFFF when buffer is OFF, and from code giving 0.2 V and ($V_{DDA}$ – 0.2) V when buffer is ON.
7. In buffered mode, the output can overshoot above the final value for low input code (starting from min value).

## 7.3 LQFP48 7 x 7 mm, 48-pin low-profile quad flat package information

**Figure 38. LQFP48 7 x 7 mm, 48-pin low-profile quad flat package outline**



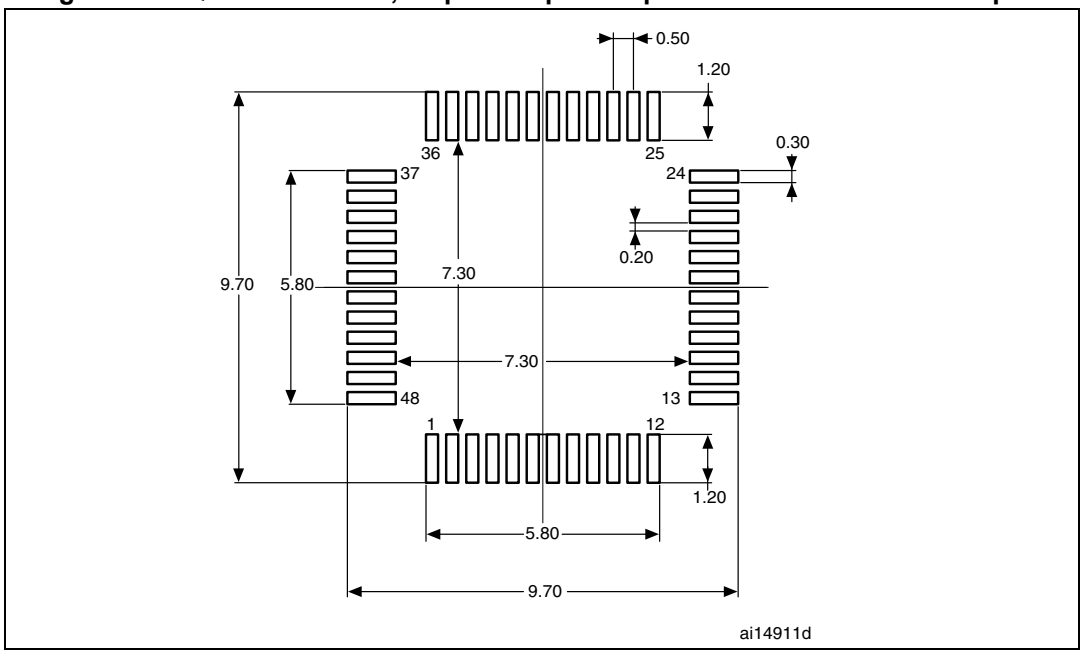

1. Drawing is not to scale.

**Table 65. LQFP48 7 x 7 mm, 48-pin low-profile quad flat package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| D1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| D3 | - | 5.500 | - | - | 0.2165 | - |
| E | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| E1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| E3 | - | 5.500 | - | - | 0.2165 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| k | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 39. LQFP48 7 x 7 mm, 48-pin low-profile quad flat recommended footprint**




1. Dimensions are in millimeters.

# 9 Revision history

Table 73. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 02-Jul-2010 | 1 | Initial release. |
| 01-Oct-2010 | 2 | Removed 5 V tolerance (FT) from PA3, PB0 and PC3 in *Table 8: STM32L15xx6/8/B pin definitions*<br>Updated *Table 14: Embedded reset and power control block characteristics*<br>Updated *Table 16: Embedded internal reference voltage*<br>Added *Table 53: ADC clock frequency*<br>Updated *Table 54: ADC characteristics* |
| 16-Dec-2010 | 3 | Modified consumptions on page 1 and in *Section 3.1: Low power modes*<br>LED_SEG8 removed on PB6.<br>Updated *Section 6: Electrical characteristics*<br>VFQFPN48 replaced by UFQFPN48 |
| 25-Feb-2011 | 4 | *Section 3.3.2: Power supply supervisor*: updated note.<br>*Table 8: STM32L15xx6/8/B pin definitions:* modified main function (after reset) and alternate function for OSC_IN and OSC_OUT pins; modified footnote 5; added footnote to OSC32_IN and OSC32_OUT pins; C1 and D1 removed on PD0 and PD1 pins (TFBGA64 column).<br>*Section 3.11: DAC (digital-to-analog converter)*: updated bullet list.<br>*Table 10: Voltage characteristics on page 52*: updated footnote 3 regarding $I_{INJ(PIN)}$.<br>*Table 11: Current characteristics on page 52*: updated footnote 4 regarding positive and negative injection.<br>*Table 14: Embedded reset and power control block characteristics on page 54*: updated typ and max values for $T_{RSTTEMPO}$ ($V_{DD}$ rising, BOR enabled).<br>*Table 17: Current consumption in Run mode, code with data processing running from Flash on page 58*: removed values for HSI clock source (16 MHz), Range 3.<br>*Table 18: Current consumption in Run mode, code with data processing running from RAM on page 59*: removed values for HSI clock source (16 MHz), Range 3.<br>*Table 19: Current consumption in Sleep mode on page 60* removed values for HSI clock source (16 MHz), Range 3 for both RAM and Flash; changed units.<br>*Table 20: Current consumption in Low power run mode on page 62*: updated parameter and max value of $I_{DD}$ Max (LP Run).<br>*Table 21: Current consumption in Low power sleep mode on page 63*: updated symbol, parameter, and max value of $I_{DD}$ Max (LP Sleep).<br>*Table 22: Typical and maximum current consumptions in Stop mode on page 64* updated values for $I_{DD\ (Stop\ with\ RTC)}$ - RTC clocked by LSE external clock (32.768 kHz), regulator in LP mode, HSI and HSE OFF (no independent watchdog). |

Table 73. Document revision history (continued)

| Date | Revision | Changes |
|---|---|---|
| 17-June-2011 | 5 | Modified 1st page (low power features)<br>Added STM32L15xC6 and STM32L15xR6 devices (32 Kbytes of Flash memory).<br>Modified *Section 3.6: GPIOs (general-purpose inputs/outputs) on page 22*<br>Modified *Section 6.3: Operating conditions on page 53*<br>Modified *Table 55: ADC accuracy on page 95*, *Table 57: DAC characteristics on page 99* and *Table 60: Comparator 1 characteristics on page 102* |
| 25-Jan-2012 | 6 | *Features*: updated internal multispeed low power RC.<br>*Table 2: Ultralow power STM32L15xx6/8/B device features and peripheral counts*: LCD 4x44 and 8x40 available for both 64- and 128-Kbyte devices; two comparators available for all devices.<br>*Table 3: Functionalities depending on the operating power supply range*: added footnote *1*.<br>*Figure 8: STM32L15xCx UFQFPN48 pinout*: replaced VFQPN48 by UFQFPN48 as name of package.<br>*Table 8: STM32L15xx6/8/B pin definitions*: replaced PH0/PH1 by PC14/PC15.<br>*Table 9: Alternate function input/output*: removed EVENT OUT from PH2 port, AFIO15 column.<br>*Table 19: Current consumption in Sleep mode*: updated MSI conditions and $f_{HCLK}$.<br>*Table 20: Current consumption in Low power run mode*: updated some temperature conditions; added footnote *2.*<br>*Table 21: Current consumption in Low power sleep mode*: updated some temperature conditions and one of the MSI clock conditions.<br>*Table 22: Typical and maximum current consumptions in Stop mode*: updated $I_{DD}$ (WU from Stop) parameter.<br>*Table 23: Typical and maximum current consumptions in Standby mode*: updated $I_{DD}$ (WU from Standby) parameter.<br>*Table 25: Low-power mode wakeup timings*: updated $f_{HCLK}$ value for $t_{WUSLEEP\_LP}$; updated typical value of parameter “Wakeup from Stop mode, regulator in Run mode”.<br>*Table 24: Peripheral current consumption*: replaced GPIOF by GPIOH.<br>*Table 33: PLL characteristics*: updated “PLL output clock”<br>*Table 35: Flash memory and data EEPROM characteristics*: updated all information for $I_{DD}$.<br>*Figure 19: I/O AC characteristics definition*: replaced the falling edge “$t_{r(IO)out}$” by “$t_{f(IO)out}$”.<br>*Table 47: I2C characteristics*: amended footnote *2.*<br>*Table 54: ADC characteristics*: updated $f_S$ max value for direct channels, 6-bit sampling rate.<br>*Table 55: ADC accuracy*: Updated the first, third and fourth $f_{ADC}$ test condition.<br>*Table 59: Temperature sensor characteristics*: updated typ, min, and max values of the $T_{S\_temp}$ parameter. |