STMicroelectronics - STM32L152R6T6 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, Cap Sense, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 20x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l152r6t6

2 Description

The ultra-low-power STM32L151x6/8/B and STM32L152x6/8/B devices incorporate the connectivity power of the universal serial bus (USB) with the high-performance ARM® Cortex®-M3 32-bit RISC core operating at 32 MHz frequency (33.3 DMIPS), a memory protection unit (MPU), high-speed embedded memories (Flash memory up to 128 Kbytes and RAM up to 16 Kbytes) and an extensive range of enhanced I/Os and peripherals connected to two APB buses.

All the devices offer a 12-bit ADC, 2 DACs and 2 ultra-low-power comparators, six general-purpose 16-bit timers and two basic timers, which can be used as time bases.

Moreover, the STM32L151x6/8/B and STM32L152x6/8/B devices contain standard and advanced communication interfaces: up to two I^{2}Cs and SPIs, three USARTs and a USB. The STM32L151x6/8/B and STM32L152x6/8/B devices offer up to 20 capacitive sensing channels to simply add touch sensing functionality to any application.

They also include a real-time clock and a set of backup registers that remain powered in Standby mode.

Finally, the integrated LCD controller (except STM32L151x6/8/B devices) has a built-in LCD voltage generator that allows to drive up to 8 multiplexed LCDs with contrast independent of the supply voltage.

The ultra-low-power STM32L151x6/8/B and STM32L152x6/8/B devices operate from a 1.8 to 3.6 V power supply (down to 1.65 V at power down) with BOR and from a 1.65 to 3.6 V power supply without BOR option. It is available in the -40 to +85 °C temperature range, extended to 105°C in low power dissipation state. A comprehensive set of power-saving modes allows the design of low-power applications.

Nested vectored interrupt controller (NVIC)

The ultra-low-power STM32L151x6/8/B and STM32L152x6/8/B devices embed a nested vectored interrupt controller able to handle up to 45 maskable interrupt channels (not including the 16 interrupt lines of Cortex®-M3) and 16 priority levels.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving*, higher-priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.3 Reset and supply management

3.3.1 Power supply schemes

- V_{DD} = 1.65 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 1.65 to 3.6 V: external analog power supplies for ADC, reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 1.8 V when the ADC is used). V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.

3.3.2 Power supply supervisor

The device has an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR) that can be coupled with a brownout reset (BOR) circuitry.

The device exists in two versions:

- The version with BOR activated at power-on operates between 1.8 V and 3.6 V.
- The other version without BOR operates between 1.65 V and 3.6 V.

After the V_{DD} threshold is reached (1.65 V or 1.8 V depending on the BOR which is active or not at power-on), the option byte loading process starts, either to confirm or modify default thresholds, or to disable the BOR permanently: in this case, the V_{DD} min value becomes 1.65 V (whatever the version, BOR active or not, at power-on).

When BOR is active at power-on, it ensures proper operation starting from 1.8 V whatever the power ramp-up phase before it reaches 1.8 V. When BOR is not active at power-up, the power ramp-up should guarantee that 1.65 V is reached on V_{DD} at least 1 ms after it exits the POR area.

3.5 Low power real-time clock and backup registers

The real-time clock (RTC) is an independent BCD timer/counter. Dedicated registers contain the second, minute, hour (12/24 hour), week day, date, month, year, in BCD (binary-coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day of the month are made automatically. The RTC provides a programmable alarm and programmable periodic interrupts with wakeup from Stop and Standby modes.

- The programmable wakeup time ranges from 120 µs to 36 hours
- Stop mode consumption with LSI and Auto-wakeup: 1.2 µA (at 1.8 V) and 1.4 µA (at 3.0 V)
- Stop mode consumption with LSE, calendar and Auto-wakeup: 1.3 µA (at 1.8V), 1.6 µA (at 3.0 V)

The RTC can be calibrated with an external 512 Hz output, and a digital compensation circuit helps reduce drift due to crystal deviation.

There are twenty 32-bit backup registers provided to store 80 bytes of user application data. They are cleared in case of tamper detection.

3.6 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions, and can be individually remapped using dedicated AFIO registers. All GPIOs are high current capable. The alternate function configuration of I/Os can be locked if needed following a specific sequence in order to avoid spurious writing to the I/O registers. The I/O controller is connected to the AHB with a toggling speed of up to 16 MHz.

External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 23 edge detector lines used to generate interrupt/event requests. Each line can be individually configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 83 GPIOs can be connected to the 16 external interrupt lines. The 7 other lines are connected to RTC, PVD, USB or Comparator events.

3.7 Memories

The STM32L151x6/8/B and STM32L152x6/8/B devices have the following features:

- Up to 16 Kbytes of embedded RAM accessed (read/write) at CPU clock speed with 0 wait states. With the enhanced bus matrix, operating the RAM does not lead to any performance penalty during accesses to the system bus (AHB and APB buses).
- The non-volatile memory is divided into three arrays:
  - 32, 64 or 128 Kbytes of embedded Flash program memory
  - 4 Kbytes of data EEPROM
  - Options bytes

  The options bytes are used to write-protect the memory (with 4 Kbytes granularity) and/or readout-protect the whole memory with the following options:
  - Level 0: no readout protection
  - Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
  - Level 2: chip readout protection, debug features (Cortex®-M3 JTAG and serial wire) and boot in RAM selection disabled (JTAG fuse)

  The whole non-volatile memory embeds the error correction code (ECC) feature.

3.8 DMA (direct memory access)

The flexible 7-channel, general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, general-purpose timers and ADC.

3.9 LCD (liquid crystal display)

The LCD drives up to 8 common terminals and 44 segment terminals to drive up to 320 pixels.

- Internal step-up converter to guarantee functionality and contrast control irrespective of V_{DD}. This converter can be deactivated, in which case the V_{LCD} pin is used to provide the voltage to the LCD
- Supports static, 1/2, 1/3, 1/4 and 1/8 duty
- Supports static, 1/2, 1/3 and 1/4 bias
- Phase inversion to reduce power consumption and EMI
- Up to 8 pixels can be programmed to blink
- Unneeded segments and common pins can be used as general I/O pins
- LCD RAM can be updated at any time owing to a double-buffer
- The LCD controller can operate in Stop mode

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channels' independent or simultaneous conversions
- DMA capability for each channel (including the underrun interrupt)
- external triggers for conversion
- input reference voltage V_{REF+}

Eight DAC trigger inputs are used in the STM32L151x6/8/B and STM32L152x6/8/B devices. The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

3.12 Ultra-low-power comparators and reference voltage

The STM32L151x6/8/B and STM32L152x6/8/B devices embed two comparators sharing the same current bias and reference voltage. The reference voltage can be internal or external (coming from an I/O).

- one comparator with fixed threshold
- one comparator with rail-to-rail inputs, fast or slow mode. The threshold can be one of the following:
  - DAC output
  - External I/O
  - Internal reference voltage (V_{REFINT}) or V_{REFINT} submultiple (1/4, 1/2, 3/4)

Both comparators can wake up from Stop mode, and be combined into a window comparator.

The internal reference voltage is available externally via a low power / low current output buffer (driving current capability of 1 µA typical).

3.13 Routing interface

This interface controls the internal routing of I/Os to TIM2, TIM3, TIM4 and to the comparator and reference voltage output.

3.14 Touch sensing

The STM32L151x6/8/B and STM32L152x6/8/B devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 20 capacitive sensing channels distributed over 10 analog I/O groups. Only software capacitive sensing acquisition mode is supported.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (glass, plastic, ...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven

Table 8. STM32L151x6/8/B and STM32L152x6/8/B pin definitions (continued)

Pins					Pin name	Pin type(1)	I/O structure	Main function(2) (after reset)	Pins functions	
LQFP100	LQFP64	TFBGA64	UFBGA100	LQFP48 or UFQFPN48					Alternate functions	Additional functions
71	45	B8	A12	33	PA12	I/O	FT	PA12	USART1_RTS/ SPI1_MOSI	USB_DP
72	46	A8	A11	34	PA13	I/O	FT	JTMS-SWDIO	JTMS-SWDIO	-
73	-	-	C11	-	PH2	I/O	FT	PH2	-	-
74	47	D5	F11	35	V_{SS_2}	S	-	V_{SS_2}	-	-
75	48	E5	G11	36	V_{DD_2}	S	-	V_{DD_2}	-	-
76	49	A7	A10	37	PA14	I/O	FT	JTCK -SWCLK	JTCK-SWCLK	-
77	50	A6	A9	38	PA15	I/O	FT	JTDI	TIM2_CH1_ETR/PA15/ SPI1_NSS/ LCD_SEG17	-
78	51	B7	B11	-	PC10	I/O	FT	PC10	USART3_TX/LCD_SEG28 /LCD_SEG40/LCD_COM4	-
79	52	B6	C10	-	PC11	I/O	FT	PC11	USART3_RX/LCD_SEG29 /LCD_SEG41/LCD_COM5	-
80	53	C5	B10	-	PC12	I/O	FT	PC12	USART3_CK/LCD_SEG30 /LCD_SEG42/LCD_COM6	-
81	-	-	C9	-	PD0	I/O	FT	PD0	SPI2_NSS/TIM9_CH1	-
82	-	-	B9	-	PD1	I/O	FT	PD1	SPI2_SCK	-
83	54	B5	C8	-	PD2	I/O	FT	PD2	TIM3_ETR/LCD_SEG31/ LCD_SEG43/LCD_COM7	-
84	-	-	B8	-	PD3	I/O	FT	PD3	USART2_CTS/ SPI2_MISO	-
85	-	-	B7	-	PD4	I/O	FT	PD4	USART2_RTS/ SPI2_MOSI	-
86	-	-	A6	-	PD5	I/O	FT	PD5	USART2_TX	-
87	-	-	B6	-	PD6	I/O	FT	PD6	USART2_RX	-
88	-	-	A5	-	PD7	I/O	FT	PD7	USART2_CK/TIM9_CH2	-
89	55	A5	A8	39	PB3	I/O	FT	JTDO	TIM2_CH2/PB3/ SPI1_SCK/LCD_SEG7/ JTDO	COMP2_INM

Table 8. STM32L151x6/8/B and STM32L152x6/8/B pin definitions (continued)

Pins					Pin name	Pin type(1)	I/O structure	Main function(2) (after reset)	Pins functions	
LQFP100	LQFP64	TFBGA64	UFBGA100	LQFP48 or UFQFPN48					Alternate functions	Additional functions
90	56	A4	A7	40	PB4	I/O	FT	NJTRST	TIM3_CH1/PB4/ SPI1_MISO/LCD_SEG8/ NJTRST	COMP2_INP
91	57	C4	C5	41	PB5	I/O	FT	PB5	I2C1_SMBA/TIM3_CH2/ SPI1_MOSI/LCD_SEG9	COMP2_INP
92	58	D3	B5	42	PB6	I/O	FT	PB6	I2C1_SCL/TIM4_CH1/ USART1_TX	
93	59	C3	B4	43	PB7	I/O	FT	PB7	I2C1_SDA/TIM4_CH2/ USART1_RX	PVD_IN
94	60	B4	A4	44	BOOT0	I	B	BOOT0	-	-
95	61	B3	A3	45	PB8	I/O	FT	PB8	TIM4_CH3/I2C1_SCL/ LCD_SEG16/TIM10_CH1	-
96	62	A3	B3	46	PB9	I/O	FT	PB9	TIM4_CH4/I2C1_SDA/ LCD_COM3/TIM11_CH1	-
97	-	-	C3	-	PE0	I/O	FT	PE0	TIM4_ETR/LCD_SEG36/ TIM10_CH1	-
98	-	-	A2	-	PE1	I/O	FT	PE1	LCD_SEG37/TIM11_CH1	-
99	63	D4	D3	47	V_{SS_3}	S	-	V_{SS_3}	-	-
100	64	E4	C4	48	V_{DD_3}	S	-	V_{DD_3}	-	-

1. I = input, O = output, S = supply.
2. Function availability depends on the chosen device. For devices having reduced peripheral counts, it is always the lower number of peripheral that is included. For example, if a device has only one SPI and two USARTs, they will be called SPI1 and USART1 & USART2, respectively. Refer to *Table 2 on page 11*.
3. Applicable to STM32L152xx devices only. In STM32L151xx devices, this pin should be connected to V_{DD}.
4. The PC14 and PC15 I/Os are only configured as OSC32_IN/OSC32_OUT when the LSE oscillator is on (by setting the LSEON bit in the RCC_CSR register). The LSE oscillator pins OSC32_IN/OSC32_OUT can be used as general-purpose PC14/PC15 I/Os, respectively, when the LSE oscillator is off (after reset, the LSE oscillator is off). The LSE has priority over the GPIO function. For more details, refer to Using the OSC32_IN/OSC32_OUT pins as GPIO PC14/PC15 port pins section in the STM32L1xxxx reference manual (RM0038).
5. The PH0 and PH1 I/Os are only configured as OSC_IN/OSC_OUT when the HSE oscillator is on (by setting the HSEON bit in the RCC_CR register). The HSE oscillator pins OSC_IN/OSC_OUT can be used as general-purpose PH0/PH1 I/Os, respectively, when the HSE oscillator is off (after reset, the HSE oscillator is off). The HSE has priority over the GPIO function.
6. Unlike in the LQFP64 package, there is no PC3 in the TFBGA64 package. The V_{REF+} functionality is provided instead.

Table 9. Alternate function input/output

Port name	Digital alternate function number														
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFOI6	AFIO7	AFIO8	AFIO9	AFIO11	AFIO12	AFIO13	AFIO14	AFIO15
	Alternate function														
	SYSTEM	TIM2	TIM3/4	TIM9/10/11	I2C1/2	SPI1/2	N/A	USART1/2/3	N/A	N/A	LCD	N/A	N/A	RI	SYSTEM
BOOT0	BOOT0	-	-	-	-	-	-	-	-	-	-	-	-	-	-
NRST	NRST	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PA0-WKUP1	-	TIM2_CH1_ETR	-	-	-	-	-	USART2_CTS	-	-	-	-	-	TIMx_IC1	EVENTOUT
PA1	-	TIM2_CH2	-	-	-	-	-	USART2_RTS	-	-	[SEG0]	-	-	TIMx_IC2	EVENTOUT
PA2	-	TIM2_CH3	-	TIM9_CH1	-	-	-	USART2_TX	-	-	[SEG1]	-	-	TIMx_IC3	EVENTOUT
PA3	-	TIM2_CH4	-	TIM9_CH2	-	-	-	USART2_RX	-	-	[SEG2]	-	-	TIMx_IC4	EVENTOUT
PA4	-	-	-	-	-	SPI1_NSS	-	USART2_CK	-	-	-	-	-	TIMx_IC1	EVENTOUT
PA5	-	TIM2_CH1_ETR	-	-	-	SPI1_SCK	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PA6	-	-	TIM3_CH1	TIM10_CH1	-	SPI1_MISO	-	-	-	-	[SEG3]	-	-	TIMx_IC3	EVENTOUT
PA7	-	-	TIM3_CH2	TIM11_CH1	-	SPI1_MOSI	-	-	-	-	[SEG4]	-	-	TIMx_IC4	EVENTOUT
PA8	MCO	-	-	-	-	-	-	USART1_CK	-	-	[COM0]	-	-	TIMx_IC1	EVENTOUT
PA9	-	-	-	-	-	-	-	USART1_TX	-	-	[COM1]	-	-	TIMx_IC2	EVENTOUT
PA10	-	-	-	-	-	-	-	USART1_RX	-	-	[COM2]	-	-	TIMx_IC3	EVENTOUT
PA11	-	-	-	-	-	SPI1_MISO	-	USART1_CTS	-	-	-	-	-	TIMx_IC4	EVENTOUT
PA12	-	-	-	-	-	SPI1_MOSI	-	USART1_RTS	-	-	-	-	-	TIMx_IC1	EVENTOUT
PA13	JTMS-SWDIO	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PA14	JTCK-SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC3	EVENTOUT
PA15	JTDI	TIM2_CH1_ETR	-	-	-	SPI1_NSS	-	-	-	-	SEG17	-	-	TIMx_IC4	EVENTOUT
PB0	-	-	TIM3_CH3	-	-	-	-	-	-	-	[SEG5]	-	-	-	EVENTOUT
PB1	-	-	TIM3_CH4	-	-	-	-	-	-	-	[SEG6]	-	-	-	EVENTOUT
PB2	BOOT1	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
PB3	JTDO	TIM2_CH2	-	-	-	SPI1_SCK	-	-	-	-	[SEG7]	-	-	-	EVENTOUT
PB4	NJTRST	-	TIM3_CH1	-	-	SPI1_MISO	-	-	-	-	[SEG8]	-	-	-	EVENTOUT

6.3.3 Embedded internal reference voltage

The parameters given in the following table are based on characterization results, unless otherwise specified.

Table 15. Embedded internal reference voltage calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at temperature of 30 °C, V_{DDA}= 3 V	0x1FF8 0078-0x1FF8 0079

Table 16. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{REFINT\ out}$[1]	Internal reference voltage	– 40 °C < T_J < +105 °C	1.202	1.224	1.242	V
I_{REFINT}	Internal reference current consumption	-	-	1.4	2.3	µA
$T_{VREFINT}$	Internal reference startup time	-	-	2	3	ms
V_{VREF_MEAS}	V_{DDA} and V_{REF+}voltage during V_{REFINT} factory measure	-	2.99	3	3.01	V
A_{VREF_MEAS}	Accuracy of factory-measured V_{REF} value [2]	Including uncertainties due to ADC and V_{DDA}/V_{REF+} values	-	-	±5	mV
T_{Coeff}[3]	Temperature coefficient	–40 °C < T_J < +105 °C	-	25	100	ppm/°C
A_{Coeff}[3]	Long-term stability	1000 hours, T= 25 °C	-	-	1000	ppm
$V_{DDCoeff}$[3]	Voltage coefficient	3.0 V < V_{DDA} < 3.6 V	-	-	2000	ppm/V
$T_{S\_vrefint}$[3][4]	ADC sampling time when reading the internal reference voltage	-	5	10	-	µs
T_{ADC_BUF}[3]	Startup time of reference voltage buffer for ADC	-	-	-	10	µs
I_{BUF_ADC}[3]	Consumption of reference voltage buffer for ADC	-	-	13.5	25	µA
I_{VREF_OUT}[3]	VREF_OUT output current[5]	-	-	-	1	µA
C_{VREF_OUT}[3]	VREF_OUT output load	-	-	-	50	pF
I_{LPBUF}[3]	Consumption of reference voltage buffer for VREF_OUT and COMP	-	-	730	1200	nA
V_{REFINT_DIV1}[3]	1/4 reference voltage	-	24	25	26	% V_{REFINT}
V_{REFINT_DIV2}[3]	1/2 reference voltage	-	49	50	51	
V_{REFINT_DIV3}[3]	3/4 reference voltage	-	74	75	76	

1. Tested in production.
2. The internal V_{REF} value is individually measured in production and stored in dedicated EEPROM bytes.
3. Guaranteed by characterization results.
4. Shortest sampling time can be determined in the application by multiple iterations.
5. To guarantee less than 1% VREF_OUT deviation.

Table 19. Current consumption in Sleep mode

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max(1)			Unit
						55 °C	85 °C	105 °C	
I_{DD} (Sleep)	Supply current in Sleep mode, code executed from RAM, Flash switched OFF	$f_{HSE} = f_{HCLK}$ up to 16 MHz included, $f_{HSE} = f_{HCLK}/2$ above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	1 MHz	80	140	140	140	µA
				2 MHz	150	210	210	210	
				4 MHz	280	330	330	330(3)	
			Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	4 MHz	280	400	400	400	
				8 MHz	450	550	550	550	
				16 MHz	900	1050	1050	1050	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	8 MHz	550	650	650	650	
				16 MHz	1050	1200	1200	1200	
				32 MHz	2300	2500	2500	2500	
		HSI clock source (16 MHz)	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	16 MHz	1000	1100	1100	1100	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	32 MHz	2300	2500	2500	2500	
		MSI clock, 65 kHz	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	65 kHz	30	50	50	60	
		MSI clock, 524 kHz		524 kHz	50	70	70	80	
		MSI clock, 4.2 MHz		4.2 MHz	200	240	240	250	
	Supply current in Sleep mode, code executed from Flash	$f_{HSE} = f_{HCLK}$ up to 16 MHz included, $f_{HSE} = f_{HCLK}/2$ above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	1 MHz	80	140	140	140	µA
				2 MHz	150	210	210	210	
				4 MHz	290	350	350	350	
			Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	4 MHz	300	400	400	400	
				8 MHz	500	600	600	600	
				16 MHz	1000	1100	1100	1100	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	8 MHz	550	650	650	650	
				16 MHz	1050	1200	1200	1200	
				32 MHz	2300	2500	2500	2500	
		HSI clock source (16 MHz)	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	16 MHz	1000	1100	1100	1100	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	32 MHz	2300	2500	2500	2500	

Table 20. Current consumption in Low power run mode

Symbol	Parameter	Conditions			Typ	Max (1)	Unit
$I_{DD\ (LP\ Run)}$	Supply current in Low power run mode	All peripherals OFF, code executed from RAM, Flash switched OFF, V_{DD} from 1.65 V to 3.6 V	MSI clock, 65 kHz f_{HCLK} = 32 kHz	T_A = -40 °C to 25 °C	9	12	µA
				T_A = 85 °C	17.5	24	
				T_A = 105 °C	31	46	
			MSI clock, 65 kHz f_{HCLK} = 65 kHz	T_A = -40 °C to 25 °C	14	17	
				T_A = 85 °C	22	29	
				T_A = 105 °C	35	51	
			MSI clock, 131 kHz f_{HCLK} = 131 kHz	T_A = -40 °C to 25 °C	37	42	
				T_A = 55 °C	37	42	
				T_A = 85 °C	37	42	
				T_A = 105 °C	48	65	
		All peripherals OFF, code executed from Flash, V_{DD} from 1.65 V to 3.6 V	MSI clock, 65 kHz f_{HCLK} = 32 kHz	T_A = -40 °C to 25 °C	24	32	
				T_A = 85 °C	33	42	
				T_A = 105 °C	48	64	
			MSI clock, 65 kHz f_{HCLK} = 65 kHz	T_A = -40 °C to 25 °C	31	40	
				T_A = 85 °C	40	48	
				T_A = 105 °C	54	70	
			MSI clock, 131 kHz f_{HCLK} = 131 kHz	T_A = -40 °C to 25 °C	48	58	
				T_A = 55 °C	54	63	
				T_A = 85 °C	56	65	
				T_A = 105 °C	70	90	
I_{DD} Max (LP Run)(2)	Max allowed current in Low power run mode	V_{DD} from 1.65 V to 3.6 V	-	-	-	200	

1. Guaranteed by characterization results, unless otherwise specified.
2. This limitation is related to the consumption of the CPU core and the peripherals that are powered by the regulator. Consumption of the I/Os is not included in this limitation.

Table 22. Typical and maximum current consumptions in Stop mode (continued)

Symbol	Parameter	Conditions		Typ (1)	Max (1)(2)	Unit
$I_{DD\ (Stop)}$	Supply current in Stop mode (RTC disabled)	Regulator in LP mode, HSI and HSE OFF, independent watchdog and LSI enabled	T_A = -40°C to 25°C	1.1	2.2	µA
		Regulator in LP mode, LSI, HSI and HSE OFF (no independent watchdog)	T_A = -40°C to 25°C	0.5	0.9	
			T_A = 55°C	1.9	5	
			T_A= 85°C	3.7	8	
			T_A = 105°C	8.9	20(6)	
$I_{DD\ (WU\ from\ Stop)}$	RMS (root mean square) supply current during wakeup time when exiting from Stop mode	MSI = 4.2 MHz	V_{DD} = 3.0 V T_A = -40°C to 25°C	2	-	mA
		MSI = 1.05 MHz		1.45	-	
		MSI = 65 kHz(7)		1.45	-	

1. The typical values are given for V_{DD} = 3.0 V and max values are given for V_{DD} = 3.6 V, unless otherwise specified.
2. Guaranteed by characterization results, unless otherwise specified
3. LCD enabled with external VLCD, static duty, division ratio = 256, all pixels active, no LCD connected
4. LCD enabled with external VLCD, 1/8 duty, 1/3 bias, division ratio = 64, all pixels active, no LCD connected.
5. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8pF loading capacitors.
6. Tested in production
7. When MSI = 64 kHz, the RMS current is measured over the first 15 µs following the wakeup event. For the remaining time of the wakeup period, the current is similar to the Run mode current.

Table 23. Typical and maximum current consumptions in Standby mode

Symbol	Parameter	Conditions		Typ(1)	Max (1)(2)	Unit
I_{DD} (Standby with RTC)	Supply current in Standby mode with RTC enabled	RTC clocked by LSI (no independent watchdog)	T_A = -40 °C to 25 °C V_{DD} = 1.8 V	0.9	-	µA
			T_A = -40 °C to 25 °C	1.1	1.8	
			T_A = 55 °C	1.42	2.5	
			T_A= 85 °C	1.87	3	
			T_A = 105 °C	2.78	5	
		RTC clocked by LSE (no independent watchdog)(3)	T_A = -40 °C to 25 °C V_{DD} = 1.8 V	1	-	
			T_A = -40 °C to 25 °C	1.33	2.9	
			T_A = 55 °C	1.59	3.4	
			T_A= 85 °C	2.01	4.3	
			T_A = 105 °C	3.27	6.3	
I_{DD} (Standby)	Supply current in Standby mode with RTC disabled	Independent watchdog and LSI enabled	T_A = -40 °C to 25 °C	1.1	1.6	
		Independent watchdog and LSI OFF	T_A = -40 °C to 25 °C	0.3	0.55	
			T_A = 55 °C	0.5	0.8	
			T_A = 85 °C	1	1.7	
			T_A = 105 °C	2.5	4(4)	
I_{DD} (WU from Standby)	RMS supply current during wakeup time when exiting from Standby mode	-	V_{DD} = 3.0 V T_A = -40 °C to 25 °C	1	-	

1. The typical values are given for V_{DD} = 3.0 V and max values are given for V_{DD} = 3.6 V, unless otherwise specified.
2. Guaranteed by characterization results, unless otherwise specified.
3. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8pF loading capacitors.
4. Tested in production.

On-chip peripheral current consumption

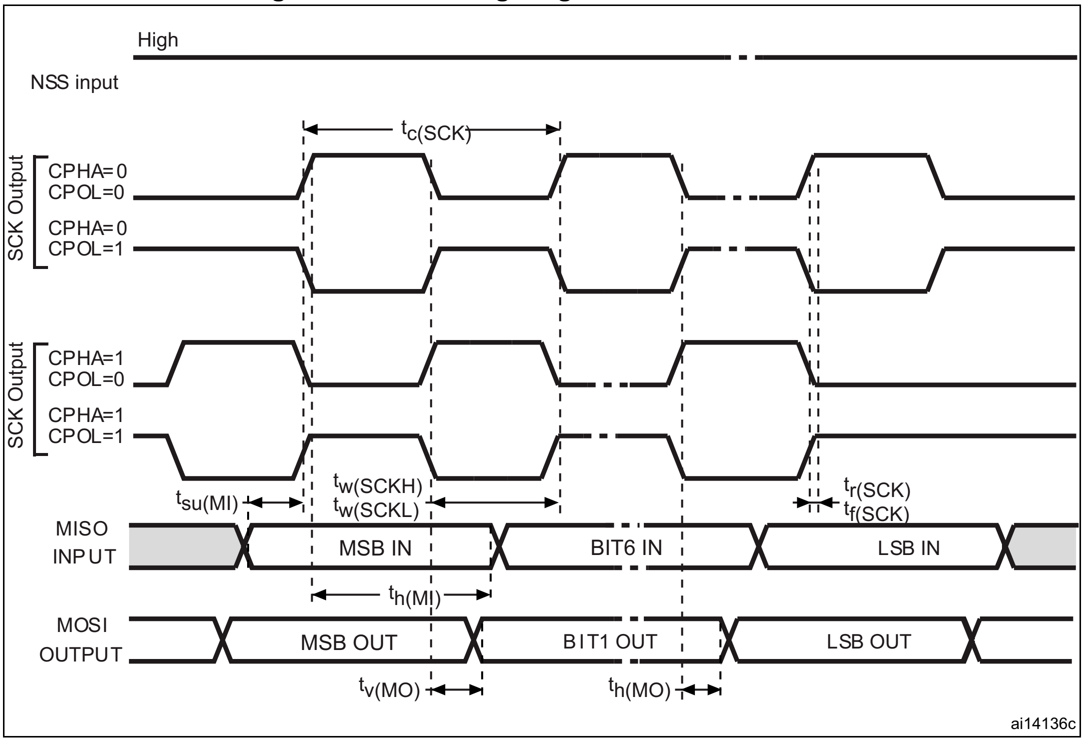
The current consumption of the on-chip peripherals is given in the following table. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on

Table 24. Peripheral current consumption[(1)]

Peripheral		Typical consumption, V_{DD} = 3.0 V, T_A = 25 °C				Unit
		Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	Low power sleep and run	
APB1	TIM2	13	10.5	8	10.5	µA/MHz (f_{HCLK})
	TIM3	14	12	9	12	
	TIM4	12.5	10.5	8	11	
	TIM6	5.5	4.5	3.5	4.5	
	TIM7	5.5	5	3.5	4.5	
	LCD	5.5	5	3.5	5	
	WWDG	4	3.5	2.5	3.5	
	SPI2	5.5	5	4	5	
	USART2	9	8	5.5	8.5	
	USART3	10.5	9	6	8	
	I2C1	8.5	7	5.5	7.5	
	I2C2	8.5	7	5.5	6.5	
	USB	12.5	10	6.5	10	
	PWR	4.5	4	3	3.5	
	DAC	9	7.5	6	7	
	COMP	4.5	4	3.5	4.5	
APB2	SYSCFG & RI	3	2.5	2	2.5	µA/MHz (f_{HCLK})
	TIM9	9	7.5	6	7	
	TIM10	6.5	5.5	4.5	5.5	
	TIM11	7	6	4.5	5.5	
	ADC[(2)]	11.5	9.5	8	9	
	SPI1	5	4.5	3	4	
	USART1	9	7.5	6	7.5	

Figure 24. SPI timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

USB characteristics

The USB interface is USB-IF certified (full speed).

Table 50. USB startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB transceiver startup time	1	µs

1. Guaranteed by design.

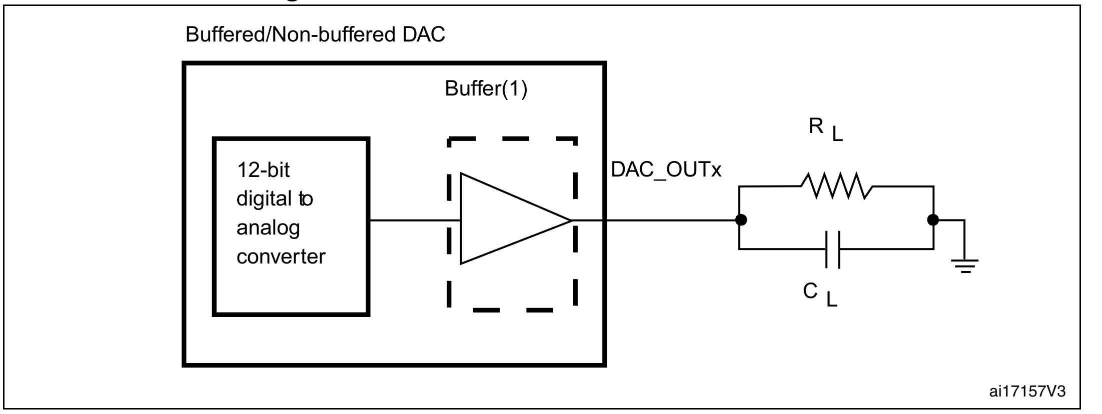
6.3.18 DAC electrical specifications

Data guaranteed by design, unless otherwise specified.

Table 57. DAC characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		1.8	-	3.6	V
V_{REF+}	Reference supply voltage	V_{REF+} must always be below V_{DDA}		1.8	-	3.6	V
V_{REF-}	Lower reference voltage	-		V_{SSA}			V
$I_{DDVREF+}$(1)	Current consumption on V_{REF+} supply V_{REF+} = 3.3 V	No load, middle code (0x800)		-	130	220	µA
		No load, worst code (0x000)		-	220	350	µA
I_{DDA}(1)	Current consumption on V_{DDA} supply V_{DDA} = 3.3 V	No load, middle code (0x800)		-	210	320	µA
		No load, worst code (0xF1C)		-	320	520	µA
R_L	Resistive load	DAC output buffer ON	Connected to V_{SSA}	5	-	-	kΩ
			Connected to V_{DDA}	25	-	-	
C_L	Capacitive load	DAC output buffer ON		-	-	50	pF
R_O	Output impedance	DAC output buffer OFF		12	16	20	kΩ
V_{DAC_OUT}	Voltage on DAC_OUT output	DAC output buffer ON		0.2	-	V_{DDA} – 0.2	V
		DAC output buffer OFF		0.5	-	V_{REF+} – 1LSB	mV
DNL(1)	Differential non linearity(2)	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON		-	1.5	3	LSB
		No R_{LOAD}, $C_L \leq 50$ pF DAC output buffer OFF		-	1.5	3	
INL(1)	Integral non linearity(3)	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON		-	2	4	
		No R_{LOAD}, $C_L \leq 50$ pF DAC output buffer OFF		-	2	4	
Offset(1)	Offset error at code 0x800 (4)	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON		-	±10	±25	
		No R_{LOAD}, $C_L \leq 50$ pF DAC output buffer OFF		-	±5	±8	
Offset1(1)	Offset error at code 0x001(5)	No R_{LOAD}, $C_L \leq 50$ pF DAC output buffer OFF		-	±1.5	±5	

Figure 31. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

6.3.19 Temperature sensor characteristics

Table 58. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}= 3 V	0x1FF8 007A-0x1FF8 007B
TS_CAL2	TS ADC raw data acquired at temperature of 110 °C V_{DDA}= 3 V	0x1FF8 007E-0x1FF8 007F

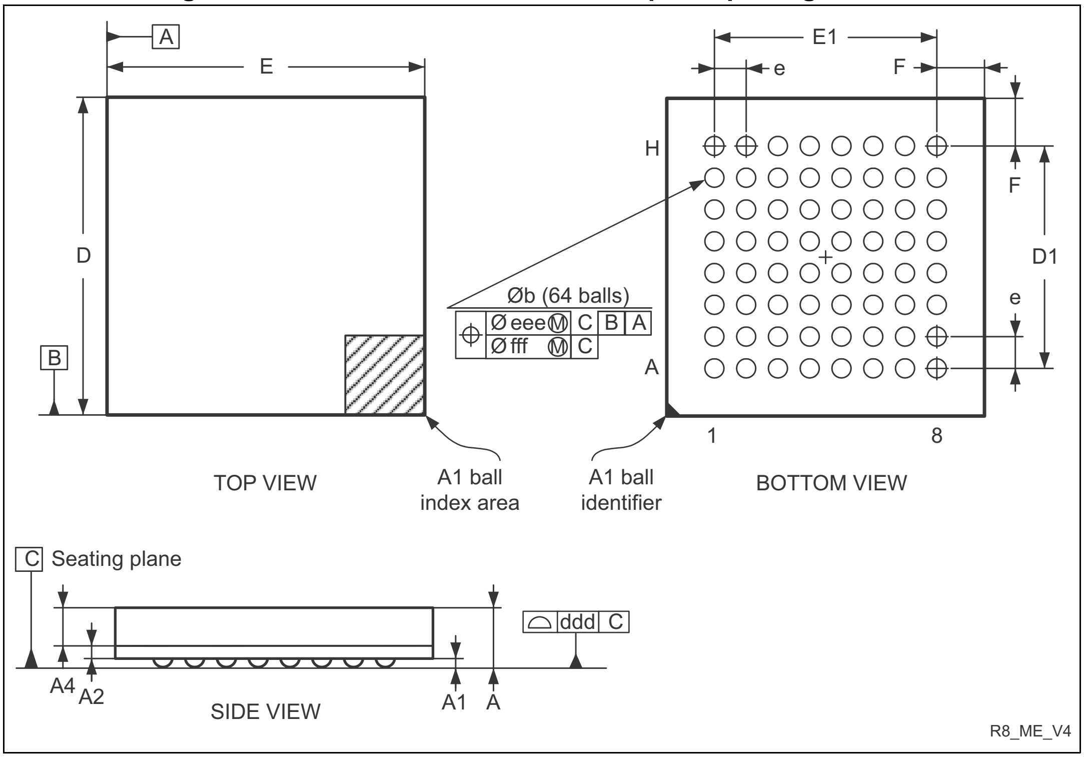
Table 59. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	1.48	1.61	1.75	mV/°C
V_{110}	Voltage at 110°C ±5°C(2)	612	626.8	641.5	mV
$I_{DDA(TEMP)}$(3)	Current consumption	-	3.4	6	µA
t_{START}(3)	Startup time	-	-	10	µs
T_{S_temp}(4)(3)	ADC sampling time when reading the temperature	10	-	-	

1. Guaranteed by characterization results.
2. Measured at V_{DD} = 3 V ±10 mV. V110 ADC conversion result is stored in the TS_CAL2 byte.
3. Guaranteed by design.
4. Shortest sampling time can be determined in the application by multiple iterations.

7.6 TFBGA64 5 x 5 mm, 0.5 mm pitch, thin fine-pitch ball grid array package information

Figure 47. TFBGA64 5 x 5 mm, 0.5 mm pitch, package outline



1. Drawing is not to scale.

Table 69. TFBGA64 5 x 5 mm, 0.5 mm pitch, package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.200	-	-	0.0472
A1	0.150	-	-	0.0059	-	-
A2	-	0.200	-	-	0.0079	-
A4	-	-	0.600	-	-	0.0236
b	0.250	0.300	0.350	0.0098	0.0118	0.0138
D	4.850	5.000	5.150	0.1909	0.1969	0.2028
D1	-	3.500	-	-	0.1378	-
E	4.850	5.000	5.150	0.1909	0.1969	0.2028
E1	-	3.500	-	-	0.1378	-
e	-	0.500	-	-	0.0197	-
F	-	0.750	-	-	0.0295	-
ddd	-	-	0.080	-	-	0.0031