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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Cap Sense, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 20x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l152r8t6tr

List of tables

2 Description

The ultra-low-power STM32L151x6/8/B and STM32L152x6/8/B devices incorporate the connectivity power of the universal serial bus (USB) with the high-performance ARM® Cortex®-M3 32-bit RISC core operating at 32 MHz frequency (33.3 DMIPS), a memory protection unit (MPU), high-speed embedded memories (Flash memory up to 128 Kbytes and RAM up to 16 Kbytes) and an extensive range of enhanced I/Os and peripherals connected to two APB buses.

All the devices offer a 12-bit ADC, 2 DACs and 2 ultra-low-power comparators, six general-purpose 16-bit timers and two basic timers, which can be used as time bases.

Moreover, the STM32L151x6/8/B and STM32L152x6/8/B devices contain standard and advanced communication interfaces: up to two I^2Cs and SPIs, three USARTs and a USB. The STM32L151x6/8/B and STM32L152x6/8/B devices offer up to 20 capacitive sensing channels to simply add touch sensing functionality to any application.

They also include a real-time clock and a set of backup registers that remain powered in Standby mode.

Finally, the integrated LCD controller (except STM32L151x6/8/B devices) has a built-in LCD voltage generator that allows to drive up to 8 multiplexed LCDs with contrast independent of the supply voltage.

The ultra-low-power STM32L151x6/8/B and STM32L152x6/8/B devices operate from a 1.8 to 3.6 V power supply (down to 1.65 V at power down) with BOR and from a 1.65 to 3.6 V power supply without BOR option. It is available in the -40 to +85 °C temperature range, extended to 105°C in low power dissipation state. A comprehensive set of power-saving modes allows the design of low-power applications.

2.1 Device overview

Table 2. Ultra-low-power STM32L151x6/8/B and STM32L152x6/8/B device features and peripheral counts

Peripheral		STM32L15xCx			STM32L15xRx			STM32L15xVx	
Flash (Kbytes)		32	64	128	32	64	128	64	128
Data EEPROM (Kbytes)		4							
RAM (Kbytes)		10	10	16	10	10	16	10	16
Timers	General-purpose	6							
	Basic	2							
Communication interfaces	SPI	2							
	I^2C	2							
	USART	3							
	USB	1							
GPIOs		37			51			83	
12-bit synchronized ADC Number of channels		1 14 channels			1 20 channels			1 24 channels	
12-bit DAC Number of channels		2 2							
LCD (STM32L152xx Only) COM x SEG		4x18			4x32 8x28			4x44 8x40	
Comparator		2							
Capacitive sensing channels		13			20				
Max. CPU frequency		32 MHz							
Operating voltage		1.8 V to 3.6 V (down to 1.65 V at power-down) with BOR option 1.65 V to 3.6 V without BOR option							
Operating temperatures		Ambient temperatures: –40 to +85 °C Junction temperature: –40 to + 105 °C							
Packages		LQFP48, UFQFPN48			LQFP64, BGA64			LQFP100, BGA100	

Table 3. Functionalities depending on the operating power supply range (continued)

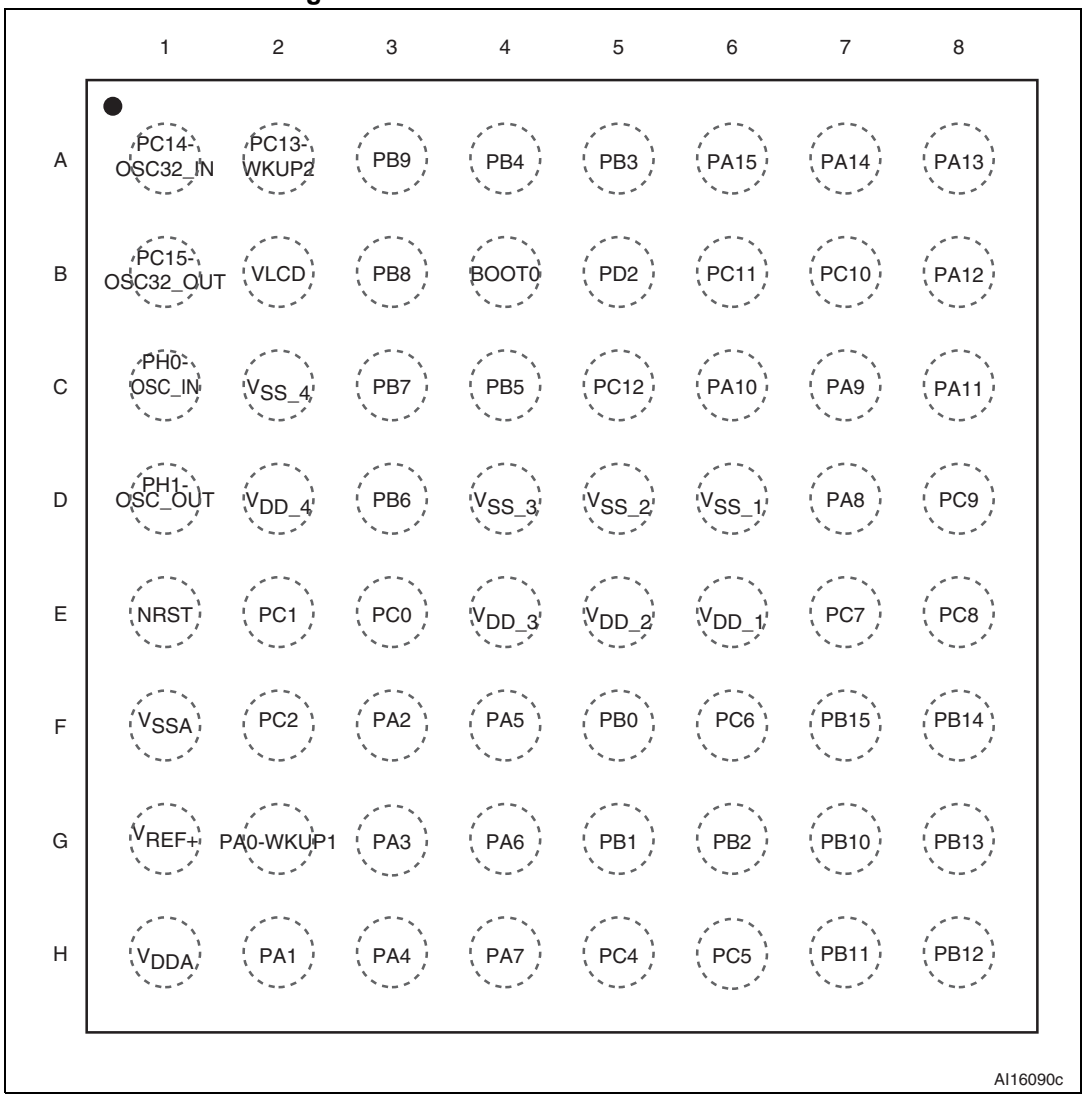
Operating power supply range	Functionalities depending on the operating power supply range			
	DAC and ADC operation	USB	Dynamic voltage scaling range	I/O operation
V_{DD} = 2.0 to 2.4 V	Conversion time up to 500 Ksps	Functional(2)	Range 1, Range 2 or Range 3	Full speed operation
V_{DD} = 2.4 to 3.6 V	Conversion time up to 1 Msps	Functional(2)	Range 1, Range 2 or Range 3	Full speed operation

1. The CPU frequency changes from initial to final must respect "F_{CPU} initial < 4*F_{CPU} final" to limit V_{CORE} drop due to current consumption peak when frequency increases. It must also respect 5 µs delay between two changes. For example to switch from 4.2 MHz to 32 MHz, you can switch from 4.2 MHz to 16 MHz, wait 5 µs, then switch from 16 MHz to 32 MHz.
2. Should be USB compliant from I/O voltage standpoint, the minimum V_{DD} is 3.0 V.

Table 4. CPU frequency range depending on dynamic voltage scaling

CPU frequency range	Dynamic voltage scaling range
16 MHz to 32 MHz (1ws) 32 kHz to 16 MHz (0ws)	Range 1
8 MHz to 16 MHz (1ws) 32 kHz to 8 MHz (0ws)	Range 2
2.1 MHz to 4.2 MHz (1ws) 32 kHz to 2.1 MHz (0ws)	Range 3

Figure 5. STM32L15xRx TFBGA64 ballout



1. This figure shows the package top view.

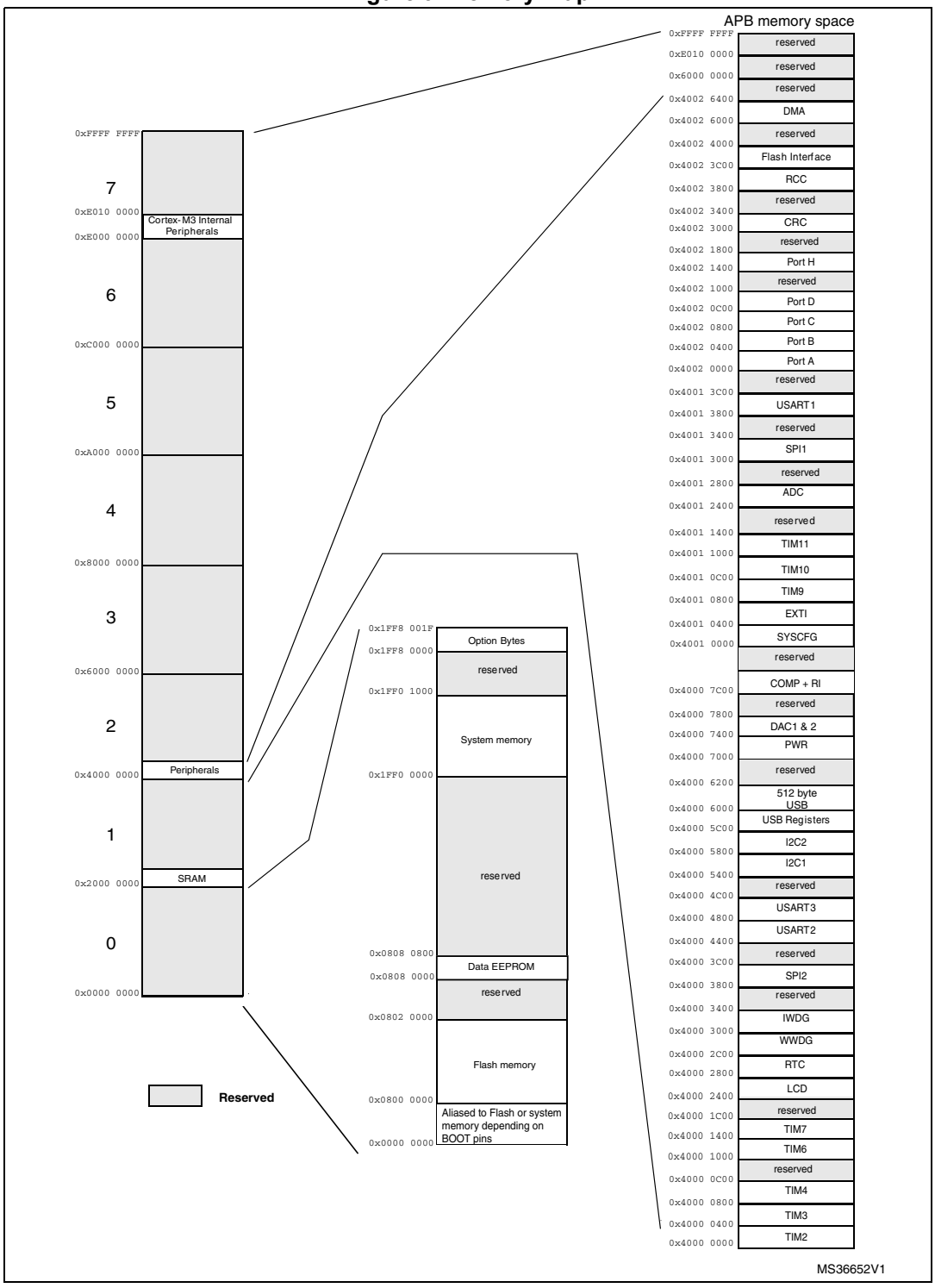
Table 9. Alternate function input/output (continued)

Port name	Digital alternate function number														
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFOI6	AFIO7	AFIO8	AFIO9	AFIO11	AFIO12	AFIO13	AFIO14	AFIO15
	Alternate function														
	SYSTEM	TIM2	TIM3/4	TIM9/10/11	I2C1/2	SPI1/2	N/A	USART1/2/3	N/A	N/A	LCD	N/A	N/A	RI	SYSTEM
PH1-OSC_OUT	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PH2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

5 Memory mapping

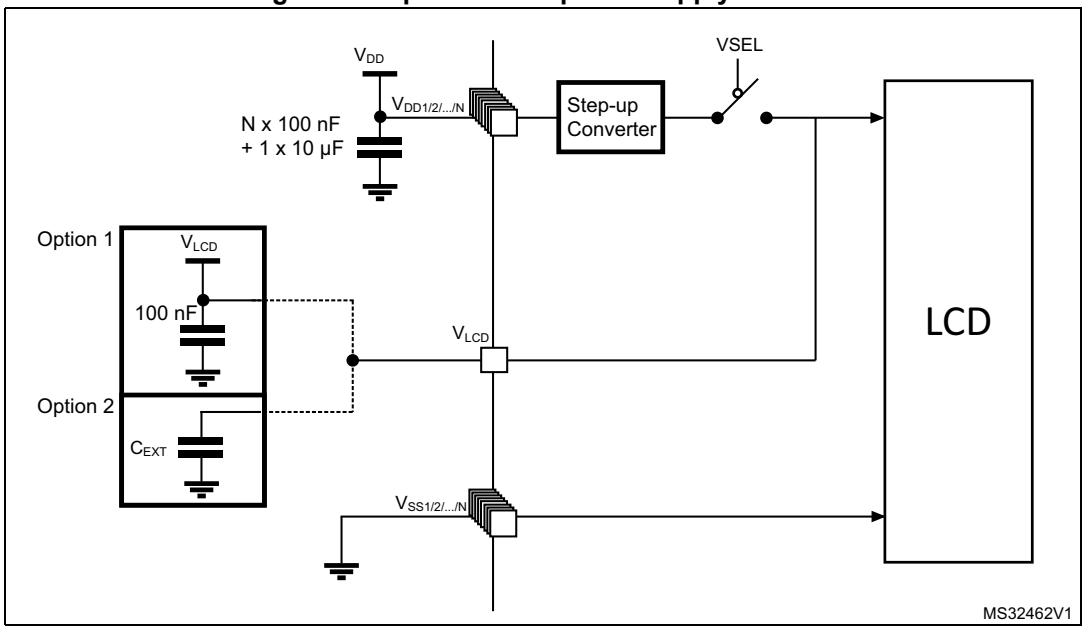
The memory map is shown in *Figure 9*.

Figure 9. Memory map



6.1.7 Optional LCD power supply scheme

Figure 13. Optional LCD power supply scheme



1. Option 1: LCD power supply is provided by a dedicated VLCD supply source, VSEL switch is open.
2. Option 2: LCD power supply is provided by the internal step-up converter, VSEL switch is closed, an external capacitance is needed for correct behavior of this converter.

6.1.8 Current consumption measurement

Figure 14. Current consumption measurement scheme

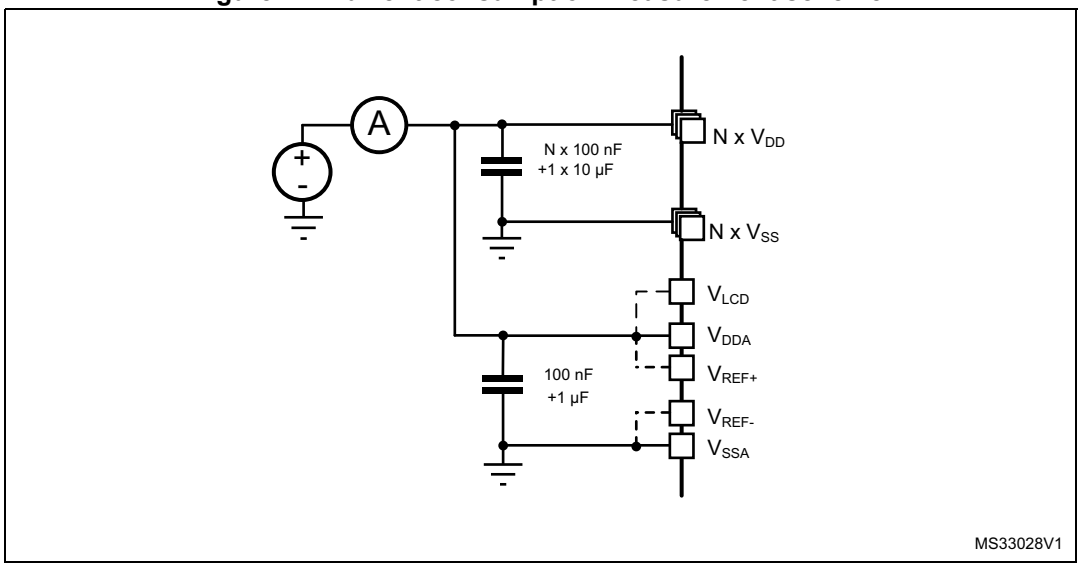


Table 12. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

6.3 Operating conditions

6.3.1 General operating conditions

Table 13. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	32	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	32	
f_{PCLK2}	Internal APB2 clock frequency	-	0	32	
V_{DD}	Standard operating voltage	BOR detector disabled	1.65	3.6	V
		BOR detector enabled, at power on	1.8	3.6	
		BOR detector disabled, after power on	1.65	3.6	
V_{DDA}(1)	Analog operating voltage (ADC and DAC not used)	Must be the same voltage as V_{DD}(2)	1.65	3.6	V
	Analog operating voltage (ADC or DAC used)		1.8	3.6	
V_{IN}	Input voltage on FT pins(3) Input voltage on BOOT0 pin Input voltage on any other pin	2.0 V ≤V_{DD} ≤ 3.6 V 1.65 V ≤ V_{DD} ≤ 2.0 V	–0.3 –0.3 0 –0.3	5.5 5.25 5.5 V_{DD}+0.3	V
P_D	Power dissipation at T_A = 85 °C(4)	BGA100 package	-	339	mW
T_A	Temperature range	Maximum power dissipation	–40	85	°C
		Low power dissipation(5)	–40	105	
T_J	Junction temperature range	-40 °C ≤T_A ≤105°C	–40	105	°C

1. When the ADC is used, refer to *Table 54: ADC characteristics*.
2. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and operation.
3. To sustain a voltage higher than V_{DD}+0.3 V, the internal pull-up/pull-down resistors must be disabled.
4. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_J max (see *Table 12: Thermal characteristics on page 53*).
5. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_J max (see *Table 12: Thermal characteristics on page 53*).

Table 14. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD0}	Programmable voltage detector threshold 0	Falling edge	1.8	1.85	1.88	V
		Rising edge	1.88	1.94	1.99	
V_{PVD1}	PVD threshold 1	Falling edge	1.98	2.04	2.09	
		Rising edge	2.08	2.14	2.18	
V_{PVD2}	PVD threshold 2	Falling edge	2.20	2.24	2.28	
		Rising edge	2.28	2.34	2.38	
V_{PVD3}	PVD threshold 3	Falling edge	2.39	2.44	2.48	
		Rising edge	2.47	2.54	2.58	
V_{PVD4}	PVD threshold 4	Falling edge	2.57	2.64	2.69	
		Rising edge	2.68	2.74	2.79	
V_{PVD5}	PVD threshold 5	Falling edge	2.77	2.83	2.88	
		Rising edge	2.87	2.94	2.99	
V_{PVD6}	PVD threshold 6	Falling edge	2.97	3.05	3.09	
		Rising edge	3.08	3.15	3.20	
V_{hyst}	Hysteresis voltage	BOR0 threshold	-	40	-	mV
		All BOR and PVD thresholds excepting BOR0	-	100	-	

1. Guaranteed by characterization results.
2. Valid for device version without BOR at power up. Please see option "T" in Ordering information scheme for more details.

Table 19. Current consumption in Sleep mode

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max(1)			Unit
						55 °C	85 °C	105 °C	
I_{DD} (Sleep)	Supply current in Sleep mode, code executed from RAM, Flash switched OFF	f_{HSE} = f_{HCLK} up to 16 MHz included, f_{HSE} = f_{HCLK}/2 above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	1 MHz	80	140	140	140	µA
				2 MHz	150	210	210	210	
				4 MHz	280	330	330	330(3)	
			Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	4 MHz	280	400	400	400	
				8 MHz	450	550	550	550	
				16 MHz	900	1050	1050	1050	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	8 MHz	550	650	650	650	
				16 MHz	1050	1200	1200	1200	
				32 MHz	2300	2500	2500	2500	
		HSI clock source (16 MHz)	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	16 MHz	1000	1100	1100	1100	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	32 MHz	2300	2500	2500	2500	
		MSI clock, 65 kHz	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	65 kHz	30	50	50	60	
		MSI clock, 524 kHz		524 kHz	50	70	70	80	
		MSI clock, 4.2 MHz		4.2 MHz	200	240	240	250	
	Supply current in Sleep mode, code executed from Flash	f_{HSE} = f_{HCLK} up to 16 MHz included, f_{HSE} = f_{HCLK}/2 above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	1 MHz	80	140	140	140	µA
				2 MHz	150	210	210	210	
				4 MHz	290	350	350	350	
			Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	4 MHz	300	400	400	400	
				8 MHz	500	600	600	600	
				16 MHz	1000	1100	1100	1100	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	8 MHz	550	650	650	650	
				16 MHz	1050	1200	1200	1200	
				32 MHz	2300	2500	2500	2500	
		HSI clock source (16 MHz)	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	16 MHz	1000	1100	1100	1100	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	32 MHz	2300	2500	2500	2500	

Low-speed external user clock generated from an external source

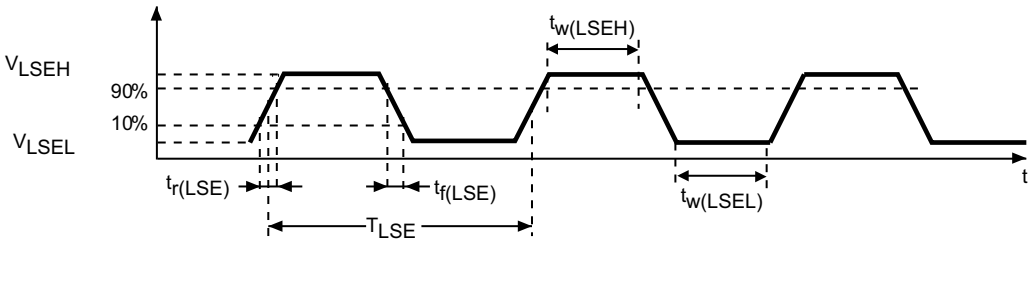
The characteristics given in the following table result from tests performed using a low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 13*.

Table 27. Low-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	1	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time		465	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time		-	-	10	
$C_{IN(LSE)}$	OSC32_IN input capacitance	-	-	0.6	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	45	-	55	%
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design.

Figure 16. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 1 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 28*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Multi-speed internal (MSI) RC oscillator

Table 32. MSI oscillator characteristics

Symbol	Parameter	Condition	Typ	Max	Unit
f_{MSI}	Frequency after factory calibration, done at V_{DD}= 3.3 V and T_A = 25 °C	MSI range 0	65.5	-	kHz
		MSI range 1	131	-	
		MSI range 2	262	-	
		MSI range 3	524	-	
		MSI range 4	1.05	-	MHz
		MSI range 5	2.1	-	
		MSI range 6	4.2	-	
ACC_{MSI}	Frequency error after factory calibration	-	±0.5	-	%
$D_{TEMP(MSI)}$(1)	MSI oscillator frequency drift 0 °C ≤T_A ≤85 °C	-	±3	-	%
$D_{VOLT(MSI)}$(1)	MSI oscillator frequency drift 1.65 V ≤V_{DD} ≤3.6 V, T_A = 25 °C	-	-	2.5	%/V
$I_{DD(MSI)}$(2)	MSI oscillator power consumption	MSI range 0	0.75	-	µA
		MSI range 1	1	-	
		MSI range 2	1.5	-	
		MSI range 3	2.5	-	
		MSI range 4	4.5	-	
		MSI range 5	8	-	
		MSI range 6	15	-	
$t_{SU(MSI)}$	MSI oscillator startup time	MSI range 0	30	-	µs
		MSI range 1	20	-	
		MSI range 2	15	-	
		MSI range 3	10	-	
		MSI range 4	6	-	
		MSI range 5	5	-	
		MSI range 6, Voltage range 1 and 2	3.5	-	
		MSI range 6, Voltage range 3	5	-	

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 38. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. frequency range			Unit
				4 MHz voltage Range 3	16 MHz voltage Range 2	32 MHz voltage Range 1	
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = 25 °C, LQFP100 package compliant with IEC 61967-2	0.1 to 30 MHz	3	-6	-5	dBµV
			30 to 130 MHz	18	4	-7	
			130 MHz to 1GHz	15	5	-7	
			SAE EMI Level	2.5	2	1	-

6.3.11 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 39. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Packages	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JESD22-A114	All	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to JESD22-C101	All	III	500	

1. Guaranteed by characterization results.

6.3.13 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 42* are derived from tests performed under conditions summarized in *Table 13*. All I/Os are CMOS and TTL compliant.

Table 42. I/O static characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IL}	Input low level voltage	-	-	-	-	$0.3V_{DD}$ (1)	V
V_{IH}	Input high level voltage	Standard I/O		$0.7\ V_{DD}$	-	-	
		FT I/O			-	-	
V_{hys}	I/O Schmitt trigger voltage hysteresis(2)	Standard I/O		-	10% V_{DD} (3)	-	
		FT I/O		-	5% V_{DD} (4)	-	
I_{lkg}	Input leakage current (5)	$V_{SS} \le V_{IN} \le V_{DD}$ I/Os with LCD		-	-	±50	nA
		$V_{SS} \le V_{IN} \le V_{DD}$ I/Os with analog switches		-	-	±50	
		$V_{SS} \le V_{IN} \le V_{DD}$ I/Os with analog switches and LCD		-	-	±50	
		$V_{SS} \le V_{IN} \le V_{DD}$ I/Os with USB		-	-	TBD	
		FT I/O $V_{DD} \le V_{IN} \le 5V$		-	-	TBD	
		$V_{SS} \le V_{IN} \le V_{DD}$ Standard I/Os		-	-	±50	
R_{PU}	Weak pull-up equivalent resistor(6)(1)	$V_{IN} = V_{SS}$		30	45	60	kΩ
R_{PD}	Weak pull-down equivalent resistor(6)	$V_{IN} = V_{DD}$		30	45	60	kΩ
C_{IO}	I/O pin capacitance	-	-	-	5	-	pF

1. Tested in production
2. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization.
3. With a minimum of 200 mV. Based on characterization results.
4. With a minimum of 100 mV. Based on characterization results.
5. The max. value may be exceeded if negative current is injected on adjacent pins.
6. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This MOS/NMOS contribution to the series resistance is minimum (~10% order).

Table 55. ADC accuracy(1)(2)

Symbol	Parameter	Test conditions	Min(3)	Typ	Max(3)	Unit
ET	Total unadjusted error	$2.4\ V \le V_{DDA} \le 3.6\ V$ $2.4\ V \le V_{REF+} \le 3.6\ V$ $f_{ADC} = 8\ MHz$, $R_{AIN} = 50\ \Omega$ $T_A = -40$ to $105\ °C$	-	2	4	LSB
EO	Offset error		-	1	2	
EG	Gain error		-	1.5	3.5	
ED	Differential linearity error		-	1	2	
EL	Integral linearity error		-	1.7	3	
ENOB	Effective number of bits	$2.4\ V \le V_{DDA} \le 3.6\ V$ $V_{DDA} = V_{REF+}$ $f_{ADC} = 16\ MHz$, $R_{AIN} = 50\ \Omega$ $T_A = -40$ to $105\ °C$ $1\ kHz \le F_{input} \le 100\ kHz$	9.2	10	-	bits
SINAD	Signal-to-noise and distortion ratio		57.5	62	-	dB
SNR	Signal-to-noise ratio		57.5	62	-	
THD	Total harmonic distortion		-74	-75	-	
ET	Total unadjusted error	$2.4\ V \le V_{DDA} \le 3.6\ V$ $1.8\ V \le V_{REF+} \le 2.4\ V$ $f_{ADC} = 4\ MHz$, $R_{AIN} = 50\ \Omega$ $T_A = -40$ to $105\ °C$	-	4	6.5	LSB
EO	Offset error		-	2	4	
EG	Gain error		-	4	6	
ED	Differential linearity error		-	1	2	
EL	Integral linearity error		-	1.5	3	
ET	Total unadjusted error	$1.8\ V \le V_{DDA} \le 2.4\ V$ $1.8\ V \le V_{REF+} \le 2.4\ V$ $f_{ADC} = 4\ MHz$, $R_{AIN} = 50\ \Omega$ $T_A = -40$ to $105\ °C$	-	2	3	LSB
EO	Offset error		-	1	1.5	
EG	Gain error		-	1.5	2	
ED	Differential linearity error		-	1	2	
EL	Integral linearity error		-	1	1.5	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative injection current: Injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.12* does not affect the ADC accuracy.
3. Guaranteed by characterization results.

Figure 28. Maximum dynamic current consumption on V_{REF+} supply pin during ADC conversion

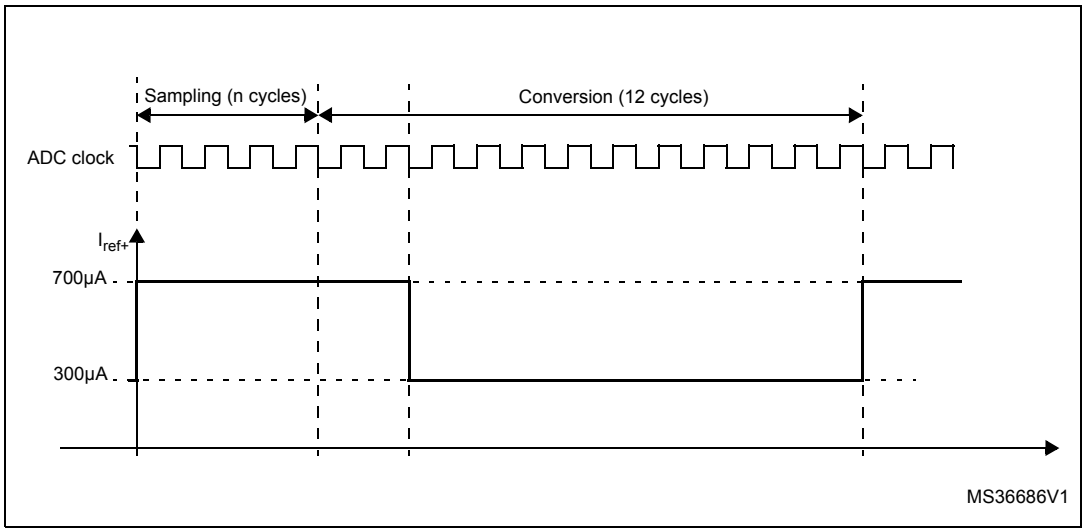


Table 56. Maximum source impedance R_{AIN} max(1)

Ts (µs)	R_{AIN} max (kOhm)				Ts (cycles) f_{ADC}= 16 MHz(2)
	Multiplexed channels		Direct channels		
	2.4 V < V_{DDA}< 3.6 V	1.8 V < V_{DDA} < 2.4 V	2.4 V < V_{DDA}< 3.3 V	1.8 V < V_{DDA} < 2.4 V	
0.25	Not allowed	Not allowed	0.7	Not allowed	4
0.5625	0.8	Not allowed	2.0	1.0	9
1	2.0	0.8	4.0	3.0	16
1.5	3.0	1.8	6.0	4.5	24
3	6.8	4.0	15.0	10.0	48
6	15.0	10.0	30.0	20.0	96
12	32.0	25.0	50.0	40.0	192
24	50.0	50.0	50.0	50.0	384

1. Guaranteed by design.
2. Number of samples calculated for **f_{ADC} = 16 MHz. F**or **f_{ADC} = 8 and 4 MHz the number of sampling cycles can be reduced with respect to the minimum sampling time Ts (us).**

General PCB design guidelines

Power supply decoupling should be performed as shown in The 10 nF capacitors should be ceramic (good quality). They should be placed as close as possible to the chip.

6.3.20 Comparator

Table 60. Comparator 1 characteristics

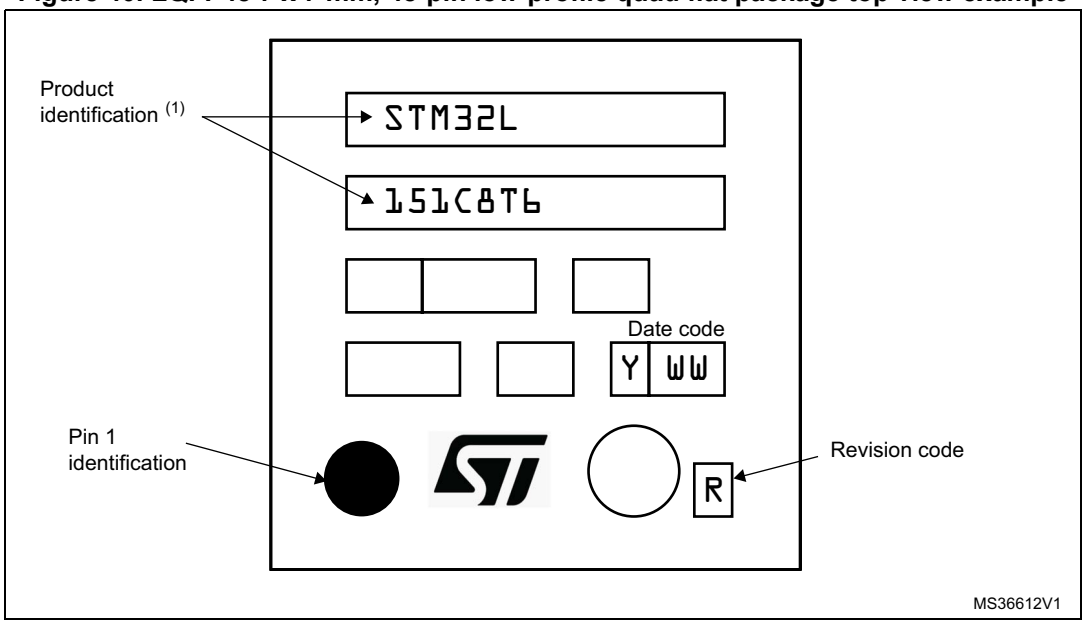
Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage	-	1.65		3.6	V
R_{400K}	R_{400K} value	-	-	400	-	kΩ
R_{10K}	R_{10K} value	-	-	10	-	
V_{IN}	Comparator 1 input voltage range	-	0.6	-	V_{DDA}	V
t_{START}	Comparator startup time	-	-	7	10	µs
td	Propagation delay(2)	-	-	3	10	
Voffset	Comparator offset	-	-	±3	±10	mV
$d_{Voffset}/dt$	Comparator offset variation in worst voltage stress conditions	V_{DDA} = 3.6 V V_{IN+} = 0 V V_{IN-} = V_{REFINT} T_A = 25 °C	0	1.5	10	mV/1000 h
I_{COMP1}	Current consumption(3)	-	-	160	260	nA

1. Guaranteed by characterization results.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage not included.

LQFP48 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 40. LQFP48 7 x 7 mm, 48-pin low-profile quad flat package top view example



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

8 Ordering information

Table 72. Ordering information scheme

Example: STM32 L 151 C 8 T 6 T TR

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

L = Low power

Device subfamily

151: Devices without LCD

152: Devices with LCD

Pin count

C = 48 pins

R = 64 pins

V = 100 pins

Flash memory size

6 = 32 Kbytes of Flash memory

8 = 64 Kbytes of Flash memory

B = 128 Kbytes of Flash memory

Package

H = BGA

T = LQFP

U = UFQFPN

Temperature range

6 = Industrial temperature range, –40 to 85 °C

Options

No character = V_{DD} range: 1.8 to 3.6 V and BOR enabled

T = V_{DD} range: 1.65 to 3.6 V and BOR disabled

Packing

TR = tape and reel

No character = tray or tube

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.