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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Not For New Designs
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, Cap Sense, DMA, I <sup>2</sup> S, LCD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 20x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TFBGA
Supplier Device Package	64-TFBGA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l152rbh6

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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## 3.17 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

## 3.18 Development support

#### Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG JTMS and JTCK pins are shared with SWDAT and SWCLK, respectively, and a specific sequence on the JTMS pin is used to switch between JTAG-DP and SW-DP.

The JTAG port can be permanently disabled with a JTAG fuse.

#### Embedded Trace Macrocell™

The ARM Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32L151x6/8/B and STM32L152x6/8/B device through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer running debugger software. TPA hardware is commercially available from common development tool vendors. It operates with third party debugger software tools.

#### STM32L151x6/8/B STM32L152x6/8/B

	1	2	3	4	5	6	7	8
A	, PC14-, 0, SC32_IN	, PC13-, WKUP2	(PB9)	( PB4 )	( PB3 )	(PA15)	(PA14)	(PA13)
В	, <sup>/</sup> Ρ́C15-`, OŚC32_ΟUT	- (VLCD)	(PB8)	воото	( PD2 )	(PC11)	(PC10)	(PA12)
С	,∕₽́ĤÒ÷, OSC_IN∳	Vss_4	(PB7)	(PB5)	(PC12)	(PA10)	( PA9 )	(PA11)
D	OSC_OUT	VDD_4	(PB6)	VSS_3	VSS_2	VSS_1	( PA8 )	(PC9)
E	(NRST)	(PC1)	(PC0)	'V <sub>DD_3</sub> '	'VDD_2'	VDD_1	(PC7)	(PC8)
F	(V <sub>SSA</sub> )	( PC2 )	( PA2 )	( PA5 )	(PB0)	( PC6 )	(PB15)	(PB14)
G	VREF+)	PA(0-WKU)P1	( PA3 )	( PA6 )	// PB1 /	( PB2 )	(PB10)	(PB13)
н	VDDA,	(PA1)	( PA4 )	(PA7)	(PC4)	( PC5 )	(PB11)	(PB12)
								Al1609

Figure 5. STM32L15xRx TFBGA64 ballout

1. This figure shows the package top view.



		Pin	s						Pins functions	
LQFP100	LQFP64	TFBGA64	UFBGA100	LQFP48 or UFQFPN48	Pin name	Pin type <sup>(1)</sup>	I/O structure	Main function <sup>(2)</sup> (after reset)	Alternate functions	Additional functions
90	56	A4	A7	40	PB4	I/O	FT	NJTRST	TIM3_CH1/PB4/ SPI1_MISO/LCD_SEG8/ NJTRST	COMP2_INP
91	57	C4	C5	41	PB5	I/O	FT	PB5	I2C1_SMBA/TIM3_CH2/ SPI1_MOSI/LCD_SEG9	COMP2_INP
92	58	D3	B5	42	PB6	I/O	FT	PB6	I2C1_SCL/TIM4_CH1/ USART1_TX	
93	59	C3	B4	43	PB7	I/O	FT	PB7	I2C1_SDA/TIM4_CH2/ USART1_RX	PVD_IN
94	60	B4	A4	44	BOOT0	Ι	В	BOOT0	-	-
95	61	В3	A3	45	PB8	I/O	FT	PB8	TIM4_CH3/I2C1_SCL/ LCD_SEG16/TIM10_CH1	-
96	62	A3	B3	46	PB9	I/O	FT	PB9	TIM4_CH4/I2C1_SDA/ LCD_COM3/TIM11_CH1	-
97	-	-	C3	-	PE0	I/O	FT	PE0	TIM4_ETR/LCD_SEG36/ TIM10_CH1	-
98	-	-	A2	-	PE1	I/O	FT	PE1	LCD_SEG37/TIM11_CH1	-
99	63	D4	D3	47	V <sub>SS_3</sub>	S	-	V <sub>SS_3</sub>	-	-
100	64	E4	C4	48	$V_{DD_3}$	s	-	V <sub>DD_3</sub>	-	-

1. I = input, O = output, S = supply.

 Function availability depends on the chosen device. For devices having reduced peripheral counts, it is always the lower number of peripheral that is included. For example, if a device has only one SPI and two USARTs, they will be called SPI1 and USART1 & USART2, respectively. Refer to *Table 2 on page 11*.

3. Applicable to STM32L152xx devices only. In STM32L151xx devices, this pin should be connected to V<sub>DD</sub>.

4. The PC14 and PC15 I/Os are only configured as OSC32\_IN/OSC32\_OUT when the LSE oscillator is on (by setting the LSEON bit in the RCC\_CSR register). The LSE oscillator pins OSC32\_IN/OSC32\_OUT can be used as general-purpose PC14/PC15 I/Os, respectively, when the LSE oscillator is off (after reset, the LSE oscillator is off). The LSE has priority over the GPIO function. For more details, refer to Using the OSC32\_IN/OSC32\_OUT pins as GPIO PC14/PC15 port pins section in the STM32L1xxxx reference manual (RM0038).

 The PH0 and PH1 I/Os are only configured as OSC\_IN/OSC\_OUT when the HSE oscillator is on (by setting the HSEON bit in the RCC\_CR register). The HSE oscillator pins OSC\_IN/OSC\_OUT can be used as general-purpose PH0/PH1 I/Os, respectively, when the HSE oscillator is off (after reset, the HSE oscillator is off). The HSE has priority over the GPIO function.

6. Unlike in the LQFP64 package, there is no PC3 in the TFBGA64 package. The V<sub>REF+</sub> functionality is provided instead.



Symbol	Ratings	Value	Unit
T <sub>STG</sub>	Storage temperature range	-65 to +150	°C
TJ	Maximum junction temperature	150	°C

#### Table 12. Thermal characteristics

## 6.3 Operating conditions

#### 6.3.1 General operating conditions

Symbol	Parameter	Conditions	Min	Мах	Unit	
f <sub>HCLK</sub>	Internal AHB clock frequency	-	0	32		
f <sub>PCLK1</sub>	Internal APB1 clock frequency	-	0	32	MHz	
f <sub>PCLK2</sub>	Internal APB2 clock frequency	-	0	32		
		BOR detector disabled	1.65	3.6		
V <sub>DD</sub>	Standard operating voltage	BOR detector enabled, at power on	1.8	3.6	v	
		BOR detector disabled, after power on	1.65	3.6		
v (1)	Analog operating voltage (ADC and DAC not used)	Must be the same voltage as	1.65	3.6	V	
VDDA` ′	Analog operating voltage (ADC or DAC used)	V <sub>DD</sub> <sup>(2)</sup>	1.8	3.6	v	
	Input voltage on FT pins <sup>(3)</sup>	2.0 V ≤V <sub>DD</sub> ≤ 3.6 V	-0.3	5.5		
VIN		$1.65 \text{ V} \le \text{V}_{\text{DD}} \le 2.0 \text{ V}$	-0.3	5.25	V	
	Input voltage on BOOT0 pin		0	5.5		
	Input voltage on any other pin		-0.3	V <sub>DD</sub> +0.3		
$P_D$	Power dissipation at $T_A = 85 \ ^{\circ}C^{(4)}$	BGA100 package	-	339	mW	
Тл	Tomporaturo rango	Maximum power dissipation	-40	85	°C	
IA		Low power dissipation <sup>(5)</sup>	-40	105		
TJ	Junction temperature range	-40 °C ≤T <sub>A</sub> ≤105°C	-40	105	°C	

#### Table 13. General operating conditions

1. When the ADC is used, refer to Table 54: ADC characteristics.

2. It is recommended to power V<sub>DD</sub> and V<sub>DDA</sub> from the same source. A maximum difference of 300 mV between V<sub>DD</sub> and V<sub>DDA</sub> can be tolerated during power-up and operation.

3. To sustain a voltage higher than  $V_{DD}$ +0.3 V, the internal pull-up/pull-down resistors must be disabled.

 If T<sub>A</sub> is lower, higher P<sub>D</sub> values are allowed as long as T<sub>J</sub> does not exceed T<sub>J</sub> max (see Table 12: Thermal characteristics on page 53).

In low power dissipation state, T<sub>A</sub> can be extended to this range as long as T<sub>J</sub> does not exceed T<sub>J</sub> max (see *Table 12: Thermal characteristics on page 53*).



		otor Conditions			-		Unit		
Symbol	Parameter	Cond	litions	THCLK	Тур	55 °C	85 °C	105 °C	Unit
			Range 3, V <sub>CORE</sub> =1.2 V	1 MHz	80	140	140	140	
				2 MHz	150	210	210	210	
			VOS[1:0] = 11	4 MHz	280	330	330	330 <sup>(3)</sup>	
		f <sub>HSE</sub> = f <sub>HCLK</sub> up to 16 MHz included	Range 2	4 MHz	280	400	400	400	
		$f_{HSE} = f_{HCLK}/2$	V <sub>CORE</sub> =1.5 V	8 MHz	450	550	550	550	
	Supply	above 16 MHz (PLL ON) <sup>(2)</sup>	VOS[1:0] = 10	16 MHz	900	1050	1050	1050	
	Sleep	- /	Range 1.	8 MHz	550	650	650	650	
	mode,		V <sub>CORE</sub> =1.8 V	16 MHz	1050	1200	1200	1200	
	executed		VOS[1:0] = 01	32 MHz	2300	2500	2500	2500	μA
	from RAM, Flash switched	HSI clock source (16 MHz)	Range 2, V <sub>CORE</sub> =1.5 V VOS[1:0] = 10	16 MHz	1000	1100	1100	1100	
			Range 1, V <sub>CORE</sub> =1.8 V VOS[1:0] = 01	32 MHz	2300	2500	2500	2500	
_		MSI clock, 65 kHz	Range 3, V <sub>CORE</sub> =1.2 V	65 kHz	30	50	50	60	
I <sub>DD</sub> (Sleen)		MSI clock, 524 kHz		524 kHz	50	70	70	80	
(Oleep)		MSI clock, 4.2 MHz	VOS[1:0] = 11	4.2 MHz	200	240	240	250	
			Range 3, V <sub>CORE</sub> =1.2 V VOS[1:0] = 11	1 MHz	80	140	140	140	
				2 MHz	150	210	210	210	
				4 MHz	290	350	350	350	
		f <sub>HSE</sub> = f <sub>HCLK</sub> up to 16 MHz included,	Range 2,	4 MHz	300	400	400	400	
	Supply	$f_{HSE} = f_{HCLK}/2$	V <sub>CORE</sub> =1.5 V	8 MHz	500	600	600	600	
	current in	ON) <sup>(2)</sup>	VOS[1:0] = 10	16 MHz	1000	1100	1100	1100	
	mode,		Range 1,	8 MHz	550	650	650	650	μA
	code		V <sub>CORE</sub> =1.8 V	16 MHz	1050	1200	1200	1200	
	from Flash		VOS[1:0] = 01	32 MHz	2300	2500	2500	2500	
		HSI clock source	Range 2, V <sub>CORE</sub> =1.5 V VOS[1:0] = 10	16 MHz	1000	1100	1100	1100	
		HSI clock source (16 MHz)	Range 1, V <sub>CORE</sub> =1.8 V VOS[1:0] = 01	32 MHz	2300	2500	2500	2500	

Table 19. Current consumption in Sleep mode



Symbol	Parameter	Cons	litione	4	f Turn	Max <sup>(1)</sup>			llait
		Conditions		HCLK	тур	55 °C	85 °C	105 °C	Unit
	Supply current in Sleep	MSI clock, 65 kHz	Range 3.	65 kHz	40	70	70	80	
		MSI clock, 524 kHz		524 kHz	60	90	90	100	
I <sub>DD</sub> (Sleep)	mode, code executed from Flash	MSI clock, 4.2 MHz	V <sub>CORE</sub> =1.2V VOS[1:0] = 11	4.2 MHz	210	250	250	260	μA

 Table 19. Current consumption in Sleep mode (continued)

1. Guaranteed by characterization results, unless otherwise specified.

2. Oscillator bypassed (HSEBYP = 1 in RCC\_CR register)

3. Tested in production



Symbol	Parameter	Conditions				Max (1)	Unit
			MSI clock, 65 kHz f <sub>HCLK</sub> = 32 kHz Flash OFF	$T_A$ = -40 °C to 25 °C	4.4	-	
			MSI clock, 65 kHz	$T_A$ = -40 °C to 25 °C	17.5	25	
			f <sub>HCLK</sub> = 32 kHz	T <sub>A</sub> = 85 °C	22	27	
		All	Flash ON	T <sub>A</sub> = 105 °C	31	39	
I <sub>DD</sub> (LP		OFF, V <sub>DD</sub>	MSI clock, 65 kHz	$T_A$ = -40 °C to 25 °C	18	26	
		from 1.65 V	f <sub>HCLK</sub> = 65 kHz,	T <sub>A</sub> = 85 °C	23	28	
		10 J.0 V	Flash ON	T <sub>A</sub> = 105 °C	31	40	
	Supply current in Low power sleep mode			T <sub>A</sub> = -40 °C to 25 °C	22	30	
			MSI clock, 131 kHz f <sub>HCLK</sub> = 131 kHz, Flash ON	T <sub>A</sub> = 55 °C	24	32	μA
				T <sub>A</sub> = 85 °C	26	34	
Sleep)				T <sub>A</sub> = 105 °C	34	45	
		TIMO and		$T_A$ = -40 °C to 25 °C	17.5	25	
			мэт сюск, 65 кнz f <sub>HCLK</sub> = 32 kHz	T <sub>A</sub> = 85 °C	22	27	
			HOLK	T <sub>A</sub> = 105 °C	31	39	
		USART1	MSI clock, 65 kHz	T <sub>A</sub> = -40 °C to 25 °C	18	26	
		enabled, Flash ON		T <sub>A</sub> = 85 °C	23	28	
		V <sub>DD</sub> from		T <sub>A</sub> = 105 °C	31	40	
		1.65 V to		T <sub>A</sub> = -40 °C to 25 °C	22	30	
		0.0 V	MSI clock, 131 kHz	T <sub>A</sub> = 55 °C	24	32	
			f <sub>HCLK</sub> = 131 kHz	T <sub>A</sub> = 85 °C	26	34	
				T <sub>A</sub> = 105 °C	34	45	
I <sub>DD</sub> Max (LP Sleep)	Max allowed current in Low power Sleep mode	V <sub>DD</sub> from 1.65 V to 3.6 V	-	-	-	200	

Table 21. Current consumption in Low power sleep mode

1. Guaranteed by characterization results, unless otherwise specified.



#### Low-speed external user clock generated from an external source

The characteristics given in the following table result from tests performed using a lowspeed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 13*.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit	
f <sub>LSE_ext</sub>	User external clock source frequency		1	32.768	1000	kHz	
V <sub>LSEH</sub>	OSC32_IN input pin high level voltage		0.7V <sub>DD</sub>	-	V <sub>DD</sub>	V	
V <sub>LSEL</sub>	OSC32_IN input pin low level voltage	-	V <sub>SS</sub>	-	0.3V <sub>DD</sub>	v	
t <sub>w(LSEH)</sub> t <sub>w(LSEL)</sub>	OSC32_IN high or low time		465	-	-	ne	
t <sub>r(LSE)</sub> t <sub>f(LSE)</sub>	OSC32_IN rise or fall time		-	-	10	115	
C <sub>IN(LSE)</sub>	OSC32_IN input capacitance	-	-	0.6	-	pF	
DuCy <sub>(LSE)</sub>	Duty cycle	-	45	-	55	%	
١L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	μA	

Table 27. Low-speed external user clock characteristics<sup>(1)</sup>

1. Guaranteed by design.





#### High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 1 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 28*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).



- t<sub>SU(LSE)</sub> is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.
- Note: For CL1 and CL2, it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator (see Figure 18). CL1 and CL2, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of CL1 and CL2. Load capacitance CL has the following formula: CL = CL1 x CL2 / (CL1 + CL2) + Cstray where Cstray is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.
- **Caution:** To avoid exceeding the maximum value of CL1 and CL2 (15 pF) it is strongly recommended to use a resonator with a load capacitance CL ≤ 7 pF. Never use a resonator with a load capacitance of 12.5 pF.

Example: if a resonator is chosen with a load capacitance of CL = 6 pF and Cstray = 2 pF, then CL1 = CL2 = 8 pF.



#### Figure 18. Typical application with a 32.768 kHz crystal

#### 6.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

#### Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- Electrostatic discharge (ESD) (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- FTB: A Burst of Fast Transient voltage (positive and negative) is applied to V<sub>DD</sub> and V<sub>SS</sub> through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table* 37. They are based on the EMS levels and classes defined in application note AN1709.

Symbol	Parameter	Conditions	Level/ Class
V <sub>FESD</sub>	Voltage limits to be applied on any I/O pin to induce a functional disturbance	$V_{DD}$ = 3.3 V, LQFP100, T <sub>A</sub> = +25 °C, f <sub>HCLK</sub> = 32 MHz conforms to IEC 61000-4-2	2B
V <sub>EFTB</sub>	Fast transient voltage burst limits to be applied through 100 pF on $V_{DD}$ and $V_{SS}$ pins to induce a functional disturbance	$\label{eq:VDD} \begin{array}{l} V_{DD} = 3.3 \text{ V}, \text{LQFP100},  \text{T}_{\text{A}} = +25 \\ ^{\circ}\text{C}, \\ \text{f}_{\text{HCLK}} = 32 \text{ MHz} \\ \text{conforms to IEC 61000-4-4} \end{array}$	4A

Table 37. EMS characteristics

#### Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

#### Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the oscillator pins for 1 second.



#### **SPI characteristics**

Unless otherwise specified, the parameters given in the following table are derived from tests performed under ambient temperature,  $f_{PCLKx}$  frequency and  $V_{DD}$  supply voltage conditions summarized in *Table 13*.

Refer to *Section 6.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Symbol	Parameter	Conditions	Min	Max <sup>(2)</sup>	Unit
_		Master mode	-	16	
f <sub>SCK</sub> 1/t <sub>e(SCK)</sub>	SPI clock frequency	Slave mode	-	16	MHz
		Slave transmitter	-	12 <sup>(3)</sup>	
$t_{r(SCK)}^{(2)}_{t_{f(SCK)}^{(2)}}$	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	6	ns
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	30	70	%
t <sub>su(NSS)</sub>	NSS setup time	Slave mode	4t <sub>HCLK</sub>	-	
t <sub>h(NSS)</sub>	NSS hold time	Slave mode	2t <sub>HCLK</sub>	-	
t <sub>w(SCKH)</sub> <sup>(2)</sup> t <sub>w(SCKL)</sub> <sup>(2)</sup>	SCK high and low time	Master mode	t <sub>SCK</sub> /2– 5	t <sub>SCK</sub> /2+ 3	
t <sub>su(MI)</sub> <sup>(2)</sup>	Data input setun time	Master mode	5	-	
t <sub>su(SI)</sub> <sup>(2)</sup>		Slave mode	6	-	
t <sub>h(MI)</sub> <sup>(2)</sup>	Data input hold time	Master mode	5	-	ns
t <sub>h(SI)</sub> <sup>(2)</sup>		Slave mode	5	-	
t <sub>a(SO)</sub> <sup>(4)</sup>	Data output access time	Slave mode	0	3t <sub>HCLK</sub>	
t <sub>v(SO)</sub> (2)	Data output valid time	Slave mode	-	33	
$t_{v(MO)}^{(2)}$	Data output valid time	Master mode	-	6.5	
t <sub>h(SO)</sub> <sup>(2)</sup>	Data output hold time	Slave mode	17	-	
t <sub>h(MO)</sub> <sup>(2)</sup>		Master mode	0.5	-	

1. The characteristics above are given for voltage Range 1.

2. Guaranteed by characterization results.

3. The maximum SPI clock frequency in slave transmitter mode is given for an SPI slave input clock duty cycle (DuCy(SCK)) ranging between 40 to 60%.

4. Min time is for the minimum time to drive the output and max time is for the maximum time to validate the data.





#### Figure 26. ADC accuracy characteristics

#### Figure 27. Typical connection diagram using the ADC



- 1. Refer to Table 56: Maximum source impedance RAIN max for the value of R<sub>AIN</sub> and Table 54: ADC characteristics for the value of CADC
- C<sub>parasitic</sub> represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high C<sub>parasitic</sub> value will downgrade conversion accuracy. To remedy this, f<sub>ADC</sub> should be reduced.



### 6.3.20 Comparator

Symbol	Parameter	Conditions	Min <sup>(1)</sup>	Тур	Max <sup>(1)</sup>	Unit
$V_{DDA}$	Analog supply voltage	-	1.65		3.6	V
R <sub>400K</sub>	R <sub>400K</sub> value	-	-	400	-	kO
R <sub>10K</sub>	R <sub>10K</sub> value	-	-	10	-	N32
V <sub>IN</sub>	Comparator 1 input voltage range	-	0.6	-	V <sub>DDA</sub>	V
t <sub>START</sub>	Comparator startup time	-	-	7	10	110
td	Propagation delay <sup>(2)</sup>	-	-	3	10	μο
Voffset	Comparator offset	-	-	±3	±10	mV
d <sub>Voffset</sub> /dt	Comparator offset variation in worst voltage stress conditions	$V_{DDA} = 3.6 V$ $V_{IN+} = 0 V$ $V_{IN-} = V_{REFINT}$ $T_{A} = 25 ^{\circ}C$	0	1.5	10	mV/1000 h
I <sub>COMP1</sub>	Current consumption <sup>(3)</sup>	-	-	160	260	nA

Table 60. Comparator 1 characteristics

1. Guaranteed by characterization results.

2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.

3. Comparator consumption only. Internal reference voltage not included.



## 7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK<sup>®</sup> is an ST trademark.

# 7.1 LQFP100 14 x 14 mm, 100-pin low-profile quad flat package information



Figure 32. LQFP100 14 x 14 mm, 100-pin low-profile quad flat package outline

1. Drawing is not to scale.



	millimeters			inches <sup>(1)</sup>		
Symbol	Min	Тур	Мах	Min	Тур	Мах
А	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
С	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
е	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
CCC	-	-	0.080	-	-	0.0031

## Table 63. LQPF100 14 x 14 mm, 100-pin low-profile quad flat package mechanical data

1. Values in inches are converted from mm and rounded to 4 decimal digits.



# 7.2 LQFP64 10 x 10 mm, 64-pin low-profile quad flat package information



Figure 35. LQFP64 10 x 10 mm, 64-pin low-profile quad flat package outline

1. Drawing is not to scale.

Table 64. LQFP64 10 x 10 mm, 64-pin low-profile quad flat package mechanical
data

Symbol	millimeters			inches <sup>(1)</sup>		
Symbol	Min	Тур	Мах	Тур	Min	Мах
А	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
С	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-



Symbol	millimeters			inches <sup>(1)</sup>		
Symbol	Min	Тур	Мах	Min	Тур	Мах
А	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
Т	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
е	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

Table 66. UFQFPN48 7 x 7 mm, 0.5 mm pitch, package mechanical data

1. Values in inches are converted from mm and rounded to 4 decimal digits.



#### Figure 42. UFQFPN48 7 x 7 mm, 0.5 mm pitch, package recommended footprint

1. Dimensions are in millimeters.



Date	Revision	Changes
12-Nov-2013	9 (continued)	Updated Table 54: ADC characteristics and Figure 27: Typical connection diagram using the ADC. Table 58: Temperature sensor calibration values was previously in Section 3.10.1: Temperature sensor. Updated Table 59: Temperature sensor characteristics. In Table 61: Comparator 2 characteristics, parameter dThreshold/dt, replaced any occurrence of "VREF+" by "V <sub>REFINT</sub> "Updated Table 63: LQPF100 14 x 14 mm, 100-pin low-profile quad flat package mechanical data, Table 64: LQFP64 10 x 10 mm 64-pin low-profile quad flat package mechanical data, Table 65: LQFP48 7 x 7 mm, 48-pin low-profile quad flat package mechanical data and Table 66: UFQFPN48 7 x 7 mm, 0.5 mm pitch, ultra thin fine-pitch quad flat no-lead package mechanical data. Updated Figure 33: LQFP100 recommended footprint. Updated Figure 46: TFBGA64 - 5.0x5.0x1.2 mm, 0.5 mm pitch, thin fine-pitch ball grid array package outline title. Remove minimum and typical values of A dimension in Table 67: UFBGA100 7 x 7 x 0.6 mm 0.5 mm pitch, ultra thin fine-pitch ball grid array package mechanical data Deleted second footnote in Figure 42: UFQFPN48 recommended footprint. Updated Section 8: Ordering information title and added first sentence. Changed BOR disabled option identifier in Table 72: Ordering information scheme.
22-Jul-2014	10	Updated <i>Figure 14</i> , <i>Figure 15</i> . Updated <i>Table 5</i> . Updated <i>Figure 6.3.4</i> . Updated note <i>5</i> inside <i>Table 54</i> . Updated Ro value inside <i>Table 54</i> .

Table 73.	Document revision history (continued)

