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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, Cap Sense, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 20x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l152rbt6

List of figures

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channels' independent or simultaneous conversions
- DMA capability for each channel (including the underrun interrupt)
- external triggers for conversion
- input reference voltage V_{REF+}

Eight DAC trigger inputs are used in the STM32L151x6/8/B and STM32L152x6/8/B devices. The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

3.12 Ultra-low-power comparators and reference voltage

The STM32L151x6/8/B and STM32L152x6/8/B devices embed two comparators sharing the same current bias and reference voltage. The reference voltage can be internal or external (coming from an I/O).

- one comparator with fixed threshold
- one comparator with rail-to-rail inputs, fast or slow mode. The threshold can be one of the following:
  - DAC output
  - External I/O
  - Internal reference voltage (V_{REFINT}) or V_{REFINT} submultiple (1/4, 1/2, 3/4)

Both comparators can wake up from Stop mode, and be combined into a window comparator.

The internal reference voltage is available externally via a low power / low current output buffer (driving current capability of 1 µA typical).

3.13 Routing interface

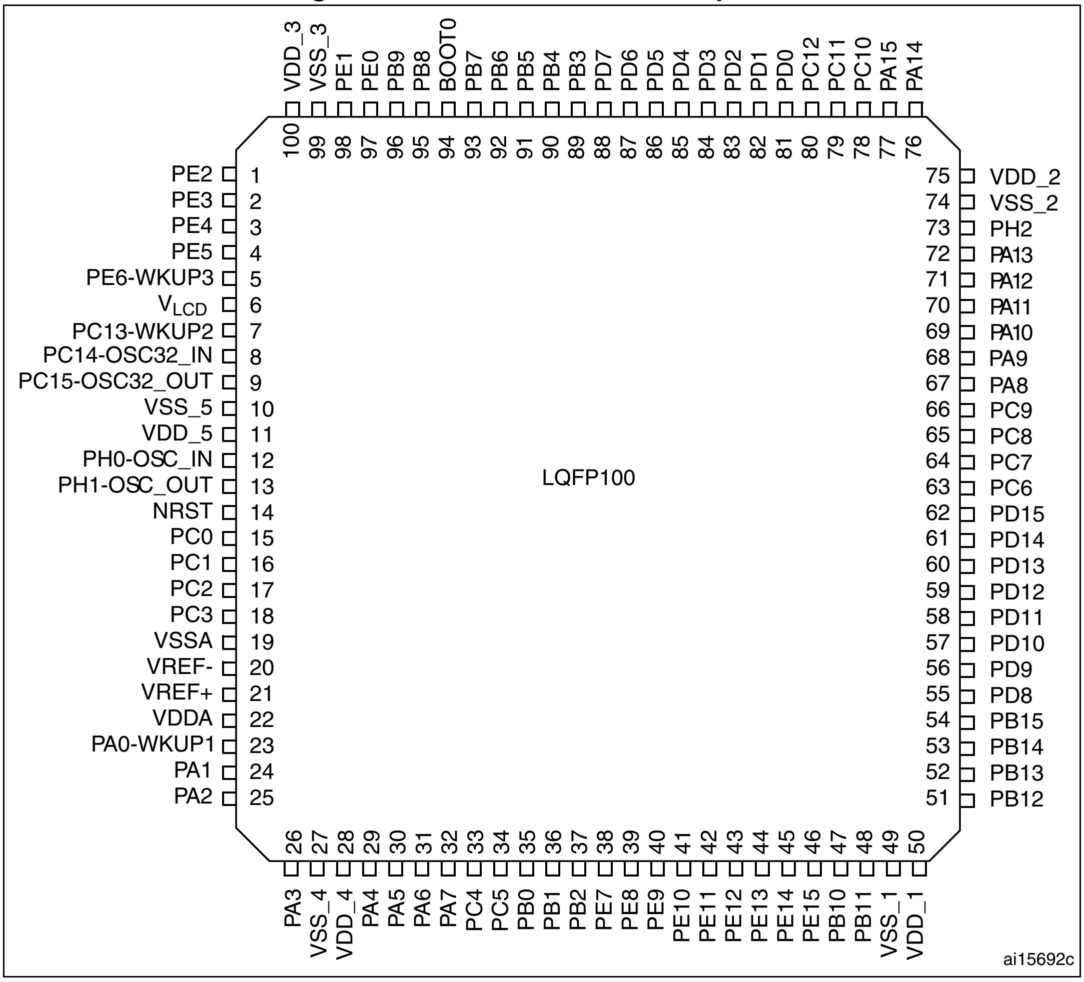
This interface controls the internal routing of I/Os to TIM2, TIM3, TIM4 and to the comparator and reference voltage output.

3.14 Touch sensing

The STM32L151x6/8/B and STM32L152x6/8/B devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 20 capacitive sensing channels distributed over 10 analog I/O groups. Only software capacitive sensing acquisition mode is supported.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (glass, plastic, ...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven

Figure 4. STM32L15xVx LQFP100 pinout



1. This figure shows the package top view.

Table 14. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD0}	Programmable voltage detector threshold 0	Falling edge	1.8	1.85	1.88	V
		Rising edge	1.88	1.94	1.99	
V_{PVD1}	PVD threshold 1	Falling edge	1.98	2.04	2.09	
		Rising edge	2.08	2.14	2.18	
V_{PVD2}	PVD threshold 2	Falling edge	2.20	2.24	2.28	
		Rising edge	2.28	2.34	2.38	
V_{PVD3}	PVD threshold 3	Falling edge	2.39	2.44	2.48	
		Rising edge	2.47	2.54	2.58	
V_{PVD4}	PVD threshold 4	Falling edge	2.57	2.64	2.69	
		Rising edge	2.68	2.74	2.79	
V_{PVD5}	PVD threshold 5	Falling edge	2.77	2.83	2.88	
		Rising edge	2.87	2.94	2.99	
V_{PVD6}	PVD threshold 6	Falling edge	2.97	3.05	3.09	
		Rising edge	3.08	3.15	3.20	
V_{hyst}	Hysteresis voltage	BOR0 threshold	-	40	-	mV
		All BOR and PVD thresholds excepting BOR0	-	100	-	

1. Guaranteed by characterization results.
2. Valid for device version without BOR at power up. Please see option "T" in Ordering information scheme for more details.

Table 24. Peripheral current consumption[(1)] (continued)

<table>
<tr><th colspan="2" rowspan="2">Peripheral</th><th colspan="4">Typical consumption, V_{DD} = 3.0 V, T_A = 25 °C</th><th rowspan="2">Unit</th></tr>
<tr><th>Range 1, V_{CORE}=1.8 V VOS[1:0] = 01</th><th>Range 2, V_{CORE}=1.5 V VOS[1:0] = 10</th><th>Range 3, V_{CORE}=1.2 V VOS[1:0] = 11</th><th>Low power sleep and run</th></tr>
<tr><td rowspan="9">AHB</td><td>GPIOA</td><td>5</td><td>4.5</td><td>3.5</td><td>4</td><td rowspan="10">µA/MHz (f_{HCLK})</td></tr>
<tr><td>GPIOB</td><td>5</td><td>4.5</td><td>3.5</td><td>4.5</td></tr>
<tr><td>GPIOC</td><td>5</td><td>4.5</td><td>3.5</td><td>4.5</td></tr>
<tr><td>GPIOD</td><td>5</td><td>4.5</td><td>3.5</td><td>4.5</td></tr>
<tr><td>GPIOE</td><td>5</td><td>4.5</td><td>3.5</td><td>4.5</td></tr>
<tr><td>GPIOH</td><td>4</td><td>4</td><td>3</td><td>3.5</td></tr>
<tr><td>CRC</td><td>1</td><td>0.5</td><td>0.5</td><td>0.5</td></tr>
<tr><td>FLASH</td><td>13</td><td>11.5</td><td>9</td><td>18.5</td></tr>
<tr><td>DMA1</td><td>12</td><td>10</td><td>8</td><td>10.5</td></tr>
<tr><td colspan="2">All enabled</td><td>166</td><td>138</td><td>106</td><td>130</td></tr>
<tr><td colspan="2">$I_{DD (RTC)}$</td><td colspan="4">0.47</td><td rowspan="9">µA</td></tr>
<tr><td colspan="2">$I_{DD (LCD)}$</td><td colspan="4">3.1</td></tr>
<tr><td colspan="2">$I_{DD (ADC)}$[(3)]</td><td colspan="4">1450</td></tr>
<tr><td colspan="2">$I_{DD (DAC)}$[(4)]</td><td colspan="4">340</td></tr>
<tr><td colspan="2">$I_{DD (COMP1)}$</td><td colspan="4">0.16</td></tr>
<tr><td rowspan="2">$I_{DD (COMP2)}$</td><td>Slow mode</td><td colspan="4">2</td></tr>
<tr><td>Fast mode</td><td colspan="4">5</td></tr>
<tr><td colspan="2">$I_{DD (PVD / BOR)}$[(5)]</td><td colspan="4">2.6</td></tr>
<tr><td colspan="2">$I_{DD (IWDG)}$</td><td colspan="4">0.25</td></tr>
</table>

1. Data based on differential I_{DD} measurement between all peripherals OFF an one peripheral with clock enabled, in the following conditions: f_{HCLK} = 32 MHz (Range 1), f_{HCLK} = 16 MHz (Range 2), f_{HCLK} = 4 MHz (Range 3), f_{HCLK} = 64kHz (Low power run/sleep), f_{APB1} = f_{HCLK}, f_{APB2} = f_{HCLK}, default prescaler value for each peripheral. The CPU is in Sleep mode in both cases. No I/O pins toggling.
2. HSI oscillator is OFF for this measure.
3. Data based on a differential I_{DD} measurement between ADC in reset configuration and continuous ADC conversion (HSI consumption not included).
4. Data based on a differential I_{DD} measurement between DAC in reset configuration and continuous DAC conversion of $V_{DD}/2$. DAC is in buffered mode, output is left floating.
5. Including supply current of internal reference voltage.

6.3.7 Internal clock source characteristics

The parameters given in the following table are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 13*.

High-speed internal (HSI) RC oscillator

Table 30. HSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	V_{DD} = 3.0 V	-	16	-	MHz
TRIM(1)(2)	HSI user-trimmed resolution	Trimming code is not a multiple of 16	-	±0.4	0.7	%
		Trimming code is a multiple of 16	-	-	±1.5	%
ACC_{HSI}(2)	Accuracy of the factory-calibrated HSI oscillator	V_{DDA} = 3.0 V, T_A = 25 °C	-1(3)	-	1(3)	%
		V_{DDA} = 3.0 V, T_A = 0 to 55 °C	-1.5	-	1.5	%
		V_{DDA} = 3.0 V, T_A = -10 to 70 °C	-2	-	2	%
		V_{DDA} = 3.0 V, T_A = -10 to 85 °C	-2.5	-	2	%
		V_{DDA} = 3.0 V, T_A = -10 to 105 °C	-4	-	2	%
		V_{DDA} = 1.65 V to 3.6 V T_A = -40 to 105 °C	-4	-	3	%
$t_{SU(HSI)}$(2)	HSI oscillator startup time	-	-	3.7	6	µs
$I_{DD(HSI)}$(2)	HSI oscillator power consumption	-	-	100	140	µA

1. The trimming step differs depending on the trimming code. It is usually negative on the codes which are multiples of 16 (0x00, 0x10, 0x20, 0x30...0xE0).
2. Guaranteed by characterization results.
3. Tested in production.

Low-speed internal (LSI) RC oscillator

Table 31. LSI oscillator characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}(1)	LSI frequency	26	38	56	kHz
D_{LSI}(2)	LSI oscillator frequency drift 0°C ≤ T_A ≤ 85°C	-10	-	4	%
$t_{su(LSI)}$(3)	LSI oscillator startup time	-	-	200	µs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	400	510	nA

1. Tested in production.
2. This is a deviation for an individual part, once the initial frequency has been measured.
3. Guaranteed by design.

6.3.9 Memory characteristics

The characteristics are given at T_A = -40 to 105 °C unless otherwise specified.

RAM memory

Table 34. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VRM	Data retention mode(1)	STOP mode (or RESET)	1.65	-	-	V

1. Minimum supply voltage without losing data stored in RAM (in Stop mode or under Reset) or in hardware registers (only in Stop mode).

Flash memory and data EEPROM

Table 35. Flash memory and data EEPROM characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
V_{DD}	Operating voltage Read / Write / Erase	-	1.65	-	3.6	V
t_{prog}	Programming / erasing time for byte / word / double word / half-page	Erasing	-	3.28	3.94	ms
		Programming	-	3.28	3.94	
I_{DD}	Average current during whole program/erase operation	T_A = 25 °C, V_{DD} = 3.6 V	-	300	-	µA
	Maximum current (peak) during program/erase operation		-	1.5	2.5	mA

1. Guaranteed by design.

Table 36. Flash memory, data EEPROM endurance and data retention

Symbol	Parameter	Conditions	Value			Unit
			Min(1)	Typ	Max	
NCYC(2)	Cycling (erase / write) Program memory	T_A = -40°C to 105 °C	10	-	-	kcycles
	Cycling (erase / write) EEPROM data memory		300	-	-	
t_{RET}(2)	Data retention (program memory) after 10 kcycles at T_A = 85 °C	TRET = +85 °C	30	-	-	years
	Data retention (EEPROM data memory) after 300 kcycles at T_A = 85 °C		30	-	-	
	Data retention (program memory) after 10 kcycles at T_A = 105 °C	TRET = +105 °C	10	-	-	
	Data retention (EEPROM data memory) after 300 kcycles at T_A = 105 °C		10	-	-	

1. Guaranteed by characterization results.
2. Characterization is done according to JEDEC JESD22-A117.

6.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 37*. They are based on the EMS levels and classes defined in application note AN1709.

Table 37. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25 °C, f_{HCLK} = 32 MHz conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25 °C, f_{HCLK} = 32 MHz conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

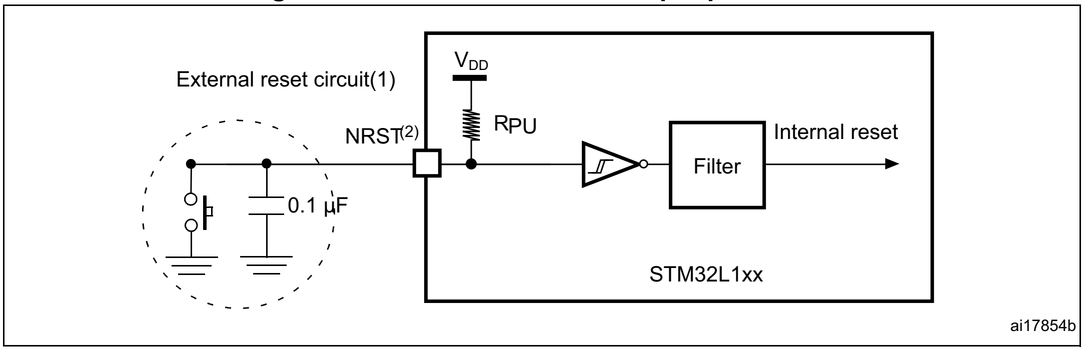
The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the oscillator pins for 1 second.

Figure 20. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 45*. Otherwise the reset will not be taken into account by the device.

6.3.15 TIM timer characteristics

The parameters given in *Table 46* are guaranteed by design.

Refer to *Section 6.3.13: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 46. TIMx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 32 MHz	31.25	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 32 MHz	0	16	MHz
Res_{TIM}	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected (timer's prescaler disabled)	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 32 MHz	0.0312	2048	µs
t_{MAX_COUNT}	Maximum possible count	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 32 MHz	-	134.2	s

1. TIMx is used as a general term to refer to the TIM2, TIM3 and TIM4 timers.

Table 51. USB DC electrical characteristics

Symbol	Parameter	Conditions	Min.(1)	Max.(1)	Unit
Input levels					
V_{DD}	USB operating voltage(2)	-	3.0	3.6	V
V_{DI}(3)	Differential input sensitivity	I(USB_DP, USB_DM)	0.2	-	V
V_{CM}(3)	Differential common mode range	Includes V_{DI} range	0.8	2.5	
V_{SE}(3)	Single ended receiver threshold	-	1.3	2.0	
Output levels					
V_{OL}(4)	Static output level low	R_L of 1.5 kΩ to 3.6 V(5)	-	0.3	V
V_{OH}(4)	Static output level high	R_L of 15 kΩ to V_{SS}(5)	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. To be compliant with the USB 2.0 full speed electrical specification, the USB_DP (D+) pin should be pulled up with a 1.5 kΩ resistor to a 3.0-to-3.6 V voltage range.
3. Guaranteed by characterization results.
4. Tested in production.
5. R_L is the load connected on the USB drivers.

Figure 25. USB timings: definition of data signal rise and fall time

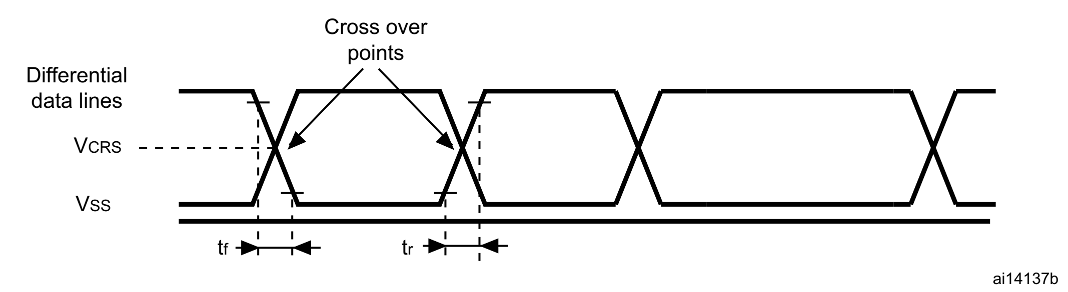


Table 52. USB: full speed electrical characteristics

Driver characteristics(1)					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_r	Rise time(2)	C_L = 50 pF	4	20	ns
t_f	Fall Time(2)	C_L = 50 pF	4	20	ns
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage		1.3	2.0	V

1. Guaranteed by design.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

Table 54. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_S	Sampling time(5)	Direct channels 2.4 V ≤ V_{DDA} ≤ 3.6 V	0.25	-	-	µs
		Multiplexed channels 2.4 V ≤ V_{DDA} ≤ 3.6 V	0.56	-	-	
		Direct channels 1.8 V ≤ V_{DDA} ≤ 2.4 V	0.56	-	-	
		Multiplexed channels 1.8 V ≤ V_{DDA} ≤ 2.4 V	1	-	-	
		-	4	-	384	$1/f_{ADC}$
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 16 MHz	1	-	24.75	µs
		-	4 to 384 (sampling phase) +12 (successive approximation)			$1/f_{ADC}$
C_{ADC}	Internal sample and hold capacitor	Direct channels	-	16	-	pF
		Multiplexed channels	-		-	
f_{TRIG}	External trigger frequency Regular sequencer	12-bit conversions	-	-	Tconv+1	$1/f_{ADC}$
		6/8/10-bit conversions	-	-	Tconv	$1/f_{ADC}$
f_{TRIG}	External trigger frequency Injected sequencer	12-bit conversions	-	-	Tconv+2	$1/f_{ADC}$
		6/8/10-bit conversions	-	-	Tconv+1	$1/f_{ADC}$
R_{AIN}	Signal source impedance(5)	-	-	-	50	κΩ
t_{lat}	Injection trigger conversion latency	f_{ADC} = 16 MHz	219	-	281	ns
		-	3.5	-	4.5	$1/f_{ADC}$
t_{latr}	Regular trigger conversion latency	f_{ADC} = 16 MHz	156	-	219	ns
		-	2.5	-	3.5	$1/f_{ADC}$
t_{STAB}	Power-up time	-	-	-	3.5	µs

1. The V_{REF+} input can be grounded iif neither the ADC nor the DAC are used (this allows to shut down an external voltage reference).
2. The current consumption through V_{REF} is composed of two parameters:
   - one constant (max 300 µA)
   - one variable (max 400 µA), only during sampling time + 2 first conversion pulses.
   So, peak consumption is 300+400 = 700 µA and average consumption is 300 + [(4 sampling + 2) /16] x 400 = 450 µA at 1Msps
3. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA}, depending on the package. Refer to *Section 4: Pin descriptions* for further details.
4. V_{SSA} must be tied to ground.
5. See *Table 56: Maximum source impedance RAIN max* for R_{AIN} limitation.

Table 57. DAC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
dOffset/dT[1]	Offset error temperature coefficient (code 0x800)	V_{DDA} = 3.3V, T_A = 0 to 50 °C DAC output buffer OFF	-20	-10	0	µV/°C
		V_{DDA} = 3.3V, T_A = 0 to 50 °C DAC output buffer ON	0	20	50	
Gain[1]	Gain error[6]	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON	-	+0.1 / -0.2%	+0.2 / - 0.5%	%
		No R_{LOAD}, $C_L \leq 50$ pF DAC output buffer OFF	-	+0 / -0.2%	+0 / -0.4%	
dGain/dT[1]	Gain error temperature coefficient	V_{DDA} = 3.3V, T_A = 0 to 50 °C DAC output buffer OFF	-10	-2	0	µV/°C
		V_{DDA} = 3.3V, T_A = 0 to 50 °C DAC output buffer ON	-40	-8	0	
TUE[1]	Total unadjusted error	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON	-	12	30	LSB
		No R_{LOAD}, $C_L \leq 50$ pF DAC output buffer OFF	-	8	12	
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes till DAC_OUT reaches final value ±1LSB	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ	-	7	12	µs
Update rate	Max frequency for a correct DAC_OUT change (95% of final value) with 1 LSB variation in the input code	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ	-	-	1	Msps
t_{WAKEUP}	Wakeup time from off state (setting the ENx bit in the DAC Control register)[7]	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ	-	9	15	µs
PSRR+	V_{DDA} supply rejection ratio (static DC measurement)	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ	-	-60	-35	dB

1. Guaranteed by characterization results.
2. Difference between two consecutive codes - 1 LSB.
3. Difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095.
4. Difference between the value measured at Code (0x800) and the ideal value = V/2.
5. Difference between the value measured at Code (0x001) and the ideal value.
6. Difference between ideal slope of the transfer function and measured slope computed from code 0x000 and 0xFFF when buffer is OFF, and from code giving 0.2 V and (V_{DDA} – 0.2) V when buffer is ON.
7. In buffered mode, the output can overshoot above the final value for low input code (starting from min value).

6.3.21 LCD controller (STM32L152xx only)

The STM32L152xx embeds a built-in step-up converter to provide a constant LCD reference voltage independently from the V_{DD} voltage. An external capacitor C_{ext} must be connected to the V_{LCD} pin to decouple this converter.

Table 62. LCD controller characteristics

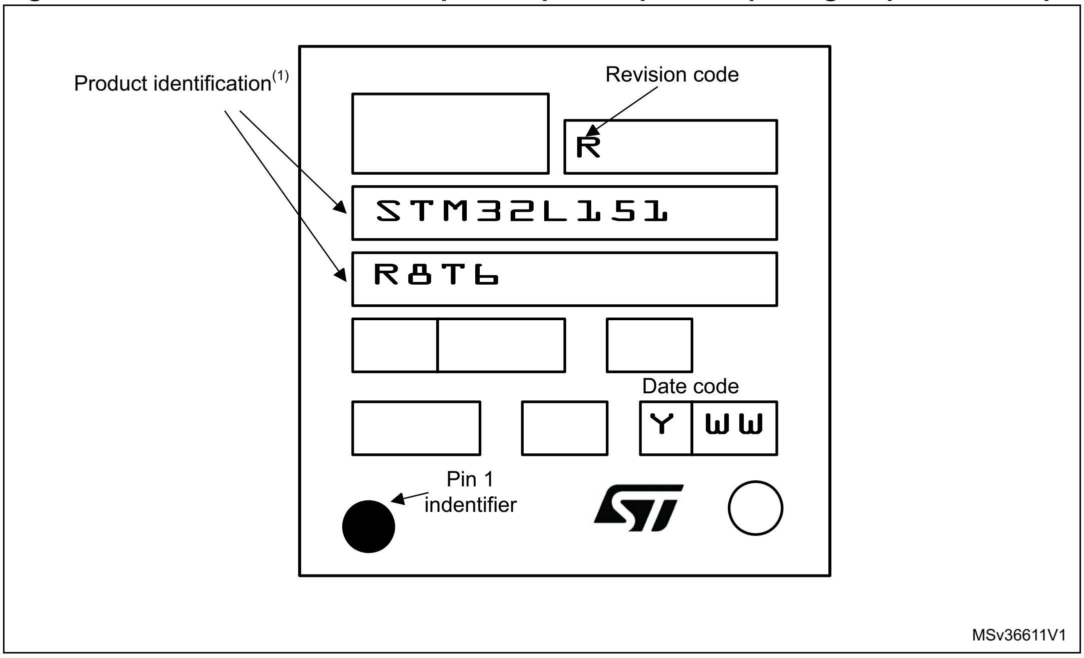
Symbol	Parameter	Min	Typ	Max	Unit
V_{LCD}	LCD external voltage	-	-	3.6	V
V_{LCD0}	LCD internal reference voltage 0	-	2.6	-	
V_{LCD1}	LCD internal reference voltage 1	-	2.73	-	
V_{LCD2}	LCD internal reference voltage 2	-	2.86	-	
V_{LCD3}	LCD internal reference voltage 3	-	2.98	-	
V_{LCD4}	LCD internal reference voltage 4	-	3.12	-	
V_{LCD5}	LCD internal reference voltage 5	-	3.26	-	
V_{LCD6}	LCD internal reference voltage 6	-	3.4	-	
V_{LCD7}	LCD internal reference voltage 7	-	3.55	-	
C_{ext}	V_{LCD} external capacitance	0.1	-	2	µF
I_{LCD}(1)	Supply current at V_{DD} = 2.2 V	-	3.3	-	µA
	Supply current at V_{DD} = 3.0 V	-	3.1	-	
R_{Htot}(2)	Low drive resistive network overall value	5.28	6.6	7.92	MΩ
R_L(2)	High drive resistive network total value	192	240	288	kΩ
V_{44}	Segment/Common highest level voltage	-	-	V_{LCD}	V
V_{34}	Segment/Common 3/4 level voltage	-	3/4 V_{LCD}	-	V
V_{23}	Segment/Common 2/3 level voltage	-	2/3 V_{LCD}	-	
V_{12}	Segment/Common 1/2 level voltage	-	1/2 V_{LCD}	-	
V_{13}	Segment/Common 1/3 level voltage	-	1/3 V_{LCD}	-	
V_{14}	Segment/Common 1/4 level voltage	-	1/4 V_{LCD}	-	
V_0	Segment/Common lowest level voltage	0	-	-	
ΔVxx(3)	Segment/Common level voltage error T_A = -40 to 85 °C	-	-	±50	mV

1. LCD enabled with 3 V internal step-up active, 1/8 duty, 1/4 bias, division ratio= 64, all pixels active, no LCD connected
2. Guaranteed by design.
3. Guaranteed by characterization results.

LQFP64 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

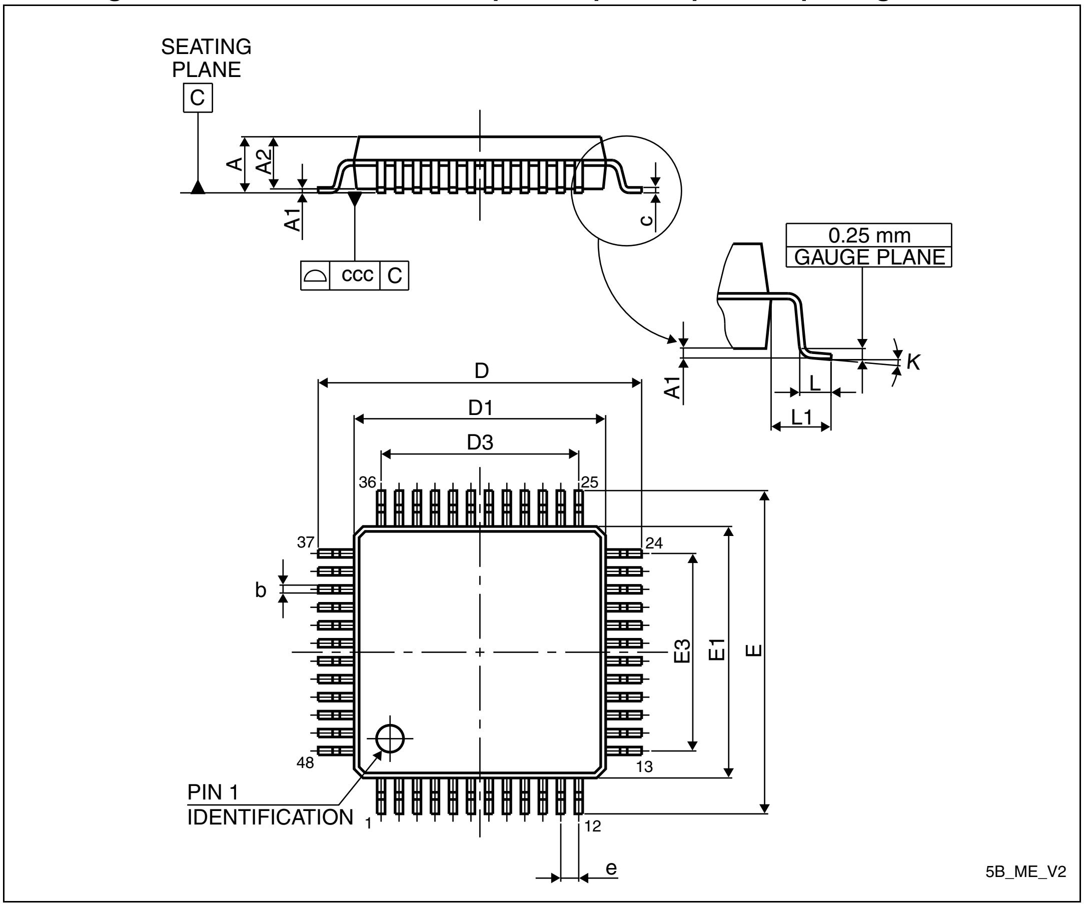
Figure 37. LQFP64 10 x 10 mm, 64-pin low-profile quad flat package top view example



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.3 LQFP48 7 x 7 mm, 48-pin low-profile quad flat package information

Figure 38. LQFP48 7 x 7 mm, 48-pin low-profile quad flat package outline

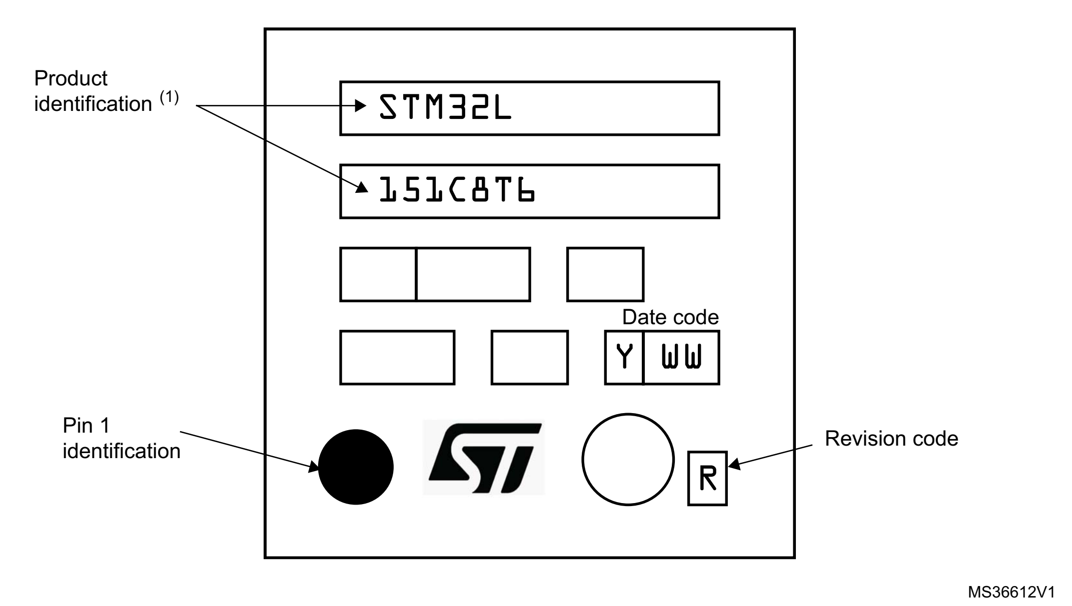


1. Drawing is not to scale.

LQFP48 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 40. LQFP48 7 x 7 mm, 48-pin low-profile quad flat package top view example



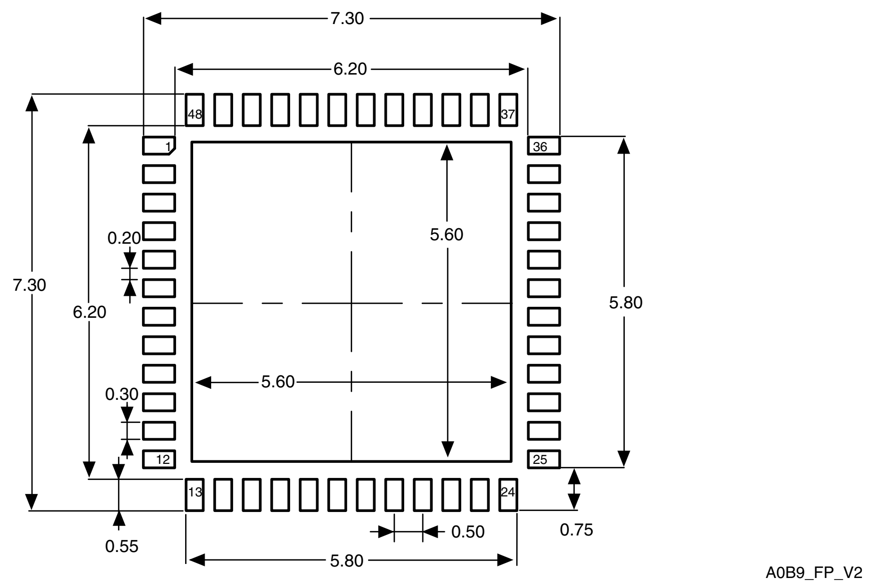
1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 66. UFQFPN48 7 x 7 mm, 0.5 mm pitch, package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

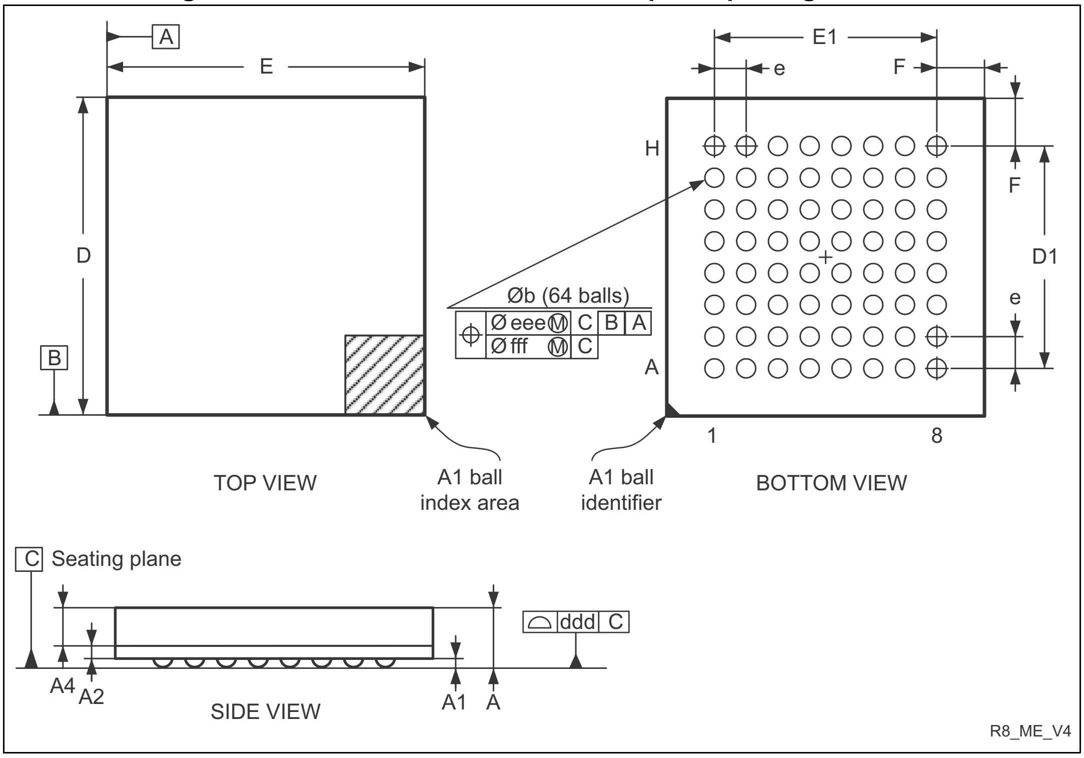
Figure 42. UFQFPN48 7 x 7 mm, 0.5 mm pitch, package recommended footprint



1. Dimensions are in millimeters.

7.6 TFBGA64 5 x 5 mm, 0.5 mm pitch, thin fine-pitch ball grid array package information

Figure 47. TFBGA64 5 x 5 mm, 0.5 mm pitch, package outline



1. Drawing is not to scale.

Table 69. TFBGA64 5 x 5 mm, 0.5 mm pitch, package mechanical data

Symbol	millimeters			inches[(1)]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.200	-	-	0.0472
A1	0.150	-	-	0.0059	-	-
A2	-	0.200	-	-	0.0079	-
A4	-	-	0.600	-	-	0.0236
b	0.250	0.300	0.350	0.0098	0.0118	0.0138
D	4.850	5.000	5.150	0.1909	0.1969	0.2028
D1	-	3.500	-	-	0.1378	-
E	4.850	5.000	5.150	0.1909	0.1969	0.2028
E1	-	3.500	-	-	0.1378	-
e	-	0.500	-	-	0.0197	-
F	-	0.750	-	-	0.0295	-
ddd	-	-	0.080	-	-	0.0031

Table 69. TFBGA64 5 x 5 mm, 0.5 mm pitch, package mechanical data (continued)

Symbol	millimeters			inches[(1)]		
	Min	Typ	Max	Min	Typ	Max
eee	-	-	0.15	-	-	0.0059
fff	-	-	0.05	-	-	0.002

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 48. TFBGA64, 5 x 5 mm, 0.5 mm pitch, recommended footprint

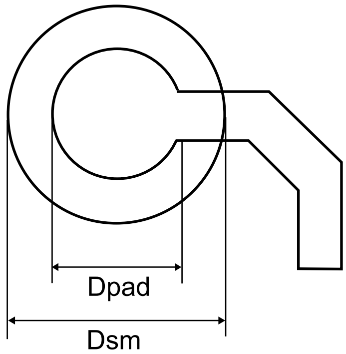


Table 70. TFBGA64 5 x 5 mm, 0.5 mm pitch, recommended PCB design rules

Dimension	Recommended values
Pitch	0.5
Dpad	0.27 mm
Dsm	0.35 mm typ. (depends on the soldermask registration tolerance)
Solder paste	0.27 mm aperture diameter.

Table 73. Document revision history (continued)

Date	Revision	Changes
26-Oct-2012	7	Updated cover page. Updated *Section 3.10: ADC (analog-to-digital converter)* Updated *Table 3: Functionalities depending on the operating power supply range*, added *Table 4: CPU frequency range depending on dynamic voltage scaling* and *Table 5: Working mode-dependent functionalities (from Run/active down to standby)*. Updated *Table 27: Low-speed external user clock characteristics*Added footnote *2.* in *Table 14: Embedded reset and power control block characteristics* Updated *Table 22: Typical and maximum current consumptions in Stop mode* and *Table 23: Typical and maximum current consumptions in Standby mode* Updated footnote *4.* in *Table 22: Typical and maximum current consumptions in Stop mode* Updated *Table 44: I/O AC characteristics* Updated *Table 47: I2C characteristics* Updated *Table 49: SPI characteristics* Updated *Section 6.3.9: Memory characteristics* Updated “non-robust” *Table 54: ADC characteristics* Removed the note “position of 4.7 µf capacitor” in *Section 6.1.6: Power supply scheme* Updated *Table 66: UFQFPN48 7 x 7 mm, 0.5 mm pitch, ultra thin fine-pitch quad flat no-lead package mechanical data* Updated *Table 65: LQFP48 7 x 7 mm, 48-pin low-profile quad flat package mechanical data* Added the resistance of TFBGA in *Table 71: Thermal characteristics* Added *Figure 50: Thermal resistance*
07-Feb-2013	8	Removed AHB1/AHB2 in *Figure 1: Ultralow power STM32L15xx6/8/B block diagram* Added IWDG and WWDG rows in *Table 5: Working mode-dependent functionalities (from Run/active down to standby)*. Updated I_{DD} (Supply current during wakeup time from Standby mode) in *Table 23: Typical and maximum current consumptions in Standby mode* The comment "HSE = 16 MHz(2) (PLL ON for fHCLK above 16 MHz)" replaced by "fHSE = fHCLK up to 16 MHz included, fHSE = fHCLK/2 above 16 MHz (PLL ON)(2)” in *Table 19: Current consumption in Sleep mode* Updated Stop mode current to 1.2 µA in *Ultra-low-power platform* Updated entire *Section 7: Package information* Removed alternate function “I2C2_SMBA” for GPIO pin “PH2” in *Table 8: STM32L15xx6/8/B pin definitions* Updated *Table 27: Low-speed external user clock characteristics* and definition of symbol “R_{AIN}” in *Table 54: ADC characteristics* Removed first sentence in *I2C interface characteristics*