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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 32MHz |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART, USB |
| Peripherals | Cap Sense, DMA, I²S, LCD, POR, PWM, WDT |
| Number of I/O | 83 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 4K x 8 |
| RAM Size | 10K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.65V ~ 3.6V |
| Data Converters | A/D 24x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l152v8t6tr |

# 2 Description

The ultra-low-power STM32L151x6/8/B and STM32L152x6/8/B devices incorporate the connectivity power of the universal serial bus (USB) with the high-performance ARM® Cortex®-M3 32-bit RISC core operating at 32 MHz frequency (33.3 DMIPS), a memory protection unit (MPU), high-speed embedded memories (Flash memory up to 128 Kbytes and RAM up to 16 Kbytes) and an extensive range of enhanced I/Os and peripherals connected to two APB buses.

All the devices offer a 12-bit ADC, 2 DACs and 2 ultra-low-power comparators, six general-purpose 16-bit timers and two basic timers, which can be used as time bases.

Moreover, the STM32L151x6/8/B and STM32L152x6/8/B devices contain standard and advanced communication interfaces: up to two $I^2C$s and SPIs, three USARTs and a USB. The STM32L151x6/8/B and STM32L152x6/8/B devices offer up to 20 capacitive sensing channels to simply add touch sensing functionality to any application.

They also include a real-time clock and a set of backup registers that remain powered in Standby mode.

Finally, the integrated LCD controller (except STM32L151x6/8/B devices) has a built-in LCD voltage generator that allows to drive up to 8 multiplexed LCDs with contrast independent of the supply voltage.

The ultra-low-power STM32L151x6/8/B and STM32L152x6/8/B devices operate from a 1.8 to 3.6 V power supply (down to 1.65 V at power down) with BOR and from a 1.65 to 3.6 V power supply without BOR option. It is available in the -40 to +85 °C temperature range, extended to 105°C in low power dissipation state. A comprehensive set of power-saving modes allows the design of low-power applications.


## 3.1 Low power modes

The ultra-low-power STM32L151x6/8/B and STM32L152x6/8/B devices support dynamic voltage scaling to optimize its power consumption in run mode. The voltage from the internal low-drop regulator that supplies the logic can be adjusted according to the system's maximum operating frequency and the external voltage supply:

- In Range 1 ($V_{DD}$ range limited to 1.71-3.6 V), the CPU runs at up to 32 MHz (refer to *Table 17* for consumption).
- In Range 2 (full $V_{DD}$ range), the CPU runs at up to 16 MHz (refer to *Table 17* for consumption)
- In Range 3 (full $V_{DD}$ range), the CPU runs at up to 4 MHz (generated only with the multispeed internal RC oscillator clock source). Refer to *Table 17* for consumption.

Seven low power modes are provided to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

  Sleep mode power consumption: refer to *Table 19*.

- **Low power run** mode

  This mode is achieved with the multispeed internal (MSI) RC oscillator set to the minimum clock (65 kHz), execution from SRAM or Flash memory, and internal regulator in low power mode to minimize the regulator's operating current. In the Low power run mode, the clock frequency and the number of enabled peripherals are both limited.

  Low power run mode consumption: refer to *Table 20: Current consumption in Low power run mode*.

- **Low power sleep** mode

  This mode is achieved by entering the Sleep mode with the internal voltage regulator in Low power mode to minimize the regulator's operating current. In the Low power sleep mode, both the clock frequency and the number of enabled peripherals are limited; a typical example would be to have a timer running at 32 kHz.
  When wakeup is triggered by an event or an interrupt, the system reverts to the run mode with the regulator on.

  Low power sleep mode consumption: refer to *Table 21: Current consumption in Low power sleep mode*.

- **Stop** mode with RTC

  Stop mode achieves the lowest power consumption while retaining the RAM and register contents and real time clock. All clocks in the $V_{CORE}$ domain are stopped, the PLL, MSI RC, HSI RC and HSE crystal oscillators are disabled. The LSE or LSI is still running. The voltage regulator is in the low power mode.

  The device can be woken up from Stop mode by any of the EXTI line, in 8 µs. The EXTI line source can be one of the 16 external lines. It can be the PVD output, the Comparator 1 event or Comparator 2 event (if internal reference voltage is on), it can be the RTC alarm(s), the USB wakeup, the RTC tamper events, the RTC timestamp event or the RTC wakeup.

- **Stop** mode without RTC

  Stop mode achieves the lowest power consumption while retaining the RAM and register contents. All clocks are stopped, the PLL, MSI RC, HSI and LSI RC, LSE and

implementation based on a surface charge transfer acquisition principle. It consists of charging the sensor capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. The capacitive sensing acquisition only requires few external components to operate.

Reliable touch sensing functionality can be quickly and easily implemented using the free STM32L1xx STMTouch touch sensing firmware library.

## 3.15 Timers and watchdogs

The ultra-low-power STM32L151x6/8/B and STM32L152x6/8/B devices include six general-purpose timers, two basic timers and two watchdog timers.

*Table 6* compares the features of the general-purpose and basic timers.

**Table 6. Timer feature comparison**

| Timer | Counter resolution | Counter type | Prescaler factor | DMA request generation | Capture/compare channels | Complementary outputs |
|---|---|---|---|---|---|---|
| TIM2, TIM3, TIM4 | 16-bit | Up, down, up/down | Any integer between 1 and 65536 | Yes | 4 | No |
| TIM9 | 16-bit | Up | Any integer between 1 and 65536 | No | 2 | No |
| TIM10, TIM11 | 16-bit | Up | Any integer between 1 and 65536 | No | 1 | No |
| TIM6, TIM7 | 16-bit | Up | Any integer between 1 and 65536 | Yes | 0 | No |

Table 8. STM32L151x6/8/B and STM32L152x6/8/B pin definitions (continued)

| Pins | | | | | Pin name | Pin type(1) | I/O structure | Main function(2) (after reset) | Pins functions | |
|---|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | LQFP64 | TFBGA64 | UFBGA100 | LQFP48 or UFQFPN48 | | | | | Alternate functions | Additional functions |
| 35 | 26 | F5 | M5 | 18 | PB0 | I/O | TC | PB0 | TIM3_CH3/LCD_SEG5 | ADC_IN8/ COMP1_INP/ VREF_OUT |
| 36 | 27 | G5 | M6 | 19 | PB1 | I/O | FT | PB1 | TIM3_CH4/LCD_SEG6 | ADC_IN9/ COMP1_INP/ VREF_OUT |
| 37 | 28 | G6 | L6 | 20 | PB2 | I/O | FT | PB2/BOOT1 | BOOT1 | - |
| 38 | - | - | M7 | - | PE7 | I/O | TC | PE7 | - | ADC_IN22/ COMP1_INP |
| 39 | - | - | L7 | - | PE8 | I/O | TC | PE8 | - | ADC_IN23/ COMP1_INP |
| 40 | - | - | M8 | - | PE9 | I/O | TC | PE9 | TIM2_CH1_ETR | ADC_IN24/ COMP1_INP |
| 41 | - | - | L8 | - | PE10 | I/O | TC | PE10 | TIM2_CH2 | ADC_IN25/ COMP1_INP |
| 42 | - | - | M9 | - | PE11 | I/O | FT | PE11 | TIM2_CH3 | - |
| 43 | - | - | L9 | - | PE12 | I/O | FT | PE12 | TIM2_CH4/SPI1_NSS | - |
| 44 | - | - | M10 | - | PE13 | I/O | FT | PE13 | SPI1_SCK | - |
| 45 | - | - | M11 | - | PE14 | I/O | FT | PE14 | SPI1_MISO | - |
| 46 | - | - | M12 | - | PE15 | I/O | FT | PE15 | SPI1_MOSI | - |
| 47 | 29 | G7 | L10 | 21 | PB10 | I/O | FT | PB10 | I2C2_SCL/USART3_TX/ TIM2_CH3/LCD_SEG10 | - |
| 48 | 30 | H7 | L11 | 22 | PB11 | I/O | FT | PB11 | I2C2_SDA/USART3_RX/ TIM2_CH4/LCD_SEG11 | - |
| 49 | 31 | D6 | F12 | 23 | $V_{SS\_1}$ | S | - | $V_{SS\_1}$ | - | - |
| 50 | 32 | E6 | G12 | 24 | $V_{DD\_1}$ | S | - | $V_{DD\_1}$ | - | - |
| 51 | 33 | H8 | L12 | 25 | PB12 | I/O | FT | PB12 | SPI2_NSS/I2C2_SMBA/ USART3_CK/ LCD_SEG12/TIM10_CH1 | ADC_IN18/ COMP1_INP |
| 52 | 34 | G8 | K12 | 26 | PB13 | I/O | FT | PB13 | SPI2_SCK/USART3_CTS/ LCD_SEG13/ TIM9_CH1 | ADC_IN19/ COMP1_INP |

Table 8. STM32L151x6/8/B and STM32L152x6/8/B pin definitions (continued)

| Pins | | | | | Pin name | Pin type(1) | I/O structure | Main function(2) (after reset) | Pins functions | |
|---|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | LQFP64 | TFBGA64 | UFBGA100 | LQFP48 or UFQFPN48 | | | | | Alternate functions | Additional functions |
| 71 | 45 | B8 | A12 | 33 | PA12 | I/O | FT | PA12 | USART1_RTS/ SPI1_MOSI | USB_DP |
| 72 | 46 | A8 | A11 | 34 | PA13 | I/O | FT | JTMS-SWDIO | JTMS-SWDIO | - |
| 73 | - | - | C11 | - | PH2 | I/O | FT | PH2 | - | - |
| 74 | 47 | D5 | F11 | 35 | $V_{SS\_2}$ | S | - | $V_{SS\_2}$ | - | - |
| 75 | 48 | E5 | G11 | 36 | $V_{DD\_2}$ | S | - | $V_{DD\_2}$ | - | - |
| 76 | 49 | A7 | A10 | 37 | PA14 | I/O | FT | JTCK -SWCLK | JTCK-SWCLK | - |
| 77 | 50 | A6 | A9 | 38 | PA15 | I/O | FT | JTDI | TIM2_CH1_ETR/PA15/ SPI1_NSS/ LCD_SEG17 | - |
| 78 | 51 | B7 | B11 | - | PC10 | I/O | FT | PC10 | USART3_TX/LCD_SEG28 /LCD_SEG40/LCD_COM4 | - |
| 79 | 52 | B6 | C10 | - | PC11 | I/O | FT | PC11 | USART3_RX/LCD_SEG29 /LCD_SEG41/LCD_COM5 | - |
| 80 | 53 | C5 | B10 | - | PC12 | I/O | FT | PC12 | USART3_CK/LCD_SEG30 /LCD_SEG42/LCD_COM6 | - |
| 81 | - | - | C9 | - | PD0 | I/O | FT | PD0 | SPI2_NSS/TIM9_CH1 | - |
| 82 | - | - | B9 | - | PD1 | I/O | FT | PD1 | SPI2_SCK | - |
| 83 | 54 | B5 | C8 | - | PD2 | I/O | FT | PD2 | TIM3_ETR/LCD_SEG31/ LCD_SEG43/LCD_COM7 | - |
| 84 | - | - | B8 | - | PD3 | I/O | FT | PD3 | USART2_CTS/ SPI2_MISO | - |
| 85 | - | - | B7 | - | PD4 | I/O | FT | PD4 | USART2_RTS/ SPI2_MOSI | - |
| 86 | - | - | A6 | - | PD5 | I/O | FT | PD5 | USART2_TX | - |
| 87 | - | - | B6 | - | PD6 | I/O | FT | PD6 | USART2_RX | - |
| 88 | - | - | A5 | - | PD7 | I/O | FT | PD7 | USART2_CK/TIM9_CH2 | - |
| 89 | 55 | A5 | A8 | 39 | PB3 | I/O | FT | JTDO | TIM2_CH2/PB3/ SPI1_SCK/LCD_SEG7/ JTDO | COMP2_INM |

## Table 9. Alternate function input/output

| Port name | Digital alternate function number | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | AFIO0 | AFIO1 | AFIO2 | AFIO3 | AFIO4 | AFIO5 | AFOI6 | AFIO7 | AFIO8 | AFIO9 | AFIO11 | AFIO12 | AFIO13 | AFIO14 | AFIO15 |
| | Alternate function | | | | | | | | | | | | | | |
| | SYSTEM | TIM2 | TIM3/4 | TIM9/10/11 | I2C1/2 | SPI1/2 | N/A | USART1/2/3 | N/A | N/A | LCD | N/A | N/A | RI | SYSTEM |
| BOOT0 | BOOT0 | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| NRST | NRST | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| PA0-WKUP1 | - | TIM2_CH1_ETR | - | - | - | - | - | USART2_CTS | - | - | - | - | - | TIMx_IC1 | EVENTOUT |
| PA1 | - | TIM2_CH2 | - | - | - | - | - | USART2_RTS | - | - | [SEG0] | - | - | TIMx_IC2 | EVENTOUT |
| PA2 | - | TIM2_CH3 | - | TIM9_CH1 | - | - | - | USART2_TX | - | - | [SEG1] | - | - | TIMx_IC3 | EVENTOUT |
| PA3 | - | TIM2_CH4 | - | TIM9_CH2 | - | - | - | USART2_RX | - | - | [SEG2] | - | - | TIMx_IC4 | EVENTOUT |
| PA4 | - | - | - | - | - | SPI1_NSS | - | USART2_CK | - | - | - | - | - | TIMx_IC1 | EVENTOUT |
| PA5 | - | TIM2_CH1_ETR | - | - | - | SPI1_SCK | - | - | - | - | - | - | - | TIMx_IC2 | EVENTOUT |
| PA6 | - | - | TIM3_CH1 | TIM10_CH1 | - | SPI1_MISO | - | - | - | - | [SEG3] | - | - | TIMx_IC3 | EVENTOUT |
| PA7 | - | - | TIM3_CH2 | TIM11_CH1 | - | SPI1_MOSI | - | - | - | - | [SEG4] | - | - | TIMx_IC4 | EVENTOUT |
| PA8 | MCO | - | - | - | - | - | - | USART1_CK | - | - | [COM0] | - | - | TIMx_IC1 | EVENTOUT |
| PA9 | - | - | - | - | - | - | - | USART1_TX | - | - | [COM1] | - | - | TIMx_IC2 | EVENTOUT |
| PA10 | - | - | - | - | - | - | - | USART1_RX | - | - | [COM2] | - | - | TIMx_IC3 | EVENTOUT |
| PA11 | - | - | - | - | - | SPI1_MISO | - | USART1_CTS | - | - | - | - | - | TIMx_IC4 | EVENTOUT |
| PA12 | - | - | - | - | - | SPI1_MOSI | - | USART1_RTS | - | - | - | - | - | TIMx_IC1 | EVENTOUT |
| PA13 | JTMS-SWDIO | - | - | - | - | - | - | - | - | - | - | - | - | TIMx_IC2 | EVENTOUT |
| PA14 | JTCK-SWCLK | - | - | - | - | - | - | - | - | - | - | - | - | TIMx_IC3 | EVENTOUT |
| PA15 | JTDI | TIM2_CH1_ETR | - | - | - | SPI1_NSS | - | - | - | - | SEG17 | - | - | TIMx_IC4 | EVENTOUT |
| PB0 | - | - | TIM3_CH3 | - | - | - | - | - | - | - | [SEG5] | - | - | - | EVENTOUT |
| PB1 | - | - | TIM3_CH4 | - | - | - | - | - | - | - | [SEG6] | - | - | - | EVENTOUT |
| PB2 | BOOT1 | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| PB3 | JTDO | TIM2_CH2 | - | - | - | SPI1_SCK | - | - | - | - | [SEG7] | - | - | - | EVENTOUT |
| PB4 | NJTRST | - | TIM3_CH1 | - | - | SPI1_MISO | - | - | - | - | [SEG8] | - | - | - | EVENTOUT |

**Table 19. Current consumption in Sleep mode**

| Symbol | Parameter | Conditions | | $f_{HCLK}$ | Typ | Max(1) | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | 55 °C | 85 °C | 105 °C | |
| $I_{DD}$ (Sleep) | Supply current in Sleep mode, code executed from RAM, Flash switched OFF | $f_{HSE}$ = $f_{HCLK}$ up to 16 MHz included, $f_{HSE}$ = $f_{HCLK}$/2 above 16 MHz (PLL ON)(2) | Range 3, $V_{CORE}$=1.2 V VOS[1:0] = 11 | 1 MHz | 80 | 140 | 140 | 140 | µA |
| | | | | 2 MHz | 150 | 210 | 210 | 210 | |
| | | | | 4 MHz | 280 | 330 | 330 | 330(3) | |
| | | | Range 2, $V_{CORE}$=1.5 V VOS[1:0] = 10 | 4 MHz | 280 | 400 | 400 | 400 | |
| | | | | 8 MHz | 450 | 550 | 550 | 550 | |
| | | | | 16 MHz | 900 | 1050 | 1050 | 1050 | |
| | | | Range 1, $V_{CORE}$=1.8 V VOS[1:0] = 01 | 8 MHz | 550 | 650 | 650 | 650 | |
| | | | | 16 MHz | 1050 | 1200 | 1200 | 1200 | |
| | | | | 32 MHz | 2300 | 2500 | 2500 | 2500 | |
| | | HSI clock source (16 MHz) | Range 2, $V_{CORE}$=1.5 V VOS[1:0] = 10 | 16 MHz | 1000 | 1100 | 1100 | 1100 | |
| | | | Range 1, $V_{CORE}$=1.8 V VOS[1:0] = 01 | 32 MHz | 2300 | 2500 | 2500 | 2500 | |
| | | MSI clock, 65 kHz | Range 3, $V_{CORE}$=1.2 V VOS[1:0] = 11 | 65 kHz | 30 | 50 | 50 | 60 | |
| | | MSI clock, 524 kHz | | 524 kHz | 50 | 70 | 70 | 80 | |
| | | MSI clock, 4.2 MHz | | 4.2 MHz | 200 | 240 | 240 | 250 | |
| | Supply current in Sleep mode, code executed from Flash | $f_{HSE}$ = $f_{HCLK}$ up to 16 MHz included, $f_{HSE}$ = $f_{HCLK}$/2 above 16 MHz (PLL ON)(2) | Range 3, $V_{CORE}$=1.2 V VOS[1:0] = 11 | 1 MHz | 80 | 140 | 140 | 140 | µA |
| | | | | 2 MHz | 150 | 210 | 210 | 210 | |
| | | | | 4 MHz | 290 | 350 | 350 | 350 | |
| | | | Range 2, $V_{CORE}$=1.5 V VOS[1:0] = 10 | 4 MHz | 300 | 400 | 400 | 400 | |
| | | | | 8 MHz | 500 | 600 | 600 | 600 | |
| | | | | 16 MHz | 1000 | 1100 | 1100 | 1100 | |
| | | | Range 1, $V_{CORE}$=1.8 V VOS[1:0] = 01 | 8 MHz | 550 | 650 | 650 | 650 | |
| | | | | 16 MHz | 1050 | 1200 | 1200 | 1200 | |
| | | | | 32 MHz | 2300 | 2500 | 2500 | 2500 | |
| | | HSI clock source (16 MHz) | Range 2, $V_{CORE}$=1.5 V VOS[1:0] = 10 | 16 MHz | 1000 | 1100 | 1100 | 1100 | |
| | | | Range 1, $V_{CORE}$=1.8 V VOS[1:0] = 01 | 32 MHz | 2300 | 2500 | 2500 | 2500 | |

**Table 20. Current consumption in Low power run mode**

| Symbol | Parameter | Conditions | | | Typ | Max (1) | Unit |
|---|---|---|---|---|---|---|---|
| $I_{DD\ (LP\ Run)}$ | Supply current in Low power run mode | All peripherals OFF, code executed from RAM, Flash switched OFF, $V_{DD}$ from 1.65 V to 3.6 V | MSI clock, 65 kHz $f_{HCLK}$ = 32 kHz | $T_A$ = -40 °C to 25 °C | 9 | 12 | µA |
| | | | | $T_A$ = 85 °C | 17.5 | 24 | |
| | | | | $T_A$ = 105 °C | 31 | 46 | |
| | | | MSI clock, 65 kHz $f_{HCLK}$ = 65 kHz | $T_A$ = -40 °C to 25 °C | 14 | 17 | |
| | | | | $T_A$ = 85 °C | 22 | 29 | |
| | | | | $T_A$ = 105 °C | 35 | 51 | |
| | | | MSI clock, 131 kHz $f_{HCLK}$ = 131 kHz | $T_A$ = -40 °C to 25 °C | 37 | 42 | |
| | | | | $T_A$ = 55 °C | 37 | 42 | |
| | | | | $T_A$ = 85 °C | 37 | 42 | |
| | | | | $T_A$ = 105 °C | 48 | 65 | |
| | | All peripherals OFF, code executed from Flash, $V_{DD}$ from 1.65 V to 3.6 V | MSI clock, 65 kHz $f_{HCLK}$ = 32 kHz | $T_A$ = -40 °C to 25 °C | 24 | 32 | |
| | | | | $T_A$ = 85 °C | 33 | 42 | |
| | | | | $T_A$ = 105 °C | 48 | 64 | |
| | | | MSI clock, 65 kHz $f_{HCLK}$ = 65 kHz | $T_A$ = -40 °C to 25 °C | 31 | 40 | |
| | | | | $T_A$ = 85 °C | 40 | 48 | |
| | | | | $T_A$ = 105 °C | 54 | 70 | |
| | | | MSI clock, 131 kHz $f_{HCLK}$ = 131 kHz | $T_A$ = -40 °C to 25 °C | 48 | 58 | |
| | | | | $T_A$ = 55 °C | 54 | 63 | |
| | | | | $T_A$ = 85 °C | 56 | 65 | |
| | | | | $T_A$ = 105 °C | 70 | 90 | |
| $I_{DD}$ Max (LP Run)(2) | Max allowed current in Low power run mode | $V_{DD}$ from 1.65 V to 3.6 V | - | - | - | 200 | |

1. Guaranteed by characterization results, unless otherwise specified.
2. This limitation is related to the consumption of the CPU core and the peripherals that are powered by the regulator. Consumption of the I/Os is not included in this limitation.

### 6.3.17 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 54* are guaranteed by design.

**Table 53. ADC clock frequency**

| Symbol | Parameter | Conditions | | | Min | Max | Unit |
|---|---|---|---|---|---|---|---|
| $f_{ADC}$ | ADC clock frequency | Voltage Range 1 & 2 | 2.4 V ≤$V_{DDA}$ ≤3.6 V | $V_{REF+}$ = $V_{DDA}$ | 0.480 | 16 | MHz |
| | | | | $V_{REF+}$ < $V_{DDA}$ $V_{REF+}$ > 2.4 V | | 8 | |
| | | | | $V_{REF+}$ < $V_{DDA}$ $V_{REF+}$ ≤2.4 V | | 4 | |
| | | | 1.8 V ≤$V_{DDA}$ ≤2.4 V | $V_{REF+}$ = $V_{DDA}$ | | 8 | |
| | | | | $V_{REF+}$ < $V_{DDA}$ | | 4 | |
| | | Voltage Range 3 | | | | 4 | |

**Table 54. ADC characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Power supply | - | 1.8 | - | 3.6 | V |
| $V_{REF+}$ | Positive reference voltage | 2.4 V ≤$V_{DDA}$ ≤3.6 V $V_{REF+}$ must be below or equal to $V_{DDA}$ | 1.8(1) | - | $V_{DDA}$ | V |
| $V_{REF-}$ | Negative reference voltage | - | - | $V_{SSA}$ | - | V |
| $I_{VDDA}$ | Current on the $V_{DDA}$ input pin | - | - | 1000 | 1450 | µA |
| $I_{VREF}$(2) | Current on the $V_{REF}$ input pin | Peak | - | 400 | 700 | µA |
| | | Average | - | | 450 | µA |
| $V_{AIN}$ | Conversion voltage range(3) | - | 0(4) | - | $V_{REF+}$ | V |
| $f_S$ | 12-bit sampling rate | Direct channels | 0.03 | - | 1 | Msps |
| | | Multiplexed channels | 0.03 | - | 0.76 | |
| | 10-bit sampling rate | Direct channels | 0.03 | - | 1.07 | Msps |
| | | Multiplexed channels | 0.03 | - | 0.8 | |
| | 8-bit sampling rate | Direct channels | 0.03 | - | 1.23 | Msps |
| | | Multiplexed channels | 0.03 | - | 0.89 | |
| | 6-bit sampling rate | Direct channels | 0.03 | - | 1.45 | Msps |
| | | Multiplexed channels | 0.03 | - | 1 | |

**Figure 26. ADC accuracy characteristics**

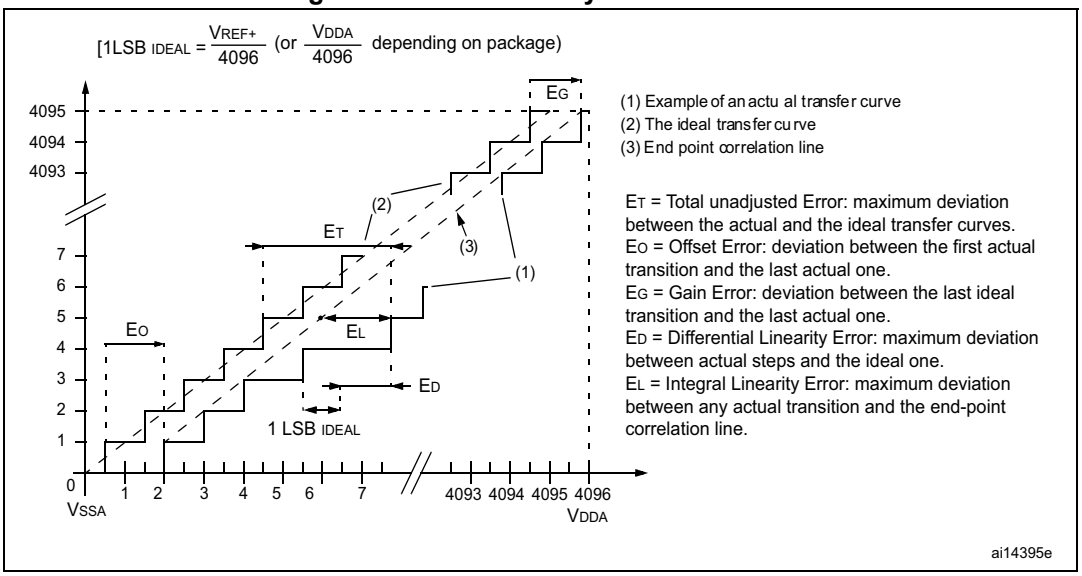
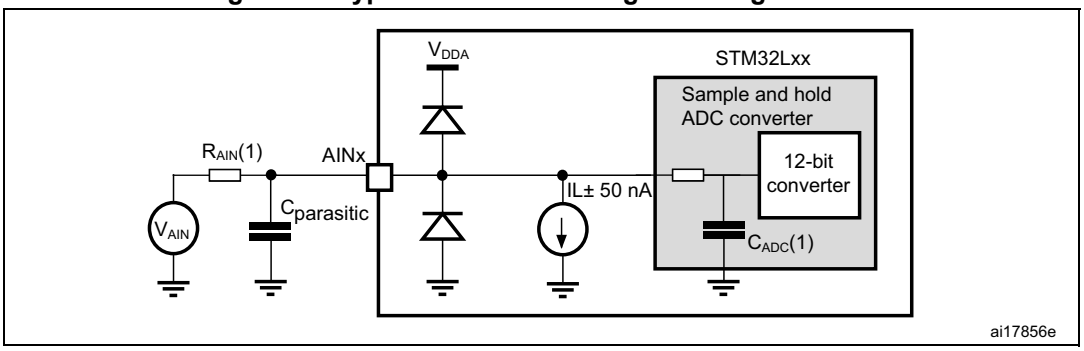



**Figure 27. Typical connection diagram using the ADC**



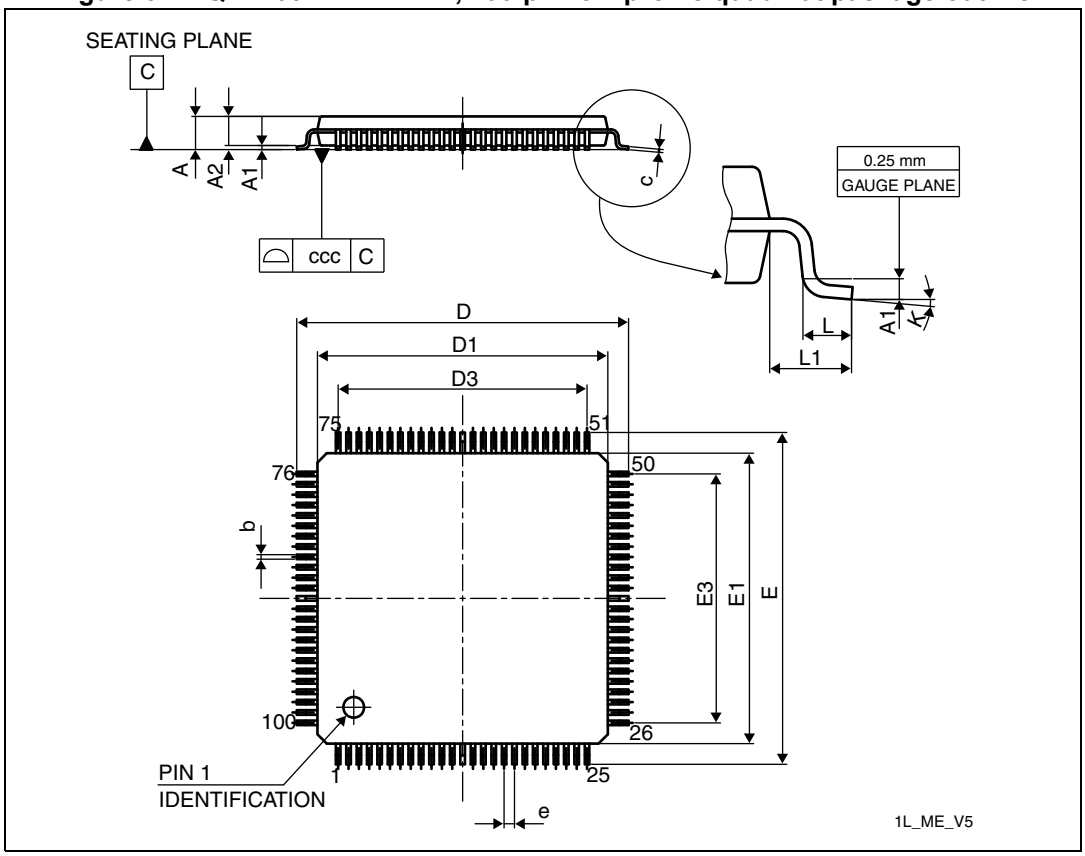

1. Refer to *Table 56: Maximum source impedance RAIN max* for the value of $R_{AIN}$ and *Table 54: ADC characteristics* for the value of CADC
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, $f_{ADC}$ should be reduced.

# 7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

## 7.1 LQFP100 14 x 14 mm, 100-pin low-profile quad flat package information

**Figure 32. LQFP100 14 x 14 mm, 100-pin low-profile quad flat package outline**

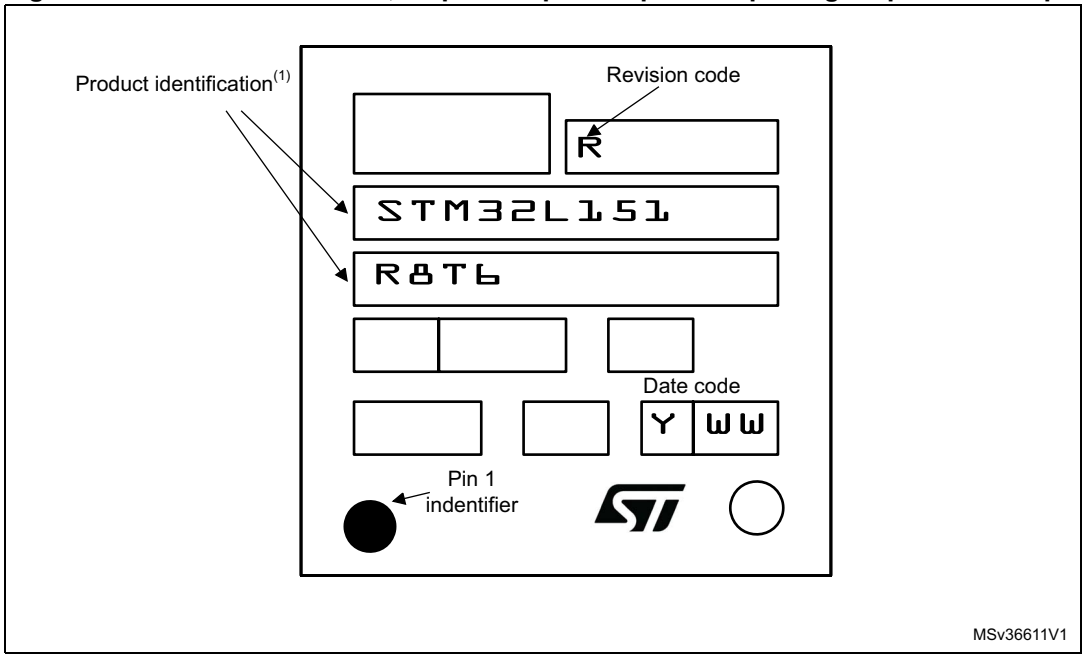



1. Drawing is not to scale.

### LQFP64 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

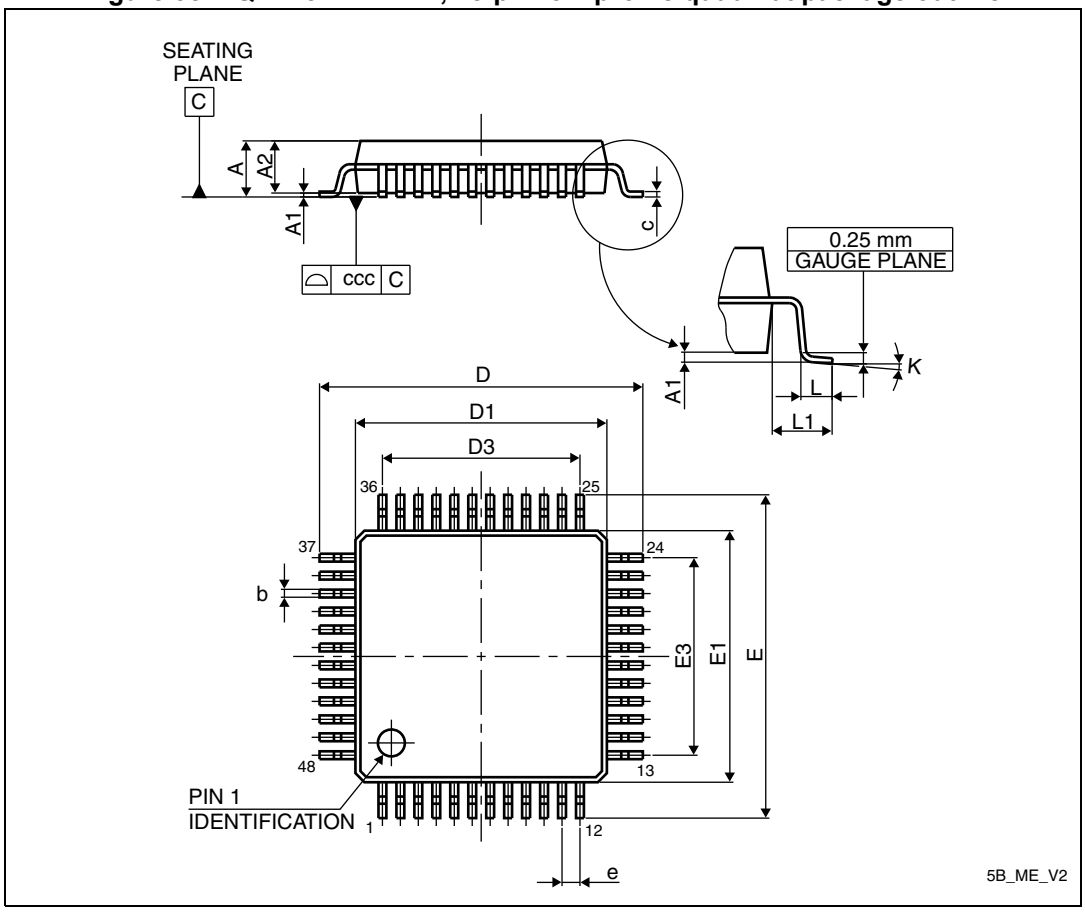
**Figure 37. LQFP64 10 x 10 mm, 64-pin low-profile quad flat package top view example**




1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

## 7.3 LQFP48 7 x 7 mm, 48-pin low-profile quad flat package information

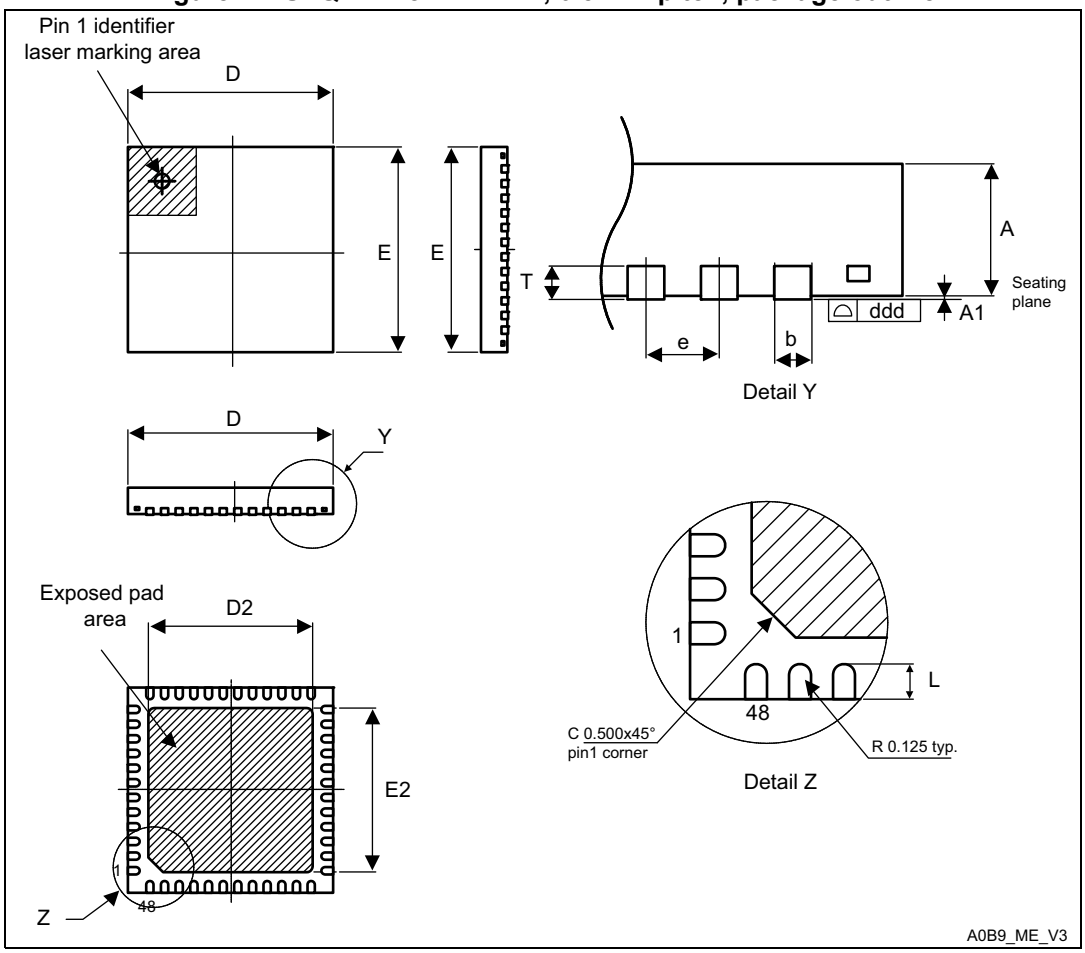
**Figure 38. LQFP48 7 x 7 mm, 48-pin low-profile quad flat package outline**




1. Drawing is not to scale.

## 7.4 UFQFPN48 7 x 7 mm, 0.5 mm pitch, package information

**Figure 41. UFQFPN48 7 x 7 mm, 0.5 mm pitch, package outline**




1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

**Table 67. UFBGA100 7 x 7 mm, 0.5 mm pitch, package mechanical data (continued)**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| eee | - | - | 0.15 | - | - | 0.0059 |
| fff | - | - | 0.05 | - | - | 0.002 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 45. UFBGA100 7 x 7 mm, 0.5 mm pitch, package recommended footprint**

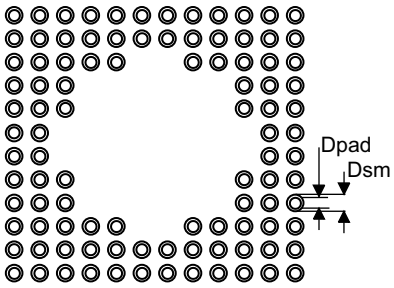



**Table 68. UFBGA100 7 x 7 mm, 0.5 mm pitch, recommended PCB design rules**

| Dimension | Recommended values |
|---|---|
| Pitch | 0.5 |
| Dpad | 0.280 mm |
| Dsm | 0.370 mm typ. (depends on the soldermask registration tolerance) |
| Stencil opening | 0.280 mm |
| Stencil thickness | Between 0.100 mm and 0.125 mm |

# 9 Revision history

Table 73. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 02-Jul-2010 | 1 | Initial release. |
| 01-Oct-2010 | 2 | Removed 5 V tolerance (FT) from PA3, PB0 and PC3 in *Table 8: STM32L15xx6/8/B pin definitions*<br>Updated *Table 14: Embedded reset and power control block characteristics*<br>Updated *Table 16: Embedded internal reference voltage*<br>Added *Table 53: ADC clock frequency*<br>Updated *Table 54: ADC characteristics* |
| 16-Dec-2010 | 3 | Modified consumptions on page 1 and in *Section 3.1: Low power modes*<br>LED_SEG8 removed on PB6.<br>Updated *Section 6: Electrical characteristics*<br>VFQFPN48 replaced by UFQFPN48 |
| 25-Feb-2011 | 4 | *Section 3.3.2: Power supply supervisor*: updated note.<br>*Table 8: STM32L15xx6/8/B pin definitions:* modified main function (after reset) and alternate function for OSC_IN and OSC_OUT pins; modified footnote 5; added footnote to OSC32_IN and OSC32_OUT pins; C1 and D1 removed on PD0 and PD1 pins (TFBGA64 column).<br>*Section 3.11: DAC (digital-to-analog converter)*: updated bullet list.<br>*Table 10: Voltage characteristics on page 52*: updated footnote 3 regarding $I_{INJ(PIN)}$.<br>*Table 11: Current characteristics on page 52*: updated footnote 4 regarding positive and negative injection.<br>*Table 14: Embedded reset and power control block characteristics on page 54*: updated typ and max values for $T_{RSTTEMPO}$ ($V_{DD}$ rising, BOR enabled).<br>*Table 17: Current consumption in Run mode, code with data processing running from Flash on page 58*: removed values for HSI clock source (16 MHz), Range 3.<br>*Table 18: Current consumption in Run mode, code with data processing running from RAM on page 59*: removed values for HSI clock source (16 MHz), Range 3.<br>*Table 19: Current consumption in Sleep mode on page 60* removed values for HSI clock source (16 MHz), Range 3 for both RAM and Flash; changed units.<br>*Table 20: Current consumption in Low power run mode on page 62*: updated parameter and max value of $I_{DD}$ Max (LP Run).<br>*Table 21: Current consumption in Low power sleep mode on page 63*: updated symbol, parameter, and max value of $I_{DD}$ Max (LP Sleep).<br>*Table 22: Typical and maximum current consumptions in Stop mode on page 64* updated values for $I_{DD\ (Stop\ with\ RTC)}$ - RTC clocked by LSE external clock (32.768 kHz), regulator in LP mode, HSI and HSE OFF (no independent watchdog). |

**Table 73. Document revision history (continued)**

| Date | Revision | Changes |
|---|---|---|
| 25-Feb-2011 | 4 (continued) | Updated *Table 23: Typical and maximum current consumptions in Standby mode on page 66* ($I_{DD}$ (WU from Standby) instead of ($I_{DD}$ (WU from Stop).<br>*Table 25: Low-power mode wakeup timings on page 69*: updated condition for Wakeup from Stop mode, regulator in Run mode; updated max values for Wakeup from Stop mode, regulator in low power mode; updated max values for $t_{WUSTDBY}$.<br>*Table 24: Peripheral current consumption on page 67*: updated values for column Low power sleep and run; updated Flash values; renamed ADC1 to ADC; updated $I_{DD\ (LCD)}$ value; updated units; added values for $I_{DD\ (RTC)}$ and $I_{DD\ (IWDG)}$; updated footnote 1 and 3; added foot note 2 concerning ADC.<br>*Table 26: High-speed external user clock characteristics on page 70*: added min value for $t_{w(HSE)}/t_{w(HSE)}$ OSC_IN high or low time; added max value for $t_{r(HSE)}/t_{f(HSE)}$ OSC_IN rise or fall time; updated $I_L$ for typ and max values.<br>*Table 27: Low-speed external user clock characteristics on page 71*: updated max value for $I_L$.<br>*Table 28: HSE oscillator characteristics on page 72*: renamed $i_2$ as $I_{HSE}$ and updated max value; updated max values for $I_{DD(HSE)}$.<br>*Table 29: LSE oscillator characteristics (fLSE = 32.768 kHz) on page 73*: updated max value for $I_{LSE}$.<br>*Table 30: HSI oscillator characteristics on page 75*: updated some min and max values for $ACC_{HSI}$.<br>*Table 32: MSI oscillator characteristics on page 76*: updated parameter, typ, and max values for $D_{VOLT(MSI)}$.<br>*Table 35: Flash memory and data EEPROM characteristics on page 78*: updated typ values for $t_{prog}$.<br>*Table 44: I/O AC characteristics on page 84*: updated some max values for 01, 10, and 11; updated min value; updated footnotes.<br>*Table 55: ADC accuracy on page 95*: updated typ values and some of the test conditions for ENOB, SINAD, SNR, and THD.<br>*Table 57: DAC characteristics on page 99*: updated footnote 7 and added footnote 8.<br>Updated leakage value in *Figure 27: Typical connection diagram using the ADC*.<br>Added *Figure 28: Maximum dynamic current consumption on VREF+ supply pin during ADC conversion*.<br>Added *Table 56: $R_{AIN}$ max for $f_{ADC}$ = 16 MHz on page 98*<br>*Figure 29: Power supply and reference decoupling (VREF+ not connected to VDDA)*: replaced all 10 nF capacitors with 100 nF capacitors.<br>*Figure 30: Power supply and reference decoupling (VREF+ connected to VDDA)*: replaced 10 nF capacitor with 100 nF capacitor. |