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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	C166SV2
Core Size	16/32-Bit
Speed	128MHz
Connectivity	CANbus, EBI/EMI, FlexRay, I ² C, LINbus, SPI, UART/USART
Peripherals	I ² S, POR, PWM, WDT
Number of I/O	118
Program Memory Size	1.06MB (1.06M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	90K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-144-13
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc2788x136f128lraakxuma1

2 General Device Information

The XC2788X series (16/32-Bit Single-Chip Microcontroller with 32-Bit Performance) is a part of the Infineon XC2000 Family of full-feature single-chip CMOS microcontrollers. These devices extend the functionality and performance of the C166 Family in terms of instructions (MAC unit), peripherals, and speed. They combine high CPU performance (up to 128 million instructions per second) with extended peripheral functionality and enhanced IO capabilities. Optimized peripherals can be adapted flexibly to meet the application requirements. These derivatives utilize clock generation via PLL and internal or external clock sources. On-chip memory modules include program Flash, program RAM, and data RAM.

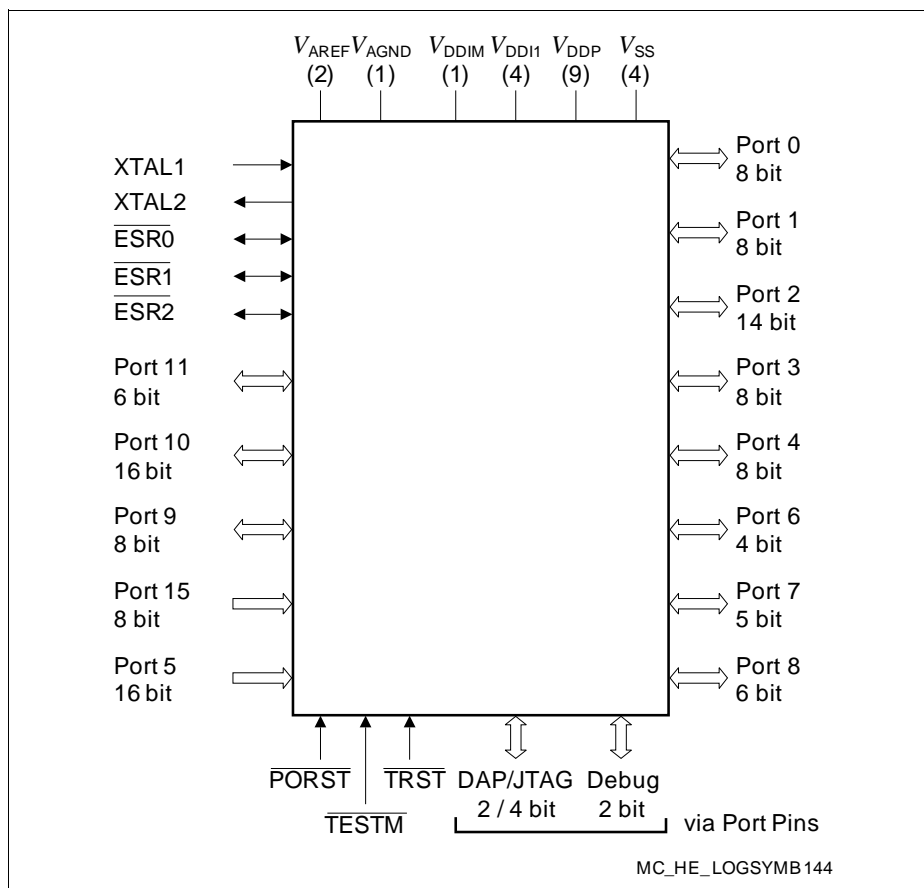


Figure 1 Logic Symbol

2.1 Pin Configuration and Definition

The pins of the XC2788X are described in detail in [Table 6](#), which includes all alternate functions. For further explanations please refer to the footnotes at the end of the table. The following figure summarizes all pins, showing their locations on the four sides of the package.

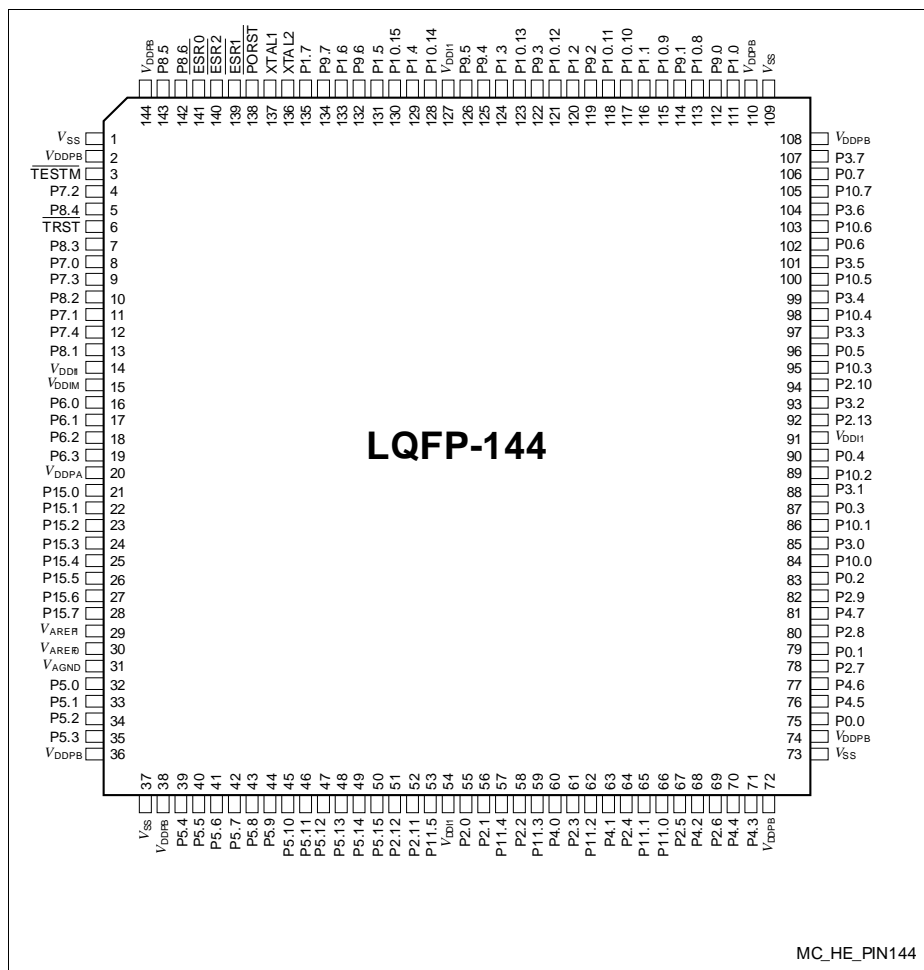


Figure 2 XC2788X Pin Configuration (top view)

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
25	P15.4	I	In/A	Bit 4 of Port 15, General Purpose Input
	ADC1_CH4	I	In/A	Analog Input Channel 4 for ADC1
	T6INA	I	In/A	GPT12E Timer T6 Count/Gate Input
26	P15.5	I	In/A	Bit 5 of Port 15, General Purpose Input
	ADC1_CH5	I	In/A	Analog Input Channel 5 for ADC1
	T6EUDA	I	In/A	GPT12E Timer T6 External Up/Down Control Input
27	P15.6	I	In/A	Bit 6 of Port 15, General Purpose Input
	ADC1_CH6	I	In/A	Analog Input Channel 6 for ADC1
28	P15.7	I	In/A	Bit 7 of Port 15, General Purpose Input
	ADC1_CH7	I	In/A	Analog Input Channel 7 for ADC1
29	V_{AREF1}	-	PS/A	Reference Voltage for A/D Converter ADC1
30	V_{AREF0}	-	PS/A	Reference Voltage for A/D Converter ADC0
31	V_{AGND}	-	PS/A	Reference Ground for A/D Converters ADC0/1
32	P5.0	I	In/A	Bit 0 of Port 5, General Purpose Input
	ADC0_CH0	I	In/A	Analog Input Channel 0 for ADC0
33	P5.1	I	In/A	Bit 1 of Port 5, General Purpose Input
	ADC0_CH1	I	In/A	Analog Input Channel 1 for ADC0
34	P5.2	I	In/A	Bit 2 of Port 5, General Purpose Input
	ADC0_CH2	I	In/A	Analog Input Channel 2 for ADC0
	TDI_A	I	In/A	JTAG Test Data Input
35	P5.3	I	In/A	Bit 3 of Port 5, General Purpose Input
	ADC0_CH3	I	In/A	Analog Input Channel 3 for ADC0
	T3INA	I	In/A	GPT12E Timer T3 Count/Gate Input

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
141	ESR0	O0 / I	St/B	External Service Request 0 After power-up, ESR0 operates as open-drain bidirectional reset with a weak pull-up.
	U1C0_DX0E	I	St/B	USIC1 Channel 0 Shift Data Input
	U1C0_DX2B	I	St/B	USIC1 Channel 0 Shift Control Input
142	P8.6	O0 / I	St/B	Bit 6 of Port 8, General Purpose Input/Output
	CCU60_COU T63	O1	St/B	CCU60 Channel 3 Output
	MCHK_MAT CH	O3	St/B	Memory Checker Match Output
	CCU60_CTR APB	I	St/B	CCU60 Emergency Trap Input
	BRKIN_D	I	St/B	OCDS Break Signal Input
	CCU62_CTR APD	I	St/B	CCU62 Emergency Trap Input
143	P8.5	O0 / I	St/B	Bit 5 of Port 8, General Purpose Input/Output
	CCU60_COU T62	O1	St/B	CCU60 Channel 2 Output
	CCU62_CC6 2	O2	St/B	CCU62 Channel 2 Output
	TCK_D	IH	St/B	DAP0/JTAG Clock Input If JTAG pos. D is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it.
	CCU62_CC6 2INB	I	St/B	CCU62 Channel 2 Input
15	V_{DDIM}	-	PS/M	Digital Core Supply Voltage for Domain M Decouple with a ceramic capacitor, see Data Sheet for details.
14, 54, 91, 127	V_{DDI1}	-	PS/1	Digital Core Supply Voltage for Domain 1 Decouple with a ceramic capacitor, see Data Sheet for details. All V_{DDI1} pins must be connected to each other.

Memory Content Protection

The contents of on-chip memories can be protected against soft errors (induced e.g. by radiation) by activating the parity mechanism or the Error Correction Code (ECC).

The parity mechanism can detect a single-bit error and prevent the software from using incorrect data or executing incorrect instructions.

The ECC mechanism can detect and automatically correct single-bit errors. This supports the stable operation of the system.

It is strongly recommended to activate the ECC mechanism wherever possible because this dramatically increases the robustness of an application against such soft errors.

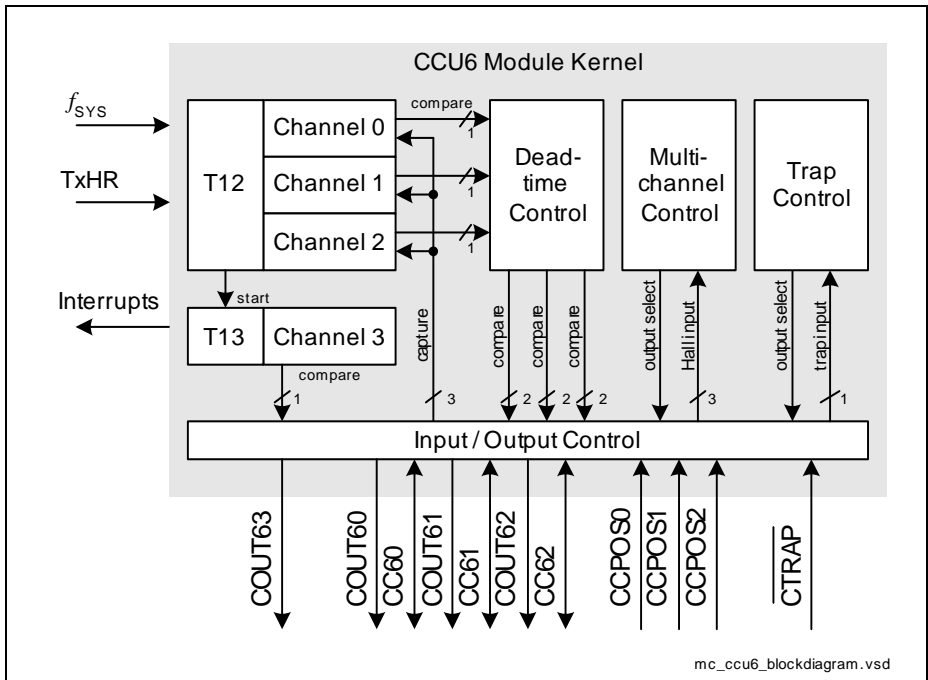


Figure 4 CCU6 Block Diagram

Timer T12 can work in capture and/or compare mode for its three channels. The modes can also be combined. Timer T13 can work in compare mode only. The multi-channel control unit generates output patterns that can be modulated by timer T12 and/or timer T13. The modulation sources can be selected and combined for signal modulation.

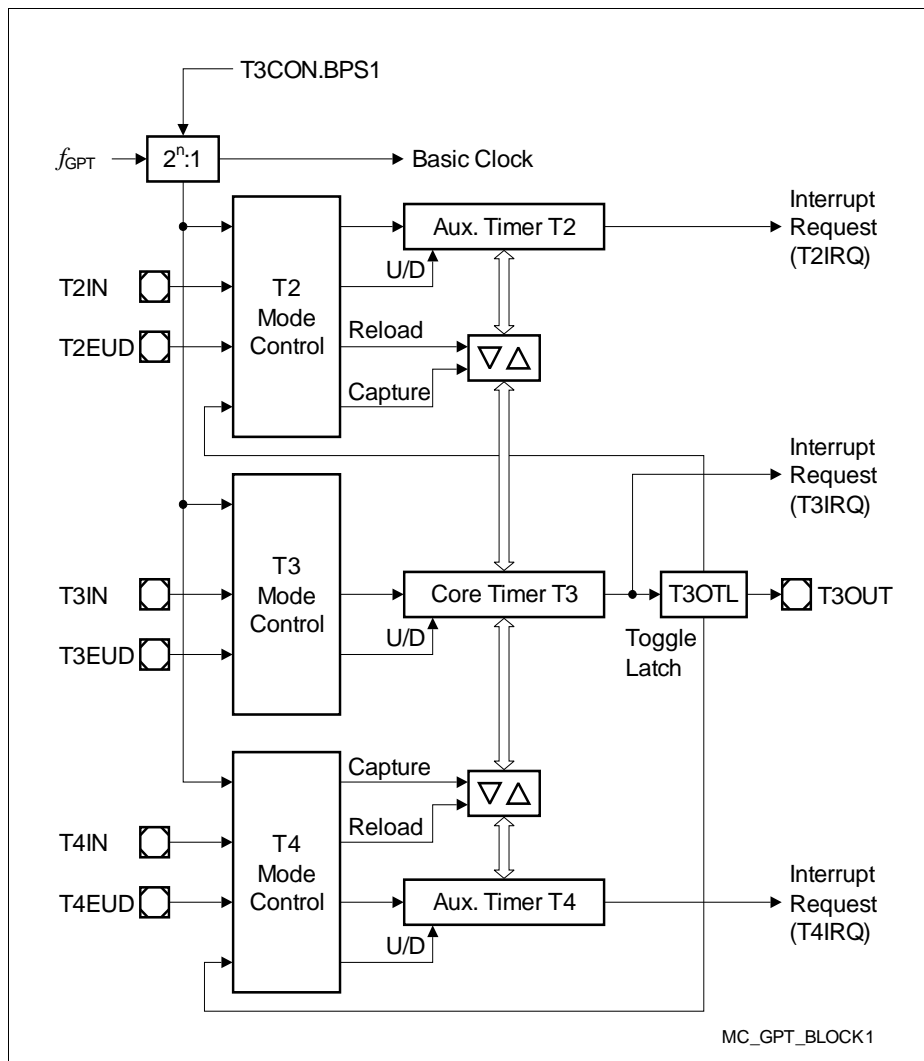


Figure 5 Block Diagram of GPT1

3.11 Real Time Clock

The Real Time Clock (RTC) module of the XC2788X can be clocked with a clock signal selected from internal sources or external sources (pins).

The RTC basically consists of a chain of divider blocks:

- Selectable 32:1 and 8:1 dividers (on - off)
- The reloadable 16-bit timer T14
- The 32-bit RTC timer block (accessible via registers RTCH and RTCL) consisting of:
 - a reloadable 10-bit timer
 - a reloadable 6-bit timer
 - a reloadable 6-bit timer
 - a reloadable 10-bit timer

All timers count up. Each timer can generate an interrupt request. All requests are combined to a common node request.

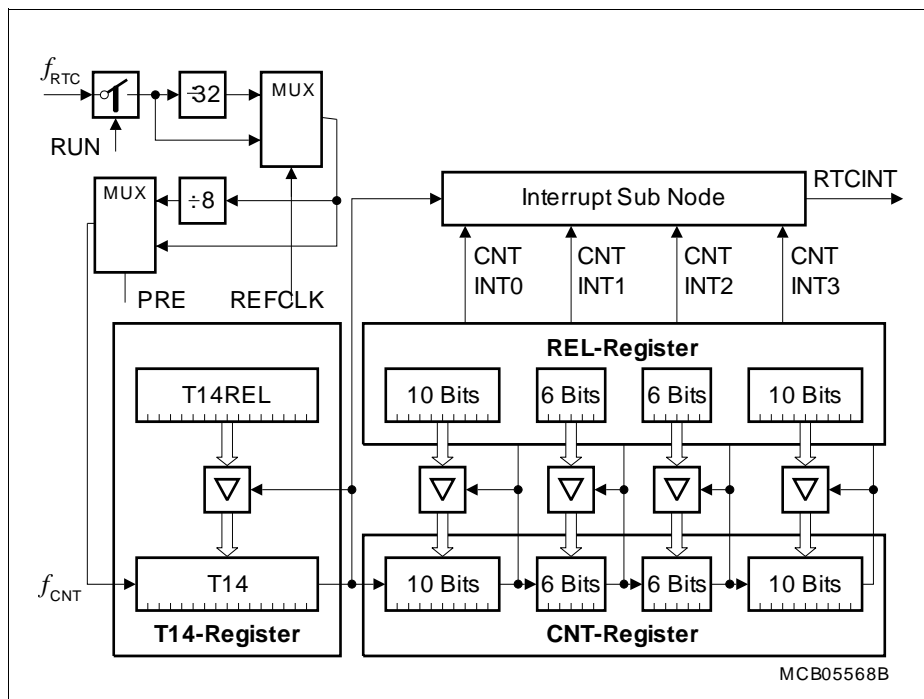


Figure 7 RTC Block Diagram

Note: The registers associated with the RTC are only affected by a power reset.

3.13 Universal Serial Interface Channel Modules (USIC)

The XC2788X features the USIC modules USIC0, USIC1, USIC2. Each module provides two serial communication channels.

The Universal Serial Interface Channel (USIC) module is based on a generic data shift and data storage structure which is identical for all supported serial communication protocols. Each channel supports complete full-duplex operation with a basic data buffer structure (one transmit buffer and two receive buffer stages). In addition, the data handling software can use FIFOs.

The protocol part (generation of shift clock/data/control signals) is independent of the general part and is handled by protocol-specific preprocessors (PPPs).

The USIC's input/output lines are connected to pins by a pin routing unit. The inputs and outputs of each USIC channel can be assigned to different interface pins, providing great flexibility to the application software. All assignments can be made during runtime.

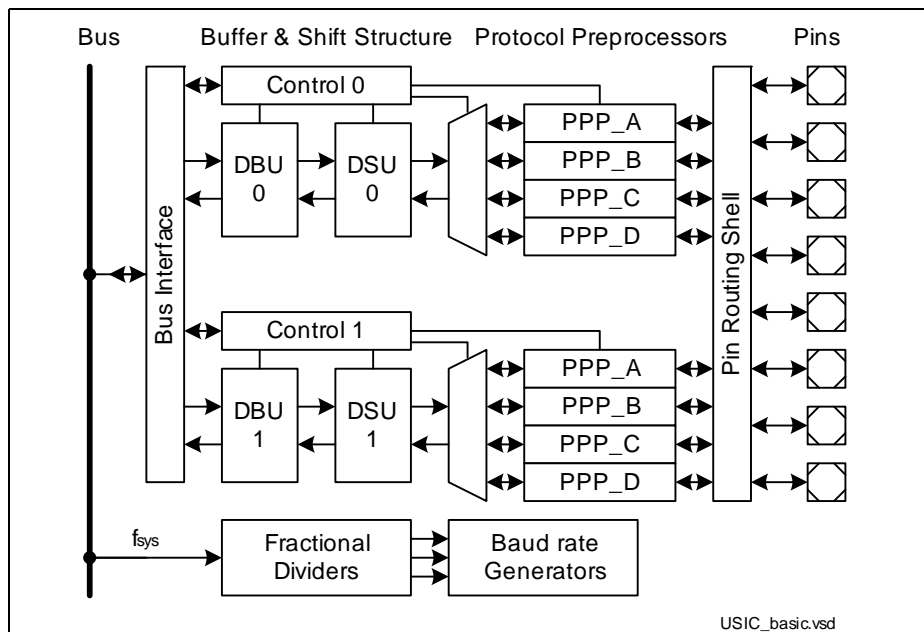


Figure 8 General Structure of a USIC Module

The regular structure of the USIC module brings the following advantages:

- Higher flexibility through configuration with same look-and-feel for data management
- Reduced complexity for low-level drivers serving different protocols
- Wide range of protocols with improved performances (baud rate, buffer handling)

4.2 DC Parameters

These parameters are static or average values that may be exceeded during switching transitions (e.g. output current).

Leakage current is strongly dependent on the operating temperature and the voltage level at the respective pin. The maximum values in the following tables apply under worst case conditions, i.e. maximum temperature and an input level equal to the supply voltage.

The value for the leakage current in an application can be determined by using the respective leakage derating formula (see tables) with values from that application.

The pads of the XC2788X are designed to operate in various driver modes. The DC parameter specifications refer to the pad current limits specified in [Section 4.6.4](#).

Supply Voltage Restrictions

The XC2788X can operate within a wide supply voltage range from 3.0 V to 5.5 V. However, during operation this supply voltage must remain within 10 percent of the selected nominal supply voltage. It cannot vary across the full operating voltage range.

Because of the supply voltage restriction and because electrical behavior depends on the supply voltage, the parameters are specified separately for the upper and the lower voltage range.

During operation, the supply voltages may only change with a maximum speed of $dV/dt < 1 \text{ V/ms}$.

During power-on sequences, the supply voltages may only change with a maximum speed of $dV/dt < 5 \text{ V/}\mu\text{s}$, i.e. the target supply voltage may be reached earliest after approx. 1 μs .

Note: To limit the speed of supply voltage changes, the employment of external buffer capacitors at pins V_{DDPA}/V_{DDPB} is recommended.

4.2.3 Power Consumption

The power consumed by the XC2788X depends on several factors such as supply voltage, operating frequency, active circuits, and operating temperature. The power consumption specified here consists of two components:

- The switching current I_S depends on the device activity
- The leakage current I_{LK} depends on the device temperature

To determine the actual power consumption, always both components, switching current I_S and leakage current I_{LK} must be added:

$$I_{DDP} = I_S + I_{LK}$$

Note: The power consumption values are not subject to production test. They are verified by design/characterization.

To determine the total power consumption for dimensioning the external power supply, also the pad driver currents must be considered.

The given power consumption parameters and their values refer to specific operating conditions:

- **Active mode:**
Regular operation, i.e. peripherals are active, code execution out of Flash.
- **Stopover mode:**
Crystal oscillator and PLL stopped, Flash switched off, clock in domain DMP_1 stopped.
- **Standby mode:**
Voltage domain DMP_1 switched off completely, power supply control switched off. Voltage domain DMP_M is supplied by the ultra low power embedded voltage regulator (ULPEVR). The standard regulator (EVR_M) is switched off.

Note: The maximum values cover the complete specified operating range of all manufactured devices.

The typical values refer to average devices under typical conditions, such as nominal supply voltage, room temperature, application-oriented activity.

After a power reset, the decoupling capacitors for V_{DDIM} and V_{DDI1} are charged with the maximum possible current.

For additional information, please refer to [Section 5.2, Thermal Considerations](#).

Note: Operating Conditions apply.

Table 18 Switching Power Consumption

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power supply current (active) with all peripherals active and EVVRs on	$I_{SACT\ CC}$	–	10 + 1.0 x $f_{SYS}^{1)}$	15 + 1.5 x $f_{SYS}^{1)}$	mA	2)3)
Power supply current in standby mode ⁴⁾	$I_{SSB\ CC}$	–	130	150	μA	Upper voltage range
		–	100	110	μA	Lower voltage range
Power supply current in stopover mode, EVVRs on	$I_{SSO\ CC}$	–	1.6	4	mA	

1) f_{SYS} in MHz.

2) The pad supply voltage pins (V_{DDPB}) provide the input current for the on-chip EVVRs and the current consumed by the pin output drivers. A small current is consumed because the drivers input stages are switched.

In Fast Startup Mode (with the Flash modules deactivated), the typical current is reduced to 3 + 1.0 x f_{SYS} .

3) Please consider the additional conditions described in section "Active Mode Power Supply Current".

4) These values are valid if the voltage validation circuits for V_{DDPB} (SWD) and V_{DDIM} (PVC_M) are off. Leaving SWD and PVC_M active adds another 90 μA.

Active Mode Power Supply Current

The actual power supply current in active mode not only depends on the system frequency but also on the configuration of the XC2788X's subsystem.

Besides the power consumed by the device logic the power supply pins also provide the current that flows through the pin output drivers.

A small current is consumed because the drivers' input stages are switched.

The IO power domains can be supplied separately. Power domain A (V_{DDPA}) supplies the A/D converters and Port 6. Power domain B (V_{DDPB}) supplies the on-chip EVVRs and all other ports.

During operation domain A draws a maximum current of 1.5 mA for each active A/D converter module from V_{DDPA} .

In Fast Startup Mode (with the Flash modules deactivated), the typical current is reduced to (3 + 1.0 x f_{SYS}) mA.

Electrical Parameters

Sample time and conversion time of the XC2788X's A/D converters are programmable. The timing above can be calculated using [Table 23](#).

The limit values for f_{ADCI} must not be exceeded when selecting the prescaler value.

Table 23 A/D Converter Computation Table

GLOBCTR.5-0 (DIVA)	A/D Converter Analog Clock f_{ADCI}	INPCRx.7-0 (STC)	Sample Time¹⁾ t_s
000000 _B	f_{SYS}	00 _H	$t_{\text{ADCI}} \times 2$
000001 _B	$f_{\text{SYS}} / 2$	01 _H	$t_{\text{ADCI}} \times 3$
000010 _B	$f_{\text{SYS}} / 3$	02 _H	$t_{\text{ADCI}} \times 4$
:	$f_{\text{SYS}} / (\text{DIVA}+1)$:	$t_{\text{ADCI}} \times (\text{STC}+2)$
111110 _B	$f_{\text{SYS}} / 63$	FE _H	$t_{\text{ADCI}} \times 256$
111111 _B	$f_{\text{SYS}} / 64$	FF _H	$t_{\text{ADCI}} \times 257$

1) The selected sample time is doubled if broken wire detection is active (due to the presampling phase).

Converter Timing Example A:

Assumptions: $f_{\text{SYS}} = 128 \text{ MHz}$ (i.e. $t_{\text{SYS}} = 7.8 \text{ ns}$), $\text{DIVA} = 06_{\text{H}}$, $\text{STC} = 00_{\text{H}}$

Analog clock $f_{\text{ADCI}} = f_{\text{SYS}} / 7 = 18.3 \text{ MHz}$, i.e. $t_{\text{ADCI}} = 54.7 \text{ ns}$

Sample time $t_s = t_{\text{ADCI}} \times 2 = 109.4 \text{ ns}$

Conversion 12-bit:

$$t_{\text{C10}} = 16 \times t_{\text{ADCI}} + 2 \times t_{\text{SYS}} = 16 \times 54.7 \text{ ns} + 2 \times 7.8 \text{ ns} = 0.891 \text{ } \mu\text{s}$$

Conversion 10-bit:

$$t_{\text{C8}} = 12 \times t_{\text{ADCI}} + 2 \times t_{\text{SYS}} = 12 \times 54.7 \text{ ns} + 2 \times 7.8 \text{ ns} = 0.672 \text{ } \mu\text{s}$$

Converter Timing Example B:

Assumptions: $f_{\text{SYS}} = 40 \text{ MHz}$ (i.e. $t_{\text{SYS}} = 25 \text{ ns}$), $\text{DIVA} = 02_{\text{H}}$, $\text{STC} = 03_{\text{H}}$

Analog clock $f_{\text{ADCI}} = f_{\text{SYS}} / 3 = 13.3 \text{ MHz}$, i.e. $t_{\text{ADCI}} = 75 \text{ ns}$

Sample time $t_s = t_{\text{ADCI}} \times 5 = 375 \text{ ns}$

Conversion 12-bit:

$$t_{\text{C10}} = 19 \times t_{\text{ADCI}} + 2 \times t_{\text{SYS}} = 19 \times 75 \text{ ns} + 2 \times 25 \text{ ns} = 1.475 \text{ } \mu\text{s}$$

Conversion 10-bit:

$$t_{\text{C8}} = 15 \times t_{\text{ADCI}} + 2 \times t_{\text{SYS}} = 15 \times 75 \text{ ns} + 2 \times 25 \text{ ns} = 1.175 \text{ } \mu\text{s}$$

Coding of bit fields LEVxV in SWD Configuration Registers

After power-on the supply watch dog is preconfigured to operate in the lower voltage range.

Table 25 Coding of bit fields LEVxV in Register SWDCON0

Code	Voltage Level	Notes ¹⁾
0000 _B	-	out of valid operation range
0001 _B	3.0 V	LEV1V: reset request
0010 _B - 0101 _B	3.1 V - 3.4 V	step width is 0.1 V
0110 _B	3.6 V	
0111 _B	4.0 V	
1000 _B	4.2 V	
1001 _B	4.5 V	LEV2V: no request
1010 _B - 1110 _B	4.6 V - 5.0 V	step width is 0.1 V
1111 _B	5.5 V	

1) The indicated default levels for LEV1V and LEV2V are selected automatically after a power-on reset.

Coding of bit fields LEVxV in PVC Configuration Registers

The core voltages are controlled internally to the nominal value of 1.5 V; a variation of $\pm 10\%$ is allowed. These operation conditions limit the possible PVC monitoring values to the predefined reset values shown in [Table 26](#).

Table 26 Coding of bit fields LEVxV in Registers PVCyCONz

Code	Voltage Level	Notes ¹⁾
000 _B -011 _B	-	out of valid operation range
100 _B	1.35 V	LEV1V: reset request
101 _B	1.45 V	LEV2V: interrupt request ²⁾
110 _B - 111 _B	-	out of valid operation range

1) The indicated default levels for LEV1V and LEV2V are selected automatically after a power-on reset.

2) Due to variations of the tolerance of both the Embedded Voltage Regulators (EVR) and the PVC levels, this interrupt can be triggered inadvertently, even though the core voltage is within the normal range. It is, therefore, recommended not to use this warning level.

4.6 AC Parameters

These parameters describe the dynamic behavior of the XC2788X.

4.6.1 Testing Waveforms

These values are used for characterization and production testing (except pin XTAL1).

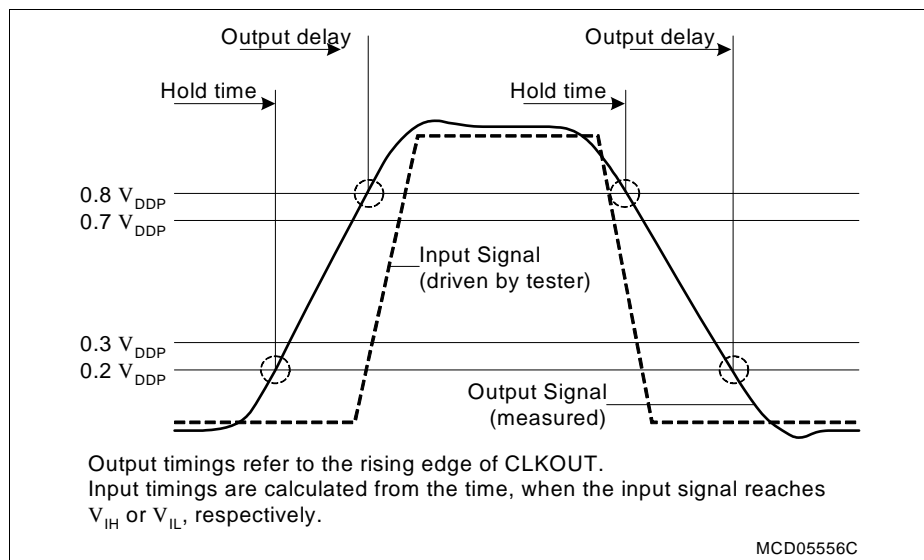


Figure 14 Input Output Waveforms

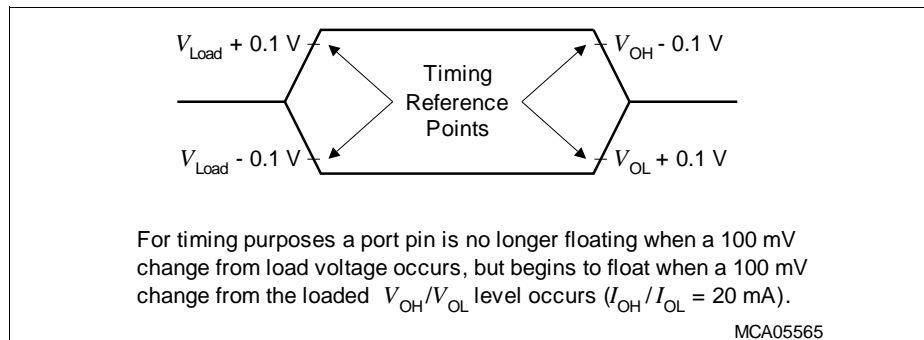


Figure 15 Floating Waveforms

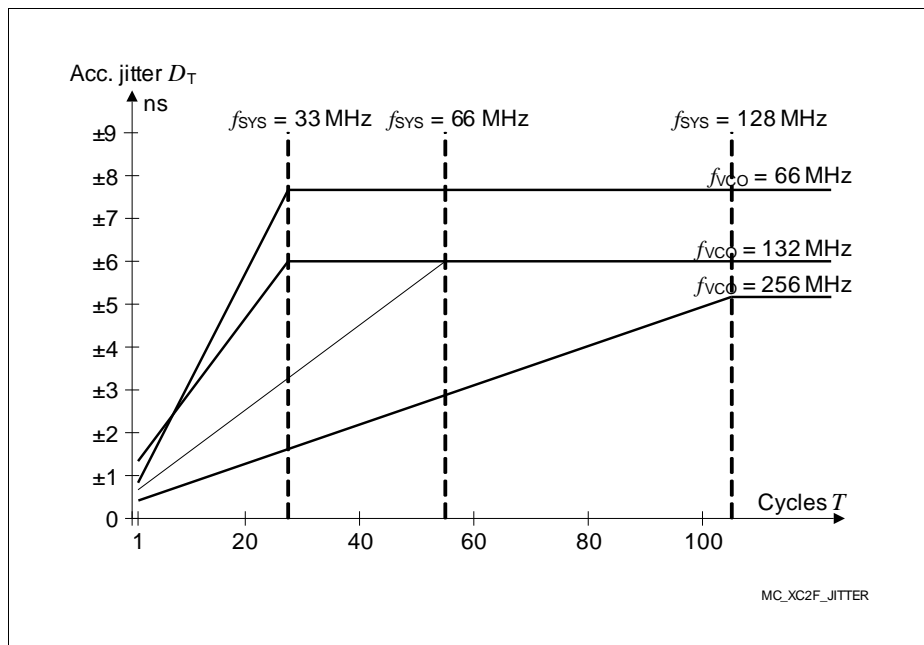


Figure 17 Approximated Accumulated PLL Jitter

Note: The specified PLL jitter values are valid if the capacitive load per pin does not exceed $C_L = 20 \text{ pF}$.

The maximum peak-to-peak noise on the pad supply voltage (measured between V_{DDPB} pin 144 and V_{SS} pin 1) is limited to a peak-to-peak voltage of $V_{PP} = 50 \text{ mV}$. This can be achieved by appropriate blocking of the supply voltage as close as possible to the supply pins and using PCB supply and ground planes.

PLL Frequency Band Selection

Different frequency bands can be selected for the VCO so that the operation of the PLL can be adjusted to a wide range of input and output frequencies:

Table 28 System PLL Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
VCO output frequency (VCO controlled)	f_{VCO} CC	50	–	110	MHz	VCOSEL = 00 _B
		100	–	200	MHz	VCOSEL = 01 _B
		200	–	280	MHz	VCOSEL = 10 _B
VCO output frequency (VCO free-running)	f_{VCO} CC	10	–	40	MHz	VCOSEL = 00 _B
		20	–	80	MHz	VCOSEL = 01 _B
		40	–	160	MHz	VCOSEL = 10 _B

4.6.4 Pad Properties

The output pad drivers of the XC2788X can operate in several user-selectable modes. Strong driver mode allows controlling external components requiring higher currents such as power bridges or LEDs. Reducing the driving power of an output pad reduces electromagnetic emissions (EME). In strong driver mode, selecting a slower edge reduces EME.

The dynamic behavior, i.e. the rise time and fall time, depends on the applied external capacitance that must be charged and discharged. Timing values are given for a capacitance of 20 pF, unless otherwise noted.

In general, the performance of a pad driver depends on the available supply voltage V_{DDP} . Therefore the following tables list the pad parameters for the upper voltage range and the lower voltage range, respectively.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

4.6.7 Debug Interface Timing

The debugger can communicate with the XC2788X either via the 2-pin DAP interface or via the standard JTAG interface.

Debug via DAP

The following parameters are applicable for communication through the DAP debug interface.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply; $C_L = 20$ pF.

Table 40 DAP Interface Timing for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DAP0 clock period	t_{11} SR	25 ¹⁾	—	—	ns	
DAP0 high time	t_{12} SR	8	—	—	ns	
DAP0 low time	t_{13} SR	8	—	—	ns	
DAP0 clock rise time	t_{14} SR	—	—	4	ns	
DAP0 clock fall time	t_{15} SR	—	—	4	ns	
DAP1 setup to DAP0 rising edge	t_{16} SR	6	—	—	ns	pad_type= standard
DAP1 hold after DAP0 rising edge	t_{17} SR	6	—	—	ns	pad_type= standard
DAP1 valid per DAP0 clock period ²⁾	t_{19} CC	17	20	—	ns	pad_type= standard

1) The debug interface cannot operate faster than the overall system, therefore $t_{11} \geq t_{\text{SYS}}$.

2) The Host has to find a suitable sampling point by analyzing the sync telegram response.

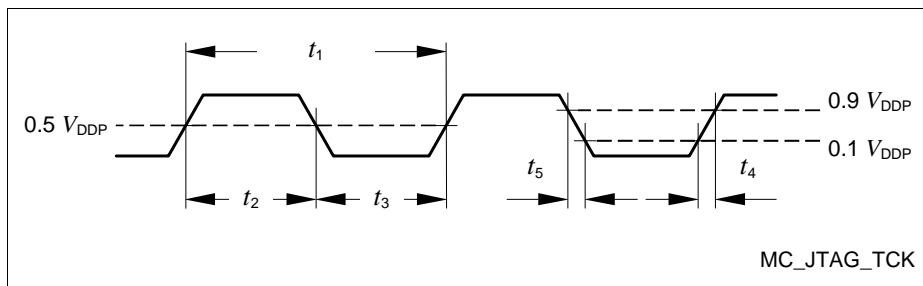


Figure 27 Test Clock Timing (TCK)

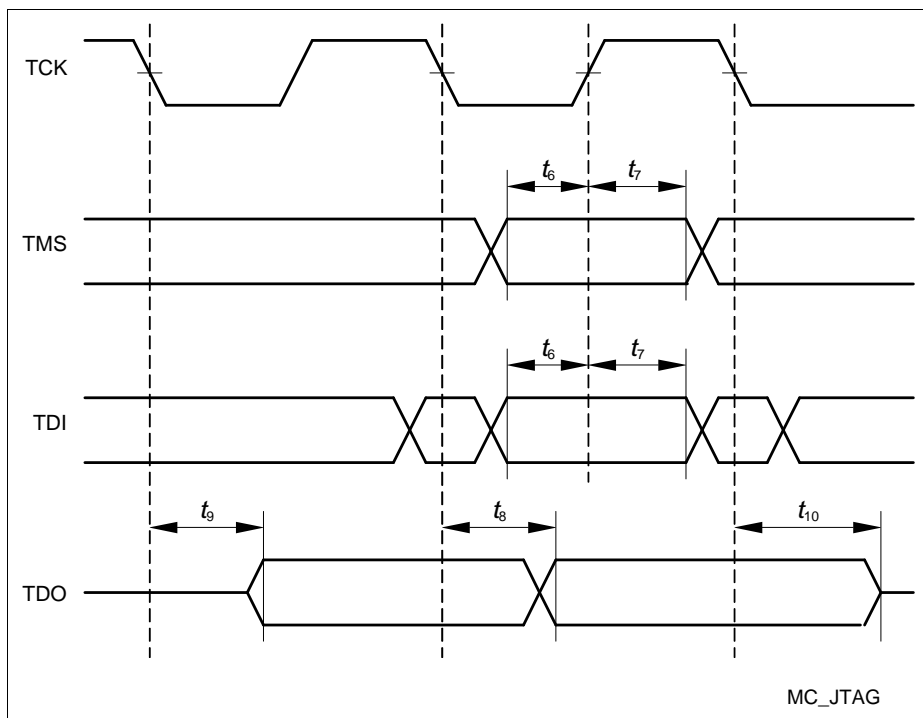


Figure 28 JTAG Timing